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# FDS4935A

# **Dual 30V P-Channel PowerTrench® MOSFET**

## **General Description**

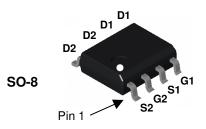
This P-Channel MOSFET is a rugged gate version of Fairchild Semiconductor's advanced PowerTrench process. It has been optimized for power management applications requiring a wide range of gave drive voltage ratings (4.5V  $-\,20$ V).

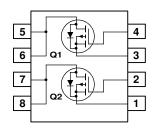
### **Applications**

- · Power management
- Load switch
- · Battery protection

### **Features**

- -7 A, -30 V  $R_{DS(ON)} = 23 \text{ m}\Omega \text{ @ V}_{GS} = -10 \text{ V}$   $R_{DS(ON)} = 35 \text{ m}\Omega \text{ @ V}_{GS} = -4.5 \text{ V}$
- Low gate charge (15nC typical)
- · Fast switching speed
- High performance trench technology for extremely low  $R_{\mbox{\scriptsize DS(ON)}}$
- High power and current handling capability





Absolute Maximum Ratings TA=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units
V <sub>DSS</sub>	Drain-Source Voltage		-30	V
V <sub>GSS</sub>	Gate-Source Voltage		±20	V
I <sub>D</sub>	Drain Current - Continuous	(Note 1a)	<b>-</b> 7	А
	- Pulsed		-30	
P <sub>D</sub>	Power Dissipation for Dual Operation		2	
P <sub>D</sub>	Power Dissipation for Single Operation	(Note 1a)	1.6	W
		(Note 1b)	1	
		(Note 1c)	0.9	
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range		-55 to +175	°C

# **Thermal Characteristics**

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	78	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	40	°C/W

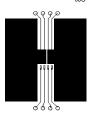
**Package Marking and Ordering Information** 

Device Marking	Device	Reel Size	Tape width	Quantity
FDS4935A	FDS4935A	13"	12mm	2500 units

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Char	racteristics	1				
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = -250 \mu\text{A}$	-30			V
<u>ΔBV<sub>DSS</sub></u> ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D = -250 \mu A$ , Referenced to 25°C		-24		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = -24 \text{ V},  V_{GS} = 0 \text{ V}$			-10	μΑ
I <sub>GSSF</sub>	Gate-Body Leakage, Forward	$V_{GS} = -20 \text{ V},  V_{DS} = 0 \text{ V}$			-100	nA
I <sub>GSSR</sub>	Gate-Body Leakage, Reverse	$V_{GS} = 20 \text{ V}, \qquad V_{DS} = 0 \text{ V}$			100	nA
On Char	acteristics (Note 2)					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = -250 \mu A$	-1	-1.6	-3	V
$\Delta V_{GS(th)} \over \Delta T_J$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250 \mu A$ , Referenced to 25°C		4.4		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	$\begin{split} V_{GS} &= -10 \text{ V}, & I_D = -7 \text{ A} \\ V_{GS} &= -4.5 \text{ V}, & I_D = -5.5 \text{ A} \\ V_{GS} &= -10 \text{ V}, I_D = -7 \text{ A}, T_J = 125 ^{\circ}\text{C} \end{split}$		19 28 26	23 35 34	mΩ
I <sub>D(on)</sub>	On-State Drain Current	$V_{GS} = -10 \text{ V}, \qquad V_{DS} = -5 \text{ V}$	-30			Α
g <sub>FS</sub>	Forward Transconductance	$V_{DS} = -5 \text{ V}, \qquad I_{D} = -7 \text{ A}$		19		S
Dynamic	Characteristics	1	I	I	I	
C <sub>iss</sub>	Input Capacitance	$V_{DS} = -15 \text{ V},  V_{GS} = 0 \text{ V},$		1233		pF
Coss	Output Capacitance	f = 1.0 MHz		311		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			152		pF
Switchin	ng Characteristics (Note 2)		I		I	1
t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD} = -15 \text{ V}, \qquad I_D = -1 \text{ A}, \\ V_{GS} = -10 \text{ V}, \qquad R_{GEN} = 6 \Omega$		13	23	ns
t <sub>r</sub>	Turn-On Rise Time			10	20	ns
t <sub>d(off)</sub>	Turn-Off Delay Time			48	77	ns
t <sub>f</sub>	Turn-Off Fall Time	1		25	40	ns
$\overline{Q_g}$	Total Gate Charge	$V_{DS} = -15 \text{ V}, \qquad I_{D} = -7 \text{ A},$		15	21	nC
$\overline{Q_{gs}}$	Gate-Source Charge	$V_{GS} = -5 \text{ V}$		4.4		nC
Q <sub>ad</sub>	Gate-Drain Charge	1		4.5		nC
3-	ource Diode Characteristics	and Maximum Ratings	<u>I</u>		<u>I</u>	
l <sub>s</sub>	Maximum Continuous Drain–Source				-2.1	Α
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V},  I_S = -2.1 \text{ A}  \text{(Note 2)}$		-0.75	-1.2	V

### Notes:

R<sub>0JA</sub> is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R<sub>0JC</sub> is guaranteed by design while R<sub>0CA</sub> is determined by the user's board design.



a) 78°C/W when mounted on a 0.5in<sup>2</sup> pad of 2 oz copper



b) 125°C/W when mounted on a 0.02 in² pad of 2 oz copper



c) 135°C/W when mounted on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width  $< 300 \mu s$ , Duty Cycle < 2.0%

# **Typical Characteristics**

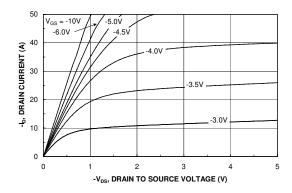


Figure 1. On-Region Characteristics.

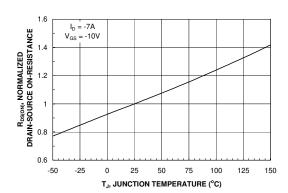


Figure 3. On-Resistance Variation with Temperature.

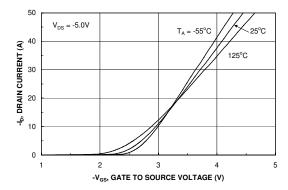


Figure 5. Transfer Characteristics.

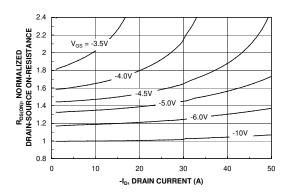


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

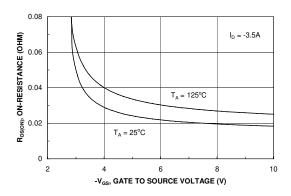


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

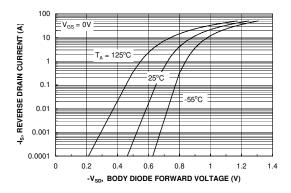
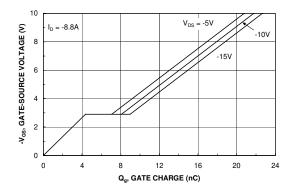


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

# **Typical Characteristics**



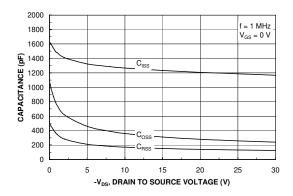
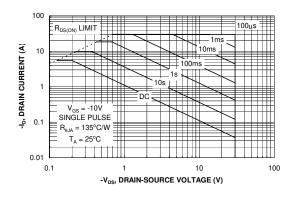


Figure 7. Gate Charge Characteristics.





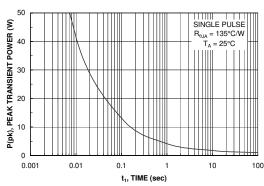


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

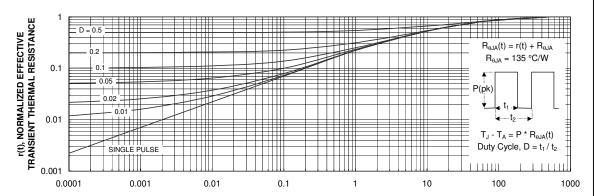


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

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