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FDS6681Z

# FDS6681Z

## 30 Volt P-Channel PowerTrench<sup>®</sup> MOSFET

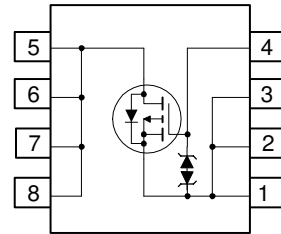
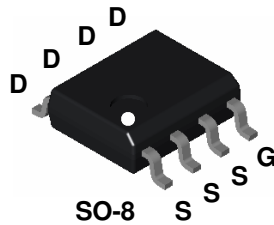
### General Description

This P-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench<sup>®</sup> process that has been especially tailored to minimize the on-state resistance.

This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

### Features

- -20 A, -30 V.  $R_{DS(ON)} = 4.6\text{ m}\Omega @ V_{GS} = -10\text{ V}$   
 $R_{DS(ON)} = 6.5\text{ m}\Omega @ V_{GS} = -4.5\text{ V}$
- Extended  $V_{GSS}$  range (-25V) for battery applications
- HBM ESD protection level of 8kV typical (note 3)
- High performance trench technology for extremely low  $R_{DS(ON)}$
- High power and current handling capability
- Termination is Lead-free and RoHS Compliant



### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-Source Voltage	-30	V
$V_{GSS}$	Gate-Source Voltage	$\pm 25$	V
$I_D$	Drain Current – Continuous (Note 1a)	-20	A
	– Pulsed	-105	
$P_D$	Power Dissipation for Single Operation (Note 1a) (Note 1b) (Note 1c)	2.5	W
		1.2	
		1.0	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	50	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case (Note 1)	25	$^\circ\text{C/W}$

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
FDS6681Z	FDS6681Z	13"	12mm	2500 units

**Electrical Characteristics** $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Off Characteristics</b>						
$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-26		mV/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}$			-1	$\mu\text{A}$
$I_{GSS}$	Gate–Body Leakage	$V_{GS} = \pm 25\text{ V}, V_{DS} = 0\text{ V}$			$\pm 10$	$\mu\text{A}$
<b>On Characteristics (Note 2)</b>						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-1	-1.8	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		6		mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = -10\text{ V}, I_D = -20\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -17\text{ A}$ $V_{GS} = -10\text{ V}, I_D = -20\text{ A}, T_J = 125^\circ\text{C}$		3.8 5.2 5.0	4.6 6.5 6.3	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = -5\text{ V}, I_D = -20\text{ A}$		79		S
<b>Dynamic Characteristics</b>						
$C_{iss}$	Input Capacitance	$V_{DS} = -15\text{ V}, V_{GS} = 0\text{ V},$		7540		pF
$C_{oss}$	Output Capacitance	$f = 1.0\text{ MHz}$		1400		pF
$C_{rss}$	Reverse Transfer Capacitance			1120		pF
<b>Switching Characteristics (Note 2)</b>						
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = -15\text{ V}, I_D = -1\text{ A},$		20	35	ns
$t_r$	Turn–On Rise Time	$V_{GS} = -10\text{ V}, R_{GEN} = 6\ \Omega$		9	18	ns
$t_{d(off)}$	Turn–Off Delay Time			660	1060	ns
$t_f$	Turn–Off Fall Time			380	610	ns
$Q_{g(TOT)}$	Total Gate Charge at $V_{GS} = -10\text{V}$	$V_{DS} = -15\text{ V}, I_D = -20\text{ A}$		185	260	nC
$Q_{g(TOT)}$	Total Gate Charge at $V_{GS} = -5\text{V}$			105	150	nC
$Q_{gs}$	Gate–Source Charge			26		nC
$Q_{gd}$	Gate–Drain Charge			47		nC

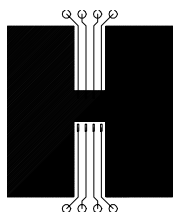
## Electrical Characteristics

$T_A = 25^\circ\text{C}$  unless otherwise noted

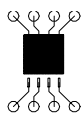
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
<b>Drain–Source Diode Characteristics and Maximum Ratings</b>						
$I_S$	Maximum Continuous Drain–Source Diode Forward Current				-2.1	A
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -2.1\text{ A}$ (Note 2)		-0.7	-1.2	V
$t_{RR}$	Reverse Recovery Time	$I_F = -20\text{ A},$		125		ns
$Q_{RR}$	Reverse Recovery Charge	$dI_F/dt = 100\text{ A}/\mu\text{s}$ (Note 2)		94		nC

**Notes:**

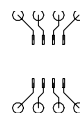
1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a)  $50^\circ\text{C}/\text{W}$  (10 sec)  
 $62.5^\circ\text{C}/\text{W}$  steady state  
 when mounted on a  
 $1\text{ in}^2$  pad of 2 oz  
 copper



b)  $105^\circ\text{C}/\text{W}$  when  
 mounted on a  $.04\text{ in}^2$   
 pad of 2 oz copper



c)  $125^\circ\text{C}/\text{W}$  when mounted  
 on a minimum pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width <  $300\mu\text{s}$ , Duty Cycle < 2.0%

3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

### Typical Characteristics

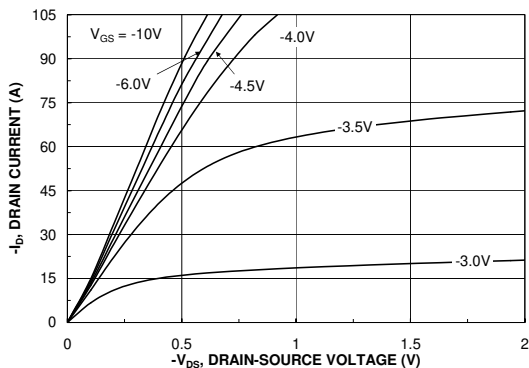


Figure 1. On-Region Characteristics.

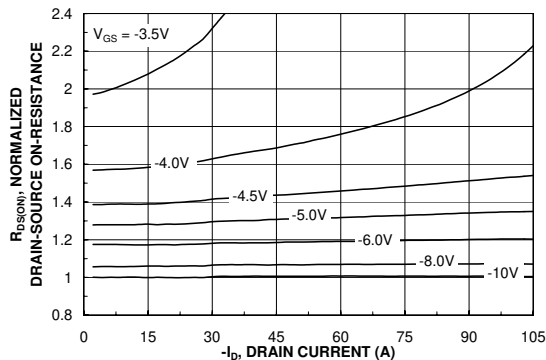


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

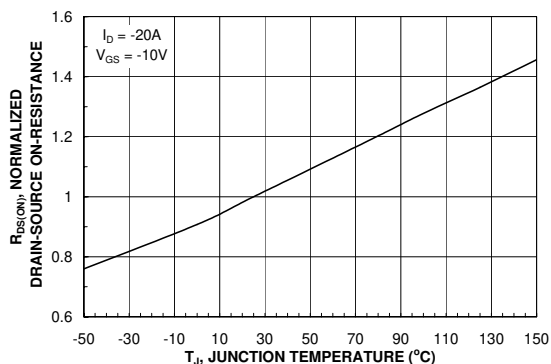


Figure 3. On-Resistance Variation with Temperature.

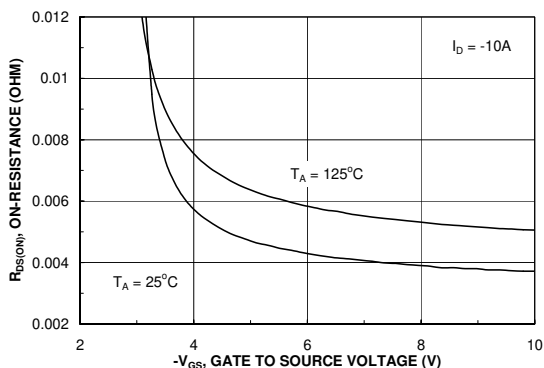


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

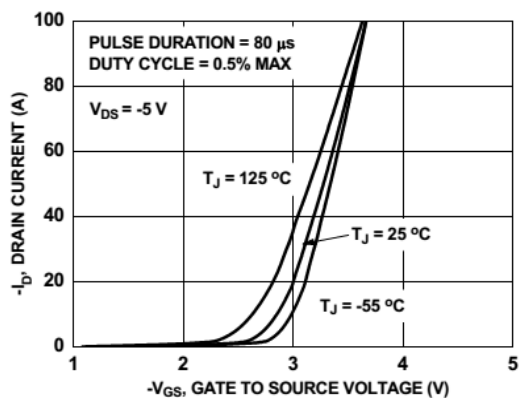


Figure 5. Transfer Characteristics.

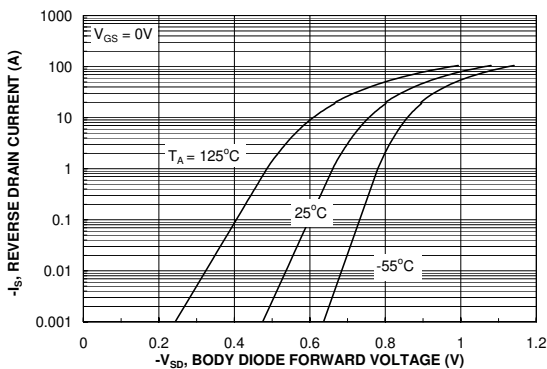


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.



### Typical Characteristics

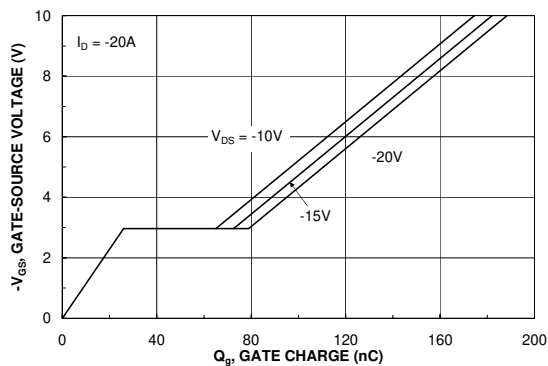


Figure 7. Gate Charge Characteristics.

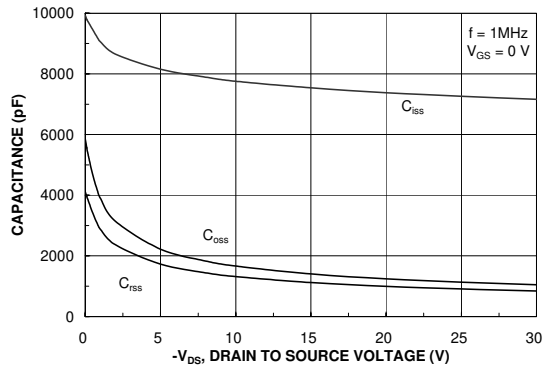


Figure 8. Capacitance Characteristics.

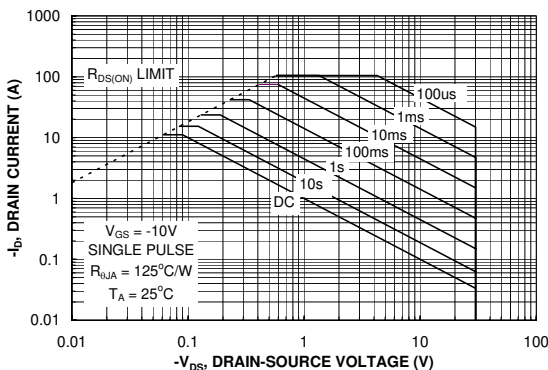


Figure 9. Maximum Safe Operating Area.

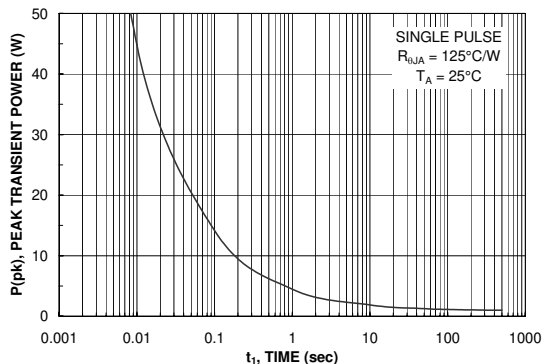


Figure 10. Single Pulse Maximum Power Dissipation.

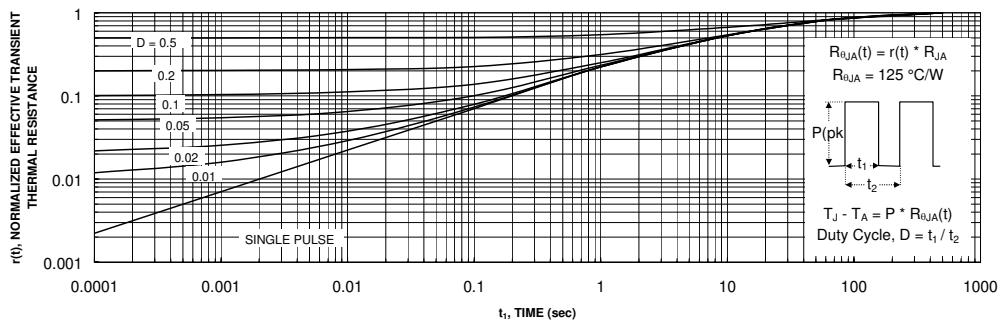
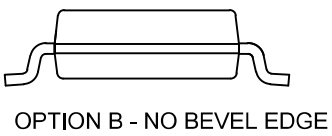
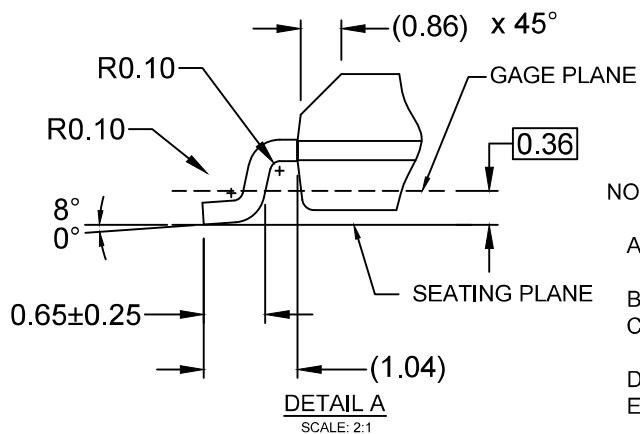
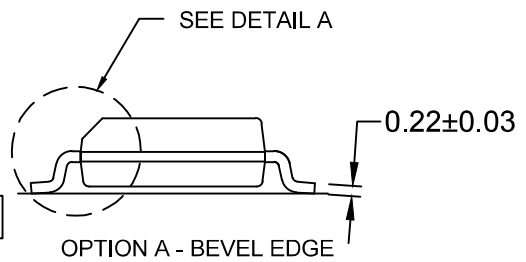
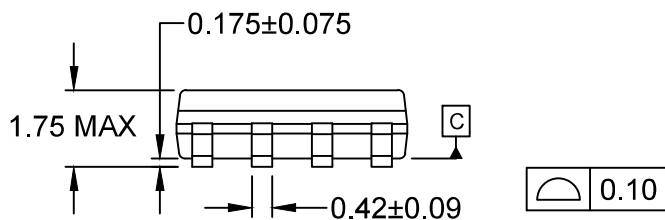
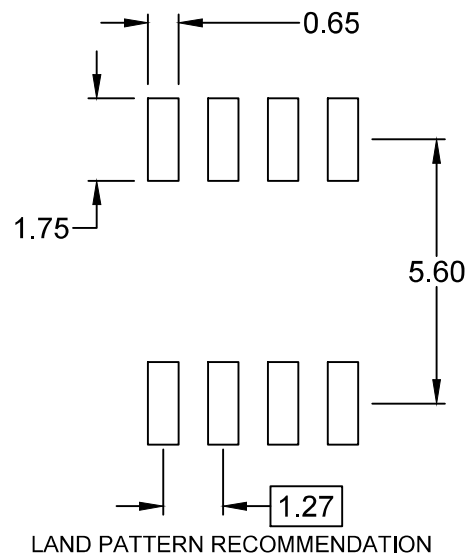
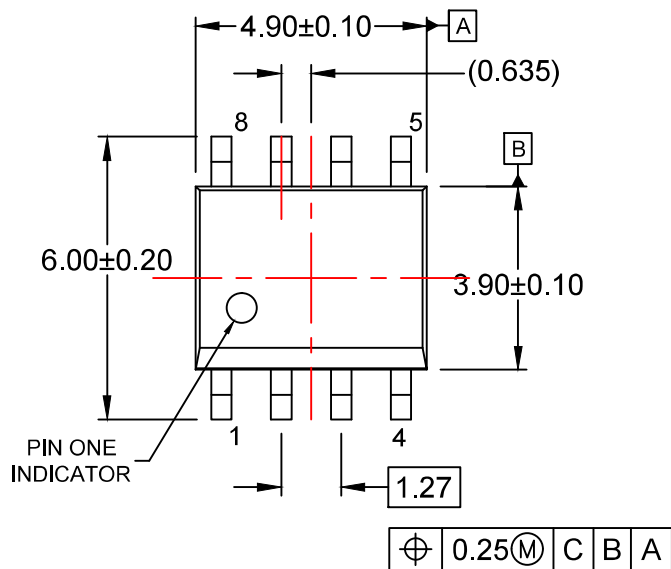


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.



NOTES:

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
- D) LANDPATTERN STANDARD: SOIC127P600X175-8M
- E) DRAWING FILENAME: M08Arev16





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