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FDS6910

Dual N-Channel Logic Level PowerTrench® MOSFET

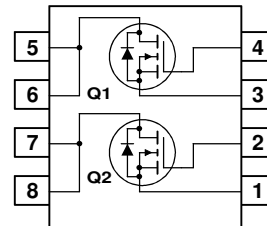
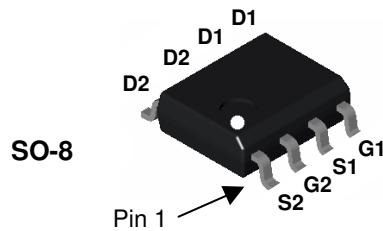
General Description

These N-Channel Logic Level MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

These devices are well suited for low voltage and battery powered applications where low in-line power loss and fast switching are required.

Features

- 7.5 A, 30 V. $R_{DS(ON)} = 13 \text{ m}\Omega @ V_{GS} = 10 \text{ V}$
 $R_{DS(ON)} = 17 \text{ m}\Omega @ V_{GS} = 4.5 \text{ V}$
- Fast switching speed
- Low gate charge
- High performance trench technology for extremely low $R_{DS(ON)}$
- High power and current handling capability



Absolute Maximum Ratings T_A=25°C unless otherwise noted

| Symbol | Parameter | Rated | Units |
|-----------------------------------|--|---------------|-------|
| V _{DSS} | Drain-Source Voltage | 30 | V |
| V _{GSS} | Gate-Source Voltage | ± 20 | V |
| I _D | Drain Current – Continuous (Note 1a) | 7.5 | A |
| | | 20 | |
| P _D | Power Dissipation for Single Operation (Note 1a) | 1.6 | W |
| | | 1.0 (Note 1b) | |
| | | 0.9 (Note 1c) | |
| T _J , T _{STG} | Operating and Storage Junction Temperature Range | -55 to +150 | °C |

Thermal Characteristics

| | | | |
|------------------|---|----|------|
| R _{θJA} | Thermal Resistance, Junction-to-Ambient (Note 1a) | 78 | °C/W |
| R _{θJC} | Thermal Resistance, Junction-to-Case (Note 1) | 40 | °C/W |

Package Marking and Ordering Information

| Device Marking | Device | Reel Size | Tape width | Quantity |
|----------------|---------|-----------|------------|------------|
| FDS6910 | FDS6910 | 13" | 12mm | 2500 units |

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

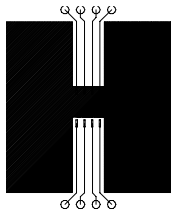
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|--|--|-----|--------------------|----------------|----------------------|
| Off Characteristics | | | | | | |
| BV_{DSS} | Drain–Source Breakdown Voltage | $V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$ | 30 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D = 250\ \mu\text{A}$, Referenced to 25°C | | 28 | | mV/ $^\circ\text{C}$ |
| I_{DSS} | Zero Gate Voltage Drain Current | $V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}, T_J = 55^\circ\text{C}$ | | | 1 10 | μA |
| I_{GSS} | Gate–Source Leakage | $V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$ | | | ± 100 | nA |
| On Characteristics (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$ | 1 | 1.8 | 3 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D = 250\ \mu\text{A}$, Referenced to 25°C | | -4.7 | | mV/ $^\circ\text{C}$ |
| $R_{DS(on)}$ | Static Drain–Source On–Resistance | $V_{GS} = 10\text{ V}, I_D = 7.5\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 6.5\text{ A}$ $V_{GS} = 10\text{ V}, I_D = 7.5\text{ A}, T_J = 125^\circ\text{C}$ | | 10.6 13 14.5 | 13 17 20 | m Ω |
| $I_{D(on)}$ | On–State Drain Current | $V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$ | 20 | | | A |
| g_{FS} | Forward Transconductance | $V_{DS} = 5\text{ V}, I_D = 7.5\text{ A}$ | | 36 | | S |
| Dynamic Characteristics | | | | | | |
| C_{iss} | Input Capacitance | $V_{DS} = 15\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$ | | 1130 | | pF |
| C_{oss} | Output Capacitance | | | 300 | | pF |
| C_{rss} | Reverse Transfer Capacitance | | | 100 | | pF |
| R_G | Gate Resistance | $V_{GS} = 15\text{ mV}, f = 1.0\text{ MHz}$ | | 2.4 | | Ω |
| Switching Characteristics (Note 2) | | | | | | |
| $t_{d(on)}$ | Turn–On Delay Time | $V_{DD} = 15\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 10\text{ V}, R_{GEN} = 6\ \Omega$ | | 9 | 18 | ns |
| t_r | Turn–On Rise Time | | | 5 | 10 | ns |
| $t_{d(off)}$ | Turn–Off Delay Time | | | 26 | 42 | ns |
| t_f | Turn–Off Fall Time | | | 7 | 14 | ns |
| $Q_{g(TOT)}$ | Total Gate Charge at $V_{GS}=10\text{V}$ | $V_{DD} = 15\text{ V}, I_D = 7.5\text{ A},$ | | 17 | 24 | nC |
| Q_g | Total Gate Charge at $V_{GS}=5\text{V}$ | | | 9 | 13 | nC |
| Q_{gs} | Gate–Source Charge | | | 3.1 | | nC |
| Q_{gd} | Gate–Drain Charge | | | 2.7 | | nC |

Electrical Characteristics **TA = 25°C unless otherwise noted**

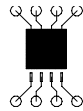
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|--|-----|-----|-----|-------|
| Drain–Source Diode Characteristics and Maximum Ratings | | | | | | |
| I_S | Maximum Continuous Drain–Source Diode Forward Current | | | | 1.3 | A |
| V_{SD} | Drain–Source Diode Forward Voltage | $V_{GS} = 0\text{ V}, I_S = 1.3\text{ A}$ (Note 2) | | | 1.2 | V |
| t_{rr} | Diode Reverse Recovery Time | $I_F = 7.5\text{ A}, dI_F/dt = 100\text{ A}/\mu\text{s}$ | | 24 | | nS |
| Q_{rr} | Diode Reverse Recovery Charge | | | 13 | | nC |

Notes:

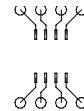
1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 78°C/W when mounted on a 0.5in² pad of 2 oz copper



b) 125°C/W when mounted on a 0.02 in² pad of 2 oz copper



c) 135°C/W when mounted on a minimum mounting pad.

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width < 300μs, Duty Cycle < 2.0%

Typical Characteristics

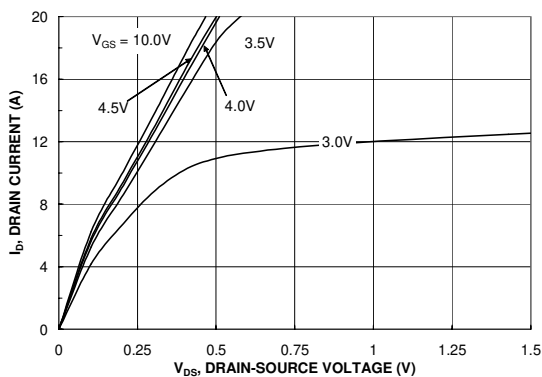


Figure 1. On-Region Characteristics.

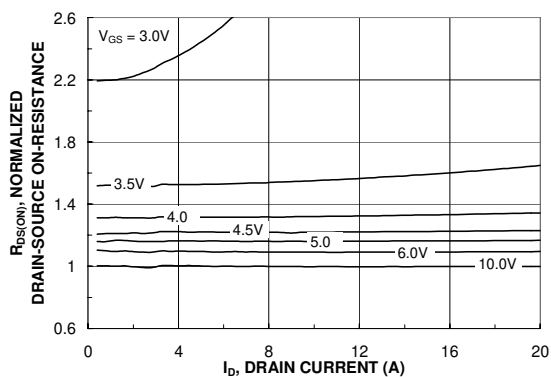


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

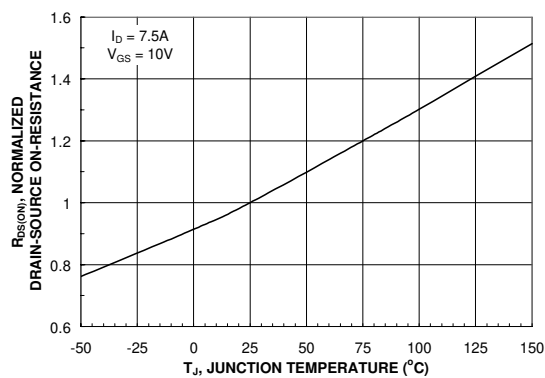


Figure 3. On-Resistance Variation with Temperature.

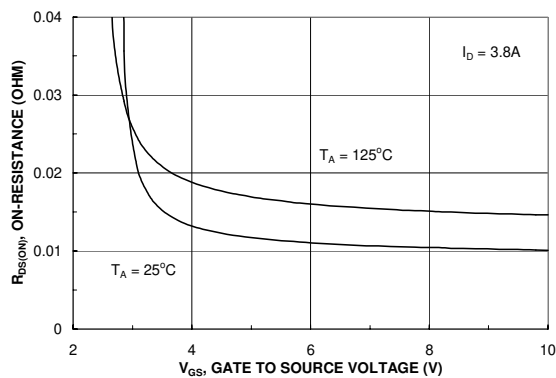


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

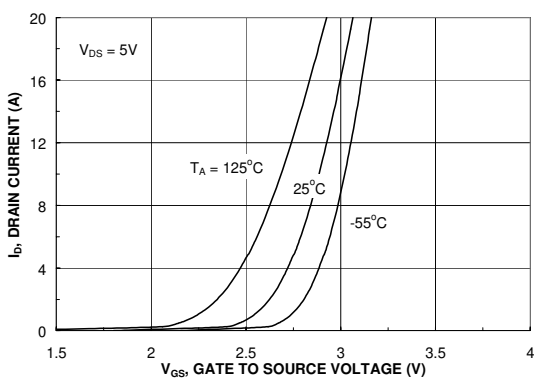


Figure 5. Transfer Characteristics.

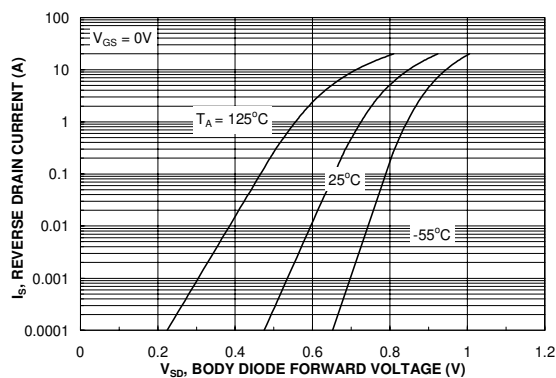


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics

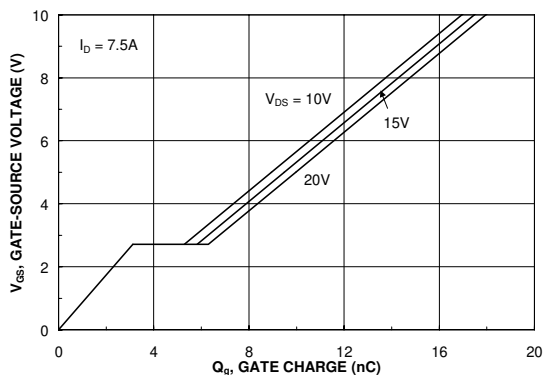


Figure 7. Gate Charge Characteristics.

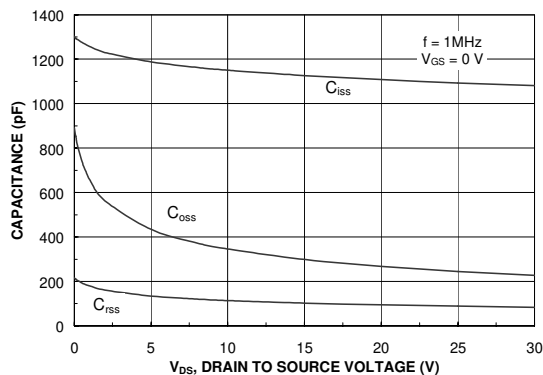


Figure 8. Capacitance Characteristics.

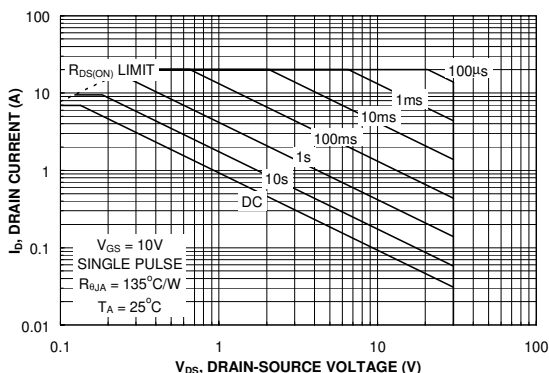


Figure 9. Maximum Safe Operating Area.

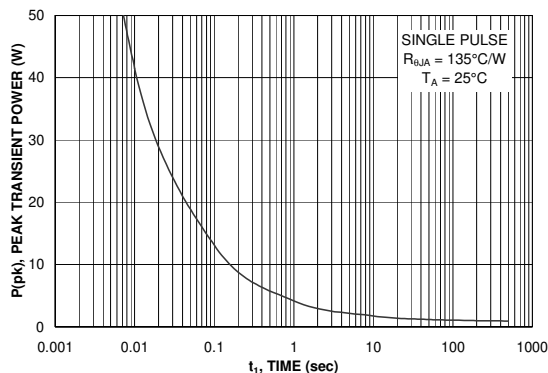


Figure 10. Single Pulse Maximum Power Dissipation.

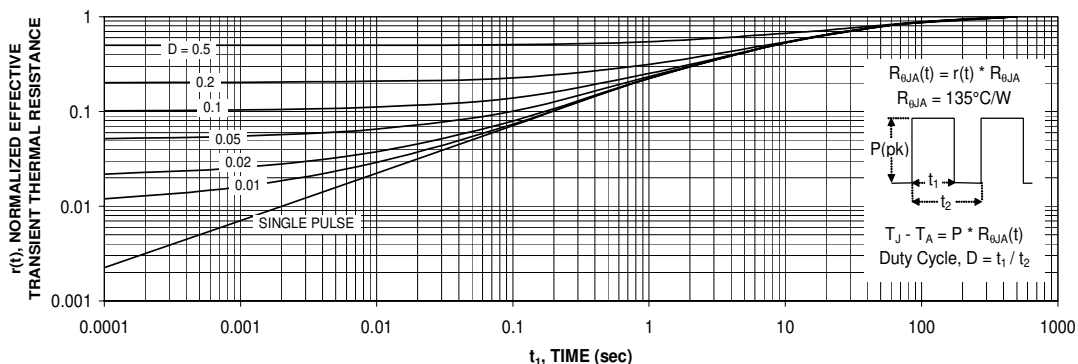


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

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