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# FDS8882

## N-Channel PowerTrench® MOSFET

30 V, 9 A, 20.0 mΩ

### Features

- Max  $r_{DS(on)}$  = 20.0 mΩ at  $V_{GS} = 10$  V,  $I_D = 9$  A
- Max  $r_{DS(on)}$  = 22.5 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 8$  A
- High performance trench technology for extremely low  $r_{DS(on)}$  and fast switching
- High power and current handling capability
- Termination is Lead-free and RoHS Compliant

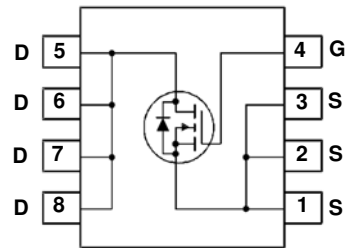
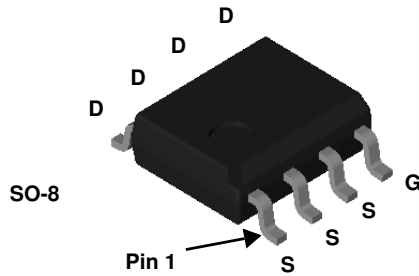


### General Description

The FDS8882 has been designed to minimize losses in power conversion application. Advancements in both silicon and package technologies have been combined to offer the lowest  $r_{DS(on)}$  while maintaining excellent switching performance.

### Applications

- Notebook System Regulators
- DC/DC Converters



### MOSFET Maximum Ratings $T_A = 25$ °C unless otherwise noted

Symbol	Parameter	Rated	Units
$V_{DS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current -Continuous	9	A
	-Pulsed	21	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	32	mJ
$P_D$	Power Dissipation $T_A = 25$ °C (Note 1a)	2.5	W
	Power Dissipation $T_A = 25$ °C (Note 1b)	1.0	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)	25	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDS8882	FDS8882	SO8	13 "	12 mm	2500 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		4		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$ , $V_{DS} = 0\text{ V}$			$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	1.0	1.7	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-6		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 9\text{ A}$		13.2	20.0	m $\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 8\text{ A}$		16.6	22.5	
		$V_{GS} = 10\text{ V}$ , $I_D = 9\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		18.5	28.0	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}$ , $I_D = 9\text{ A}$		36		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$		707	940	pF
$C_{oss}$	Output Capacitance			138	185	pF
$C_{rss}$	Reverse Transfer Capacitance			88	135	pF
$R_g$	Gate Resistance			1.8		$\Omega$

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}$ , $I_D = 9\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		7	14	ns
$t_r$	Rise Time			3	10	ns
$t_{d(off)}$	Turn-Off Delay Time			19	35	ns
$t_f$	Fall Time			4	10	ns
$Q_g$	Total Gate Charge		$V_{GS} = 0\text{ V to } 10\text{ V}$	$V_{DD} = 15\text{ V}$ , $I_D = 9\text{ A}$	14	20
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{ V to } 5\text{ V}$	8		11	nC
$Q_{gs}$	Gate to Source Charge		2.2			nC
$Q_{gd}$	Gate to Drain "Miller" Charge		2.8			nC

### Drain-Source Diode Characteristics

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 9\text{ A}$		0.8	1.2	V
		$V_{GS} = 0\text{ V}$ , $I_S = 2.1\text{ A}$		0.7	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 9\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		17	31	ns
$Q_{rr}$	Reverse Recovery Charge			6	12	nC

#### NOTES:

- $R_{\theta JA}$  is determined with the device mounted on a  $1\text{ in}^2$  pad of 2 oz copper on a  $1.5 \times 1.5\text{ in.}$  board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



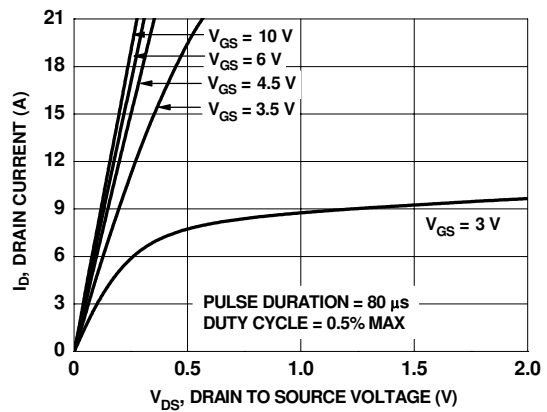
a)  $50\text{ }^\circ\text{C}/\text{W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper.



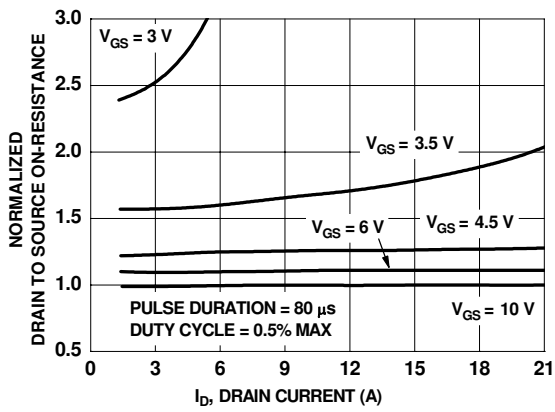
b)  $125\text{ }^\circ\text{C}/\text{W}$  when mounted on a minimum pad.

- Pulse Test: Pulse Width <  $300\text{ }\mu\text{s}$ , Duty cycle < 2.0%.
- Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 1\text{ mH}$ ,  $I_{AS} = 8\text{ A}$ ,  $V_{DD} = 27\text{ V}$ ,  $V_{GS} = 10\text{ V}$ .

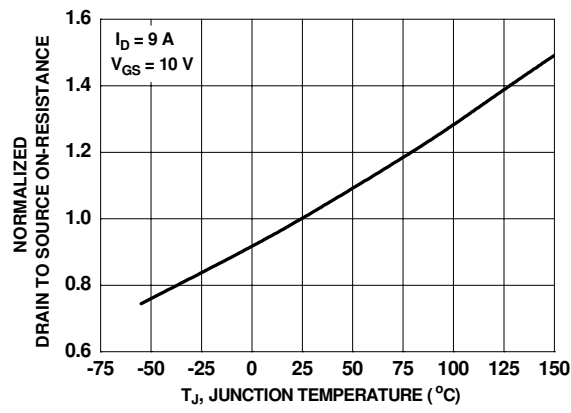
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



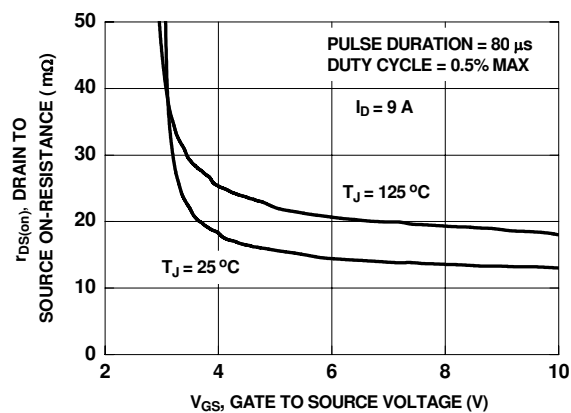
**Figure 1. On Region Characteristics**



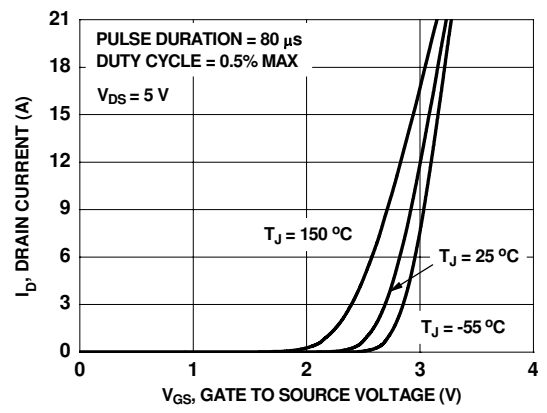
**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**



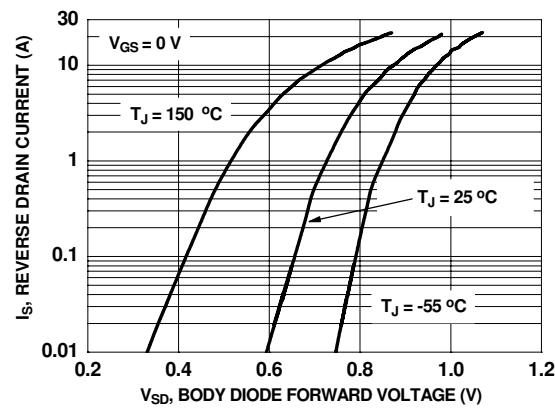
**Figure 3. Normalized On Resistance vs Junction Temperature**



**Figure 4. On-Resistance vs Gate to Source Voltage**

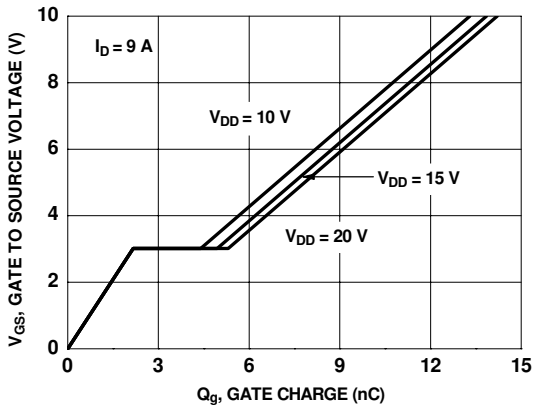


**Figure 5. Transfer Characteristics**

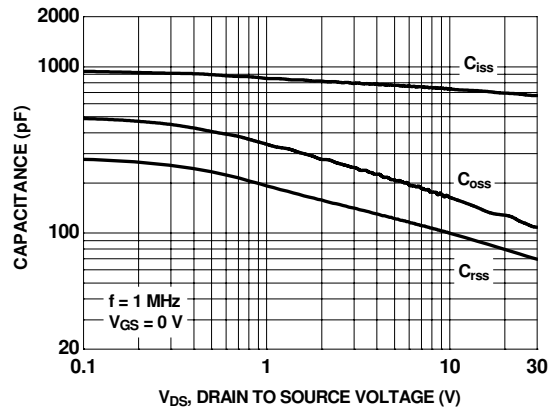


**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

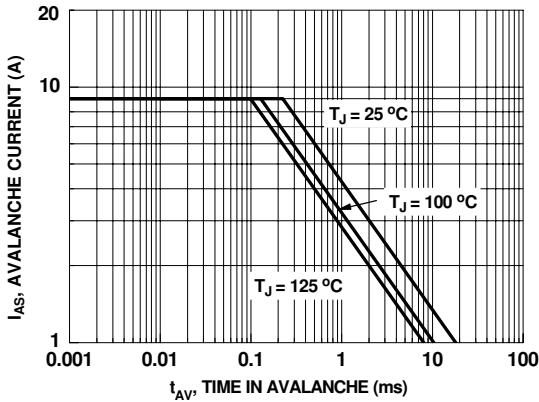
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted



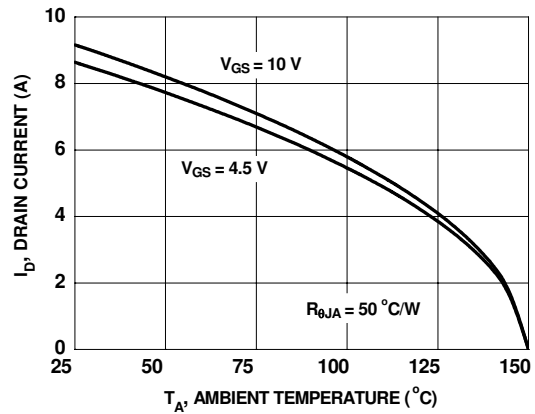
**Figure 7. Gate Charge Characteristics**



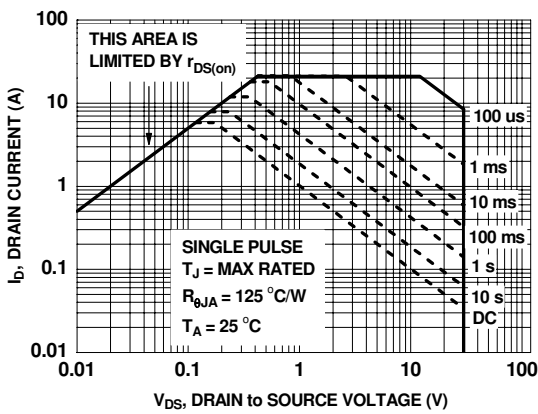
**Figure 8. Capacitance vs Drain to Source Voltage**



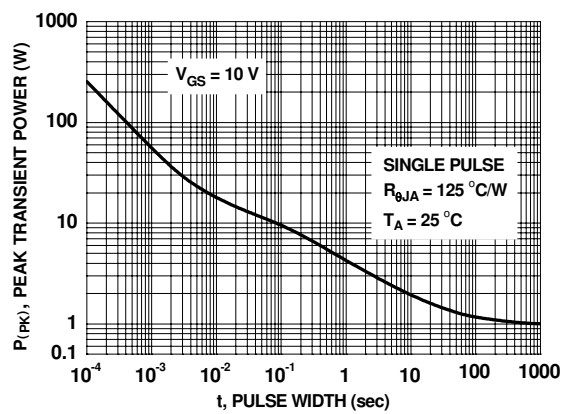
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs Ambient Temperature**

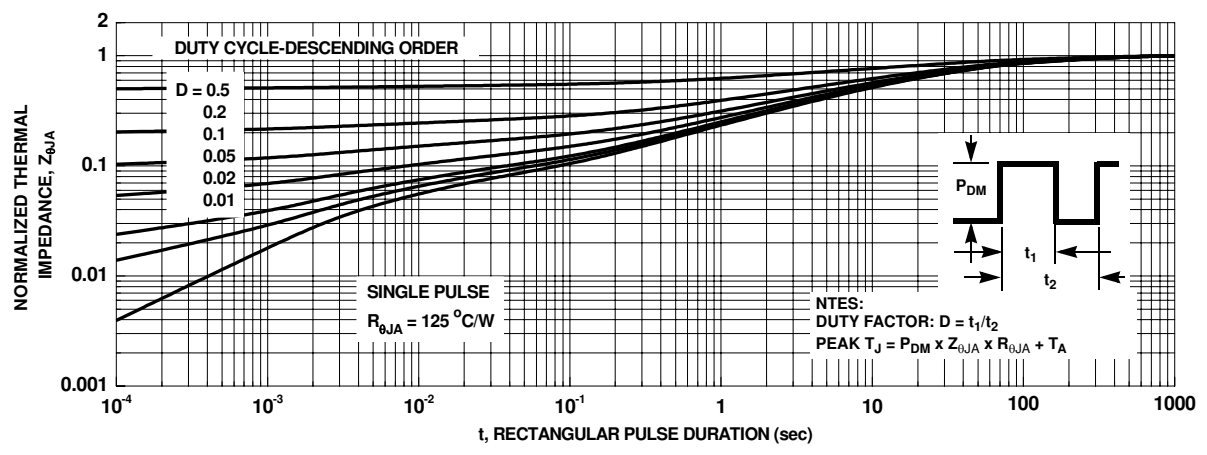


**Figure 11. Forward Bias Safe Operating Area**



**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted









**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**



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