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FDS9435A

30V P-Channel PowerTrench® MOSFET

General Description

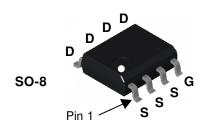
This P-Channel MOSFET is a rugged gate version of Fairchild Semiconductor's advanced PowerTrench process. It has been optimized for power management applications requiring a wide range of gave drive voltage ratings (4.5V-25V).

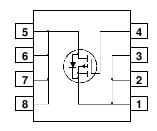
Applications

- Power management
- · Load switch
- · Battery protection

Features

- -5.3 A, -30 V $R_{DS(ON)} = 50 \text{ m}\Omega$ @ $V_{GS} = -10 \text{ V}$ $R_{DS(ON)} = 80 \text{ m}\Omega$ @ $V_{GS} = -4.5 \text{ V}$
- · Low gate charge
- · Fast switching speed
- High performance trench technology for extremely low R_{DS(ON)}
- High power and current handling capability





Absolute Maximum Ratings T_A=25°C unless otherwise noted

| Symbol | Parameter | | Ratings | Units |
|-----------------------------------|--|-----------|-------------|-------|
| V _{DSS} | Drain-Source Voltage | | -30 | V |
| V _{GSS} | Gate-Source Voltage | | ±25 | V |
| I _D | Drain Current - Continuous | (Note 1a) | -5.3 | Α |
| | - Pulsed | | -50 | |
| P _D | Power Dissipation for Single Operation | (Note 1a) | 2.5 | W |
| | | (Note 1b) | 1.2 | |
| | | (Note 1c) | 1 | |
| T _J , T _{STG} | Operating and Storage Junction Temperature Range | | -55 to +175 | °C |

Thermal Characteristics

| R _{0JA} | Thermal Resistance, Junction-to-Ambient | (Note 1a) | 50 | °C/W | |
|------------------|---|-----------|-----|------|--|
| R _{0JA} | Thermal Resistance, Junction-to-Ambient | (Note 1c) | 125 | °C/W | |
| Rejc | Thermal Resistance, Junction-to-Case | (Note 1) | 25 | °C/W | |

Package Marking and Ordering Information

| Device Marking | Device | Reel Size | Tape width | Quantity |
|-------------------|--------|-----------|------------|----------|
| FDS9435A FDS9435A | | 13" | 13" 12mm | |

| Symbol | Parameter | Test Conditions | Min | Тур | Max | Units |
|--|---|--|-----|----------------|----------------|-------|
| Off Char | acteristics | | | I | ı | |
| BV _{DSS} | Drain-Source Breakdown Voltage | $V_{GS} = 0 \text{ V}, I_D = -250 \mu\text{A}$ | -30 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_{J}}$ | Breakdown Voltage Temperature Coefficient | $I_D = -250 \mu A$, Referenced to 25°C | | -23 | | mV/°C |
| DSS | Zero Gate Voltage Drain Current | $V_{DS} = -24 \text{ V}, V_{GS} = 0 \text{ V}$ | | | -1 | μΑ |
| GSSF | Gate-Body Leakage, Forward | $V_{GS} = 25 \text{ V}, \qquad V_{DS} = 0 \text{ V}$ | | | 100 | nA |
| IGSSR | Gate-Body Leakage, Reverse | $V_{GS} = -25 \text{ V}$ $V_{DS} = 0 \text{ V}$ | | | -100 | nA |
| On Char | acteristics (Note 2) | | | | | |
| V _{GS(th)} | Gate Threshold Voltage | $V_{DS} = V_{GS}, I_D = -250 \mu A$ | -1 | -1.7 | -3 | ٧ |
| $\Delta V_{GS(th)} \over \Delta T_J$ | Gate Threshold Voltage Temperature Coefficient | $I_D = -250 \mu A$, Referenced to 25°C | | 4.5 | | mV/°C |
| R _{DS(on)} | Static Drain-Source On-Resistance | $V_{GS} = -10 \text{ V}, I_D = -5.3 \text{ A}$ $V_{GS} = -4.5 \text{ V}, I_D = -4 \text{ A}$ $V_{GS} = -10 \text{ V}, I_D = -5.3 \text{ A}, T_J = 125^{\circ}\text{C}$ | | 42 65 57 | 50 80 77 | mΩ |
| I _{D(on)} | On-State Drain Current | $V_{GS} = -10 \text{ V}, \qquad V_{DS} = -5 \text{ V}$ | -25 | | | Α |
| g FS | Forward Transconductance | $V_{DS} = -5 \text{ V}, \qquad I_{D} = -5.3 \text{ A}$ | | 10 | | S |
| Dynamic | Characteristics | | | I. | | |
| C _{iss} | Input Capacitance | $V_{DS} = -15 \text{ V}, V_{GS} = 0 \text{ V},$ | | 528 | | pF |
| Coss | Output Capacitance | f = 1.0 MHz | | 132 | | pF |
| C _{rss} | Reverse Transfer Capacitance | | | 70 | | pF |
| Switchin | g Characteristics (Note 2) | | | I | I | |
| t _{d(on)} | Turn-On Delay Time | $V_{DD} = -15 \text{ V}, \qquad I_D = -1 \text{ A},$ | | 7 | 14 | ns |
| t _r | Turn-On Rise Time | $V_{GS} = -10 \text{ V}, \qquad R_{GEN} = 6 \Omega$ | | 13 | 24 | ns |
| t _{d(off)} | Turn-Off Delay Time | | | 14 | 25 | ns |
| t _f | Turn-Off Fall Time | | | 9 | 17 | ns |
| Qg | Total Gate Charge | $V_{DS} = -15 \text{ V}, I_{D} = -4 \text{ A},$ | | 10 | 14 | nC |
| Q _{gs} | Gate-Source Charge | V _{GS} = -10 V | | 2.2 | | nC |
| Q _{gd} | Gate-Drain Charge | 1 | | 2 | | nC |
| Drain-Se | ource Diode Characteristics | and Maximum Ratings | | | 1 | 1 |
| ls | Maximum Continuous Drain-Source | | | | -2.1 | Α |
| V _{SD} | Drain-Source Diode Forward Voltage | V _{GS} = 0 V, I _S = -2.1 A (Note 2) | | -0.8 | -1.2 | V |

Notes:

R_{BUA} is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. R_{BUC} is guaranteed by design while R_{BCA} is determined by the user's board design.



a) 50°C/W when mounted on a 1irf pad of 2 oz copper



b) 105°C/W when mounted on a .04 in² pad of 2 oz copper



c) 125°C/W when mounted on a minimum pad.

Scale 1:1 on letter size paper

2. Pulse Test: Pulse Width < $300\mu s,$ Duty Cycle < 2.0%

Typical Characteristics

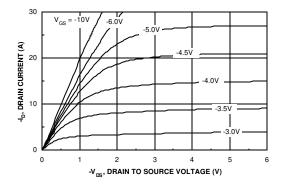


Figure 1. On-Region Characteristics.

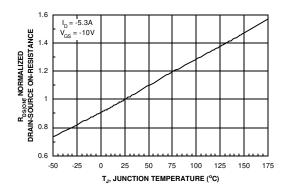


Figure 3. On-Resistance Variation with Temperature.

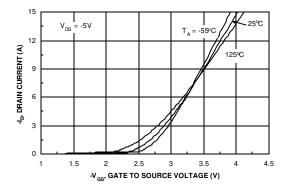


Figure 5. Transfer Characteristics.

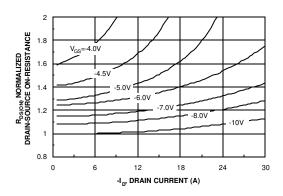


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

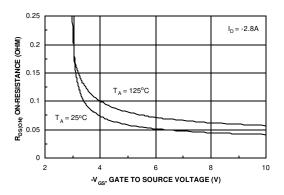


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

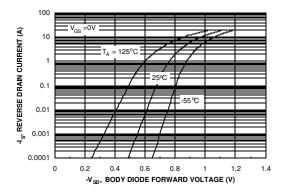
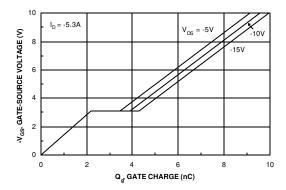


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

Typical Characteristics



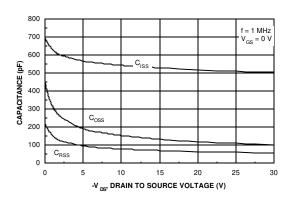
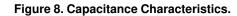
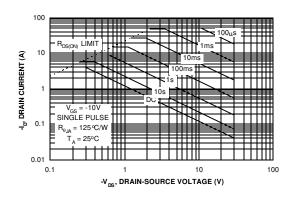


Figure 7. Gate Charge Characteristics.





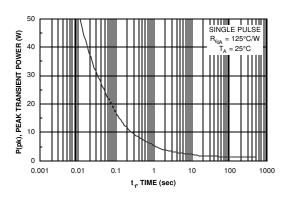


Figure 9. Maximum Safe Operating Area.

Figure 10. Single Pulse Maximum Power Dissipation.

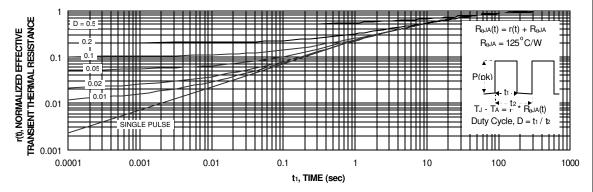


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.

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