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# **FDT3612**

## 100V N-Channel PowerTrench® MOSFET

### **General Description**

This N-Channel MOSFET has been designed specifically to improve the overall efficiency of DC/DC converters using either synchronous or conventional switching PWM controllers.

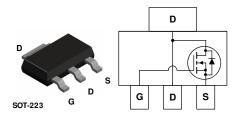
These MOSFETs feature faster switching and lower gate charge than other MOSFETs with comparable  $R_{\rm DS(ON)}$  specifications. The result is a MOSFET that is easy and safer to drive (even at very high frequencies), and DC/DC power supply designs with higher overall efficiency.

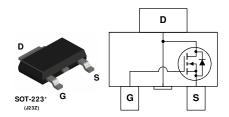
#### **Applications**

- DC/DC converter
- · Motor driving

#### **Features**

- 3.7 A, 100 V.  $R_{DS(ON)} = 120 \ m\Omega \ @\ V_{GS} = 10 \ V$   $R_{DS(ON)} = 130 \ m\Omega \ @\ V_{GS} = 6 \ V$
- · Fast switching speed
- Low gate charge (14nC typ)
- High performance trench technology for extremely low  $R_{\mbox{\scriptsize DS(ON)}}$
- High power and current handling capability in a widely used surface mount package





## Absolute Maximum Ratings T<sub>A</sub>=25°C unless otherwise noted

Symbol	Parameter		Ratings	Units	
V <sub>DSS</sub>	Drain-Source Voltage		100	V	
V <sub>GSS</sub>	Gate-Source Voltage		±20	V	
I <sub>D</sub>	Drain Current - Continuous	(Note 1a)	3.7	A	
	- Pulsed		20		
P <sub>D</sub>	Maximum Power Dissipation	(Note 1a)	3.0	W	
		(Note 1b)	1.3		
		(Note 1c)	1.1		
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction Temperature Range		-55 to +150	°C	

#### **Thermal Characteristics**

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	(Note 1a)	42	°C/W
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	(Note 1)	12	°C/W

#### **Package Marking and Ordering Information**

1 0.01.0.9	9	9			
Device Marking	Device	Reel Size	Tape width	Quantity	
3612	FDT3612	13"	12mm	2500 units	

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Drain-So	urce Avalanche Ratings (Note	2)		ı	I	I
W <sub>DSS</sub>	Drain-Source Avalanche Energy	Single Pulse, $V_{DD} = 50 \text{ V}$ , $I_D = 3.7 \text{ A}$			90	mJ
I <sub>AR</sub>	Drain-Source Avalanche Current				3.7	Α
Off Char	acteristics					
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	100			V
<u>ΔBV<sub>DSS</sub></u> ΔT <sub>J</sub>	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, Referenced to 25°C		106		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 80 \text{ V}, \qquad V_{GS} = 0 \text{ V}$			10	μΑ
I <sub>GSSF</sub>	Gate-Body Leakage, Forward	$V_{GS} = 20 \text{ V}, \qquad V_{DS} = 0 \text{ V}$			100	nA
I <sub>GSSR</sub>	Gate-Body Leakage, Reverse	$V_{GS} = -20 \text{ V},  V_{DS} = 0 \text{ V}$			-100	nA
On Char	acteristics (Note 2)					
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	2	2.5	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, Referenced to 25°C		-6		mV/°C
R <sub>DS(on)</sub>	Static Drain–Source On–Resistance	$\begin{split} &V_{GS} = 10 \text{ V}, &I_{D} = 3.7 \text{ A} \\ &V_{GS} = 6 \text{ V}, &I_{D} = 3.5 \text{ A} \\ &V_{GS} = 10 \text{ V}, I_{D} = 3.7 \text{A}, T_{J} = 125 ^{\circ}\text{C} \end{split}$		88 94 170	120 130 245	mΩ
I <sub>D(on)</sub>	On-State Drain Current	$V_{GS} = 10 \text{ V}, V_{DS} = 10 \text{ V}$	10			Α
g <sub>FS</sub>	Forward Transconductance	$V_{DS} = 10 \text{ V}, \qquad I_{D} = 3.7 \text{ A}$		11		S
Dvnamio	Characteristics			1	1	I
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 50 \text{ V},  V_{GS} = 0 \text{ V},$		632		pF
Coss	Output Capacitance	f = 1.0 MHz		40		pF
C <sub>rss</sub>	Reverse Transfer Capacitance	7		20		pF
Switchin	g Characteristics (Note 2)			ı	ı	ı
t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD} = 50 \text{ V}, \qquad I_D = 1 \text{ A},$		8.5	17	ns
t <sub>r</sub>	Turn-On Rise Time	$V_{GS} = 10 \text{ V}, \qquad R_{GEN} = 6 \Omega$		2	4	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	1		23	37	ns
t <sub>f</sub>	Turn-Off Fall Time	7		4.5	9	ns
Q <sub>g</sub>	Total Gate Charge	$V_{DS} = 50 \text{ V}, \qquad I_{D} = 3.7 \text{ A},$		14	20	nC
Q <sub>gs</sub>	Gate-Source Charge	V <sub>GS</sub> = 10 V		2.4		nC
$Q_{gd}$	Gate-Drain Charge	7		3.8		nC
Drain-Se	ource Diode Characteristics	and Maximum Ratings			•	•
Is	Maximum Continuous Drain-Source				2.5	Α
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V},  I_S = 2.5 \text{ A}$ (Note 2)		0.75	1.2	V

#### Notes

1.  $R_{\theta,JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta,JC}$  is guaranteed by design while  $R_{\theta,CA}$  is determined by the user's board design.



a) 42°C/W when mounted on a 1in² pad of 2 oz copper



b) 95°C/W when mounted on a .0066 in² pad of 2 oz copper



c) 110°C/W when mounted on a minimum pad.

# **Typical Characteristics**

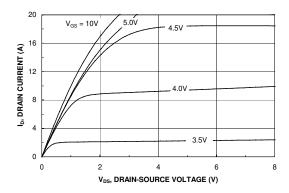


Figure 1. On-Region Characteristics.

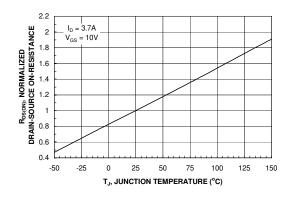


Figure 3. On-Resistance Variation with Temperature.

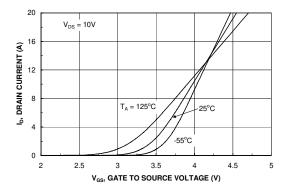


Figure 5. Transfer Characteristics.

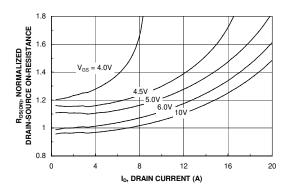


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

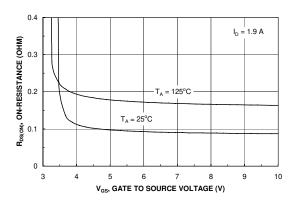


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

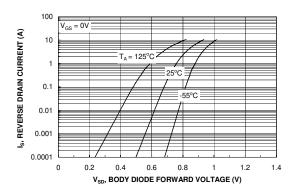
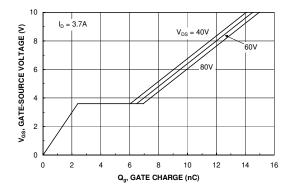


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

## **Typical Characteristics**



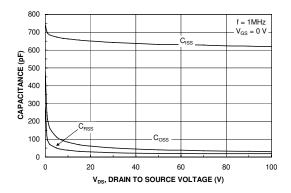


Figure 7. Gate Charge Characteristics.

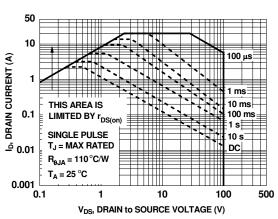


Figure 8. Capacitance Characteristics.

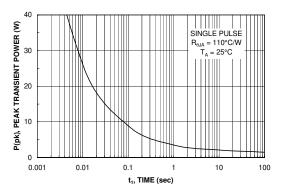


Figure 9. Maximum Safe Operating Area.



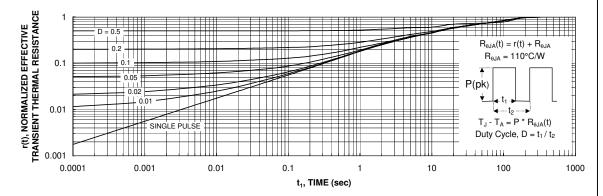
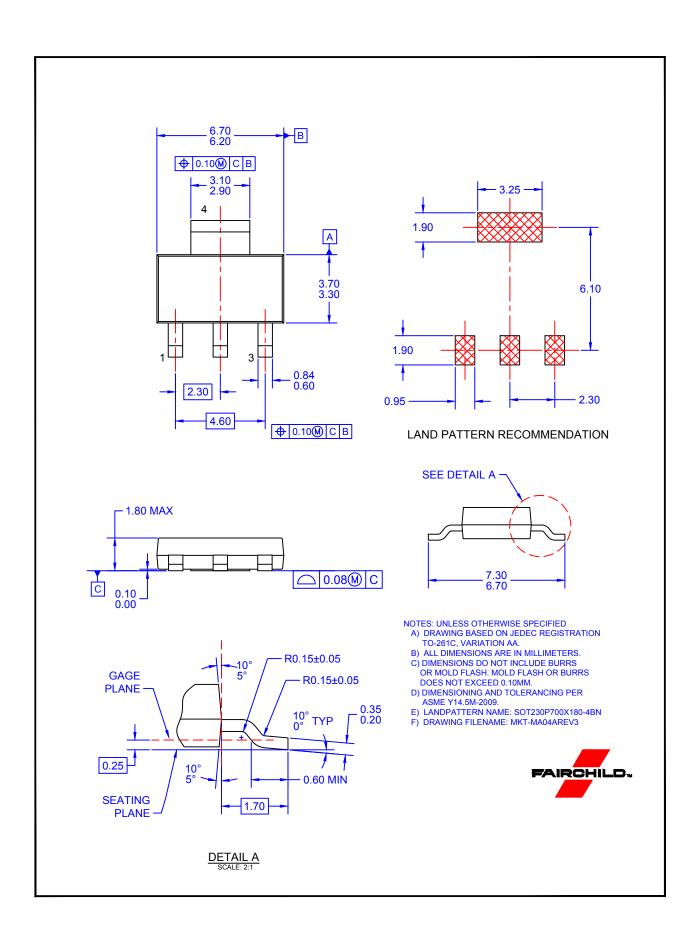


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.



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