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January 2016

# FDT86244

# N-Channel Shielded Gate PowerTrench<sup>®</sup> MOSFET 150 V, 2.8 A, 128 m $\Omega$

#### **Features**

- Shielded Gate MOSFET Technology
- Max  $r_{DS(on)} = 128 \text{ m}\Omega$  at  $V_{GS} = 10 \text{ V}$ ,  $I_D = 2.8 \text{ A}$
- Max  $r_{DS(on)} = 178 \text{ m}\Omega$  at  $V_{GS} = 6 \text{ V}$ ,  $I_D = 2.4 \text{ A}$
- High Performance Trench Technology for Extremely Low r<sub>DS(on)</sub>
- High Power and Current Handling Capability in a Widely Used Surface Mount Package
- Fast Switching Speed
- 100% UIL Tested
- RoHS Compliant



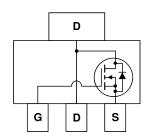
#### **General Description**

This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced PowerTrench<sup>®</sup> process that incorporates Shielded Gate technology. This process has been optimized for  $r_{DS(on)}$ , switching performance and ruggedness.

## **Applications**

- Load Switch
- Primary Switch





### MOSFET Maximum Ratings T<sub>C</sub> = 25 °C unless otherwise noted

Symbol		Parameter		Ratings	Units
$V_{DS}$	Drain to Source Voltage			150	V
$V_{GS}$	Gate to Source Voltage			±20	V
	Drain Current -Continuous	T <sub>A</sub> = 25 °C	(Note 1a)	2.8	^
ID	-Pulsed			12	— A
E <sub>AS</sub>	Single Pulse Avalanche Energy		(Note 3)	12	mJ
В	Power Dissipation	T <sub>A</sub> = 25 °C	(Note 1a)	2.2	W
$P_{D}$	Power Dissipation	T <sub>A</sub> = 25 °C	(Note 1b)	1.0	VV
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Junction T	emperature Range		-55 to +150	°C

#### **Thermal Characteristics**

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	12	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	55	C/VV

#### **Package Marking and Ordering Information**

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
86244	FDT86244	SOT-223	13 "	12 mm	2500 units

## Electrical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Тур	Max	Units
Off Chara	acteristics					
BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	$I_D = 250 \mu A, V_{GS} = 0 V$	150			V
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, referenced to 25 °C		104		mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 120 V, V <sub>GS</sub> = 0 V			1	μΑ
I <sub>GSS</sub>	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$			±100	nA

#### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu A$	2.0	3.1	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D$ = 250 $\mu$ A, referenced to 25 °C		-10		mV/°C
		$V_{GS} = 10 \text{ V}, I_D = 2.8 \text{ A}$		106	128	
r <sub>DS(on)</sub>	Static Drain to Source On Resistance	$V_{GS} = 6 \text{ V}, I_D = 2.4 \text{ A}$		127	178	$m\Omega$
		$V_{GS} = 10 \text{ V}, I_D = 2.8 \text{ A}, T_J = 125 \text{ °C}$		196	237	
9 <sub>FS</sub>	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_{D} = 2.8 \text{ A}$		12		S

#### **Dynamic Characteristics**

C <sub>iss</sub>	Input Capacitance	V 75 V V 0 V	295	395	pF
Coss	Output Capacitance	V <sub>DS</sub> = 75 V, V <sub>GS</sub> = 0 V, f = 1 MHz	33	45	pF
C <sub>rss</sub>	Reverse Transfer Capacitance	1 = 1 101112	2.4	5	pF
$R_g$	Gate Resistance		1.0		Ω

# **Switching Characteristics**

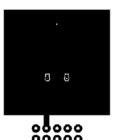
$t_{d(on)}$	Turn-On Delay Time		5.3	11	ns
t <sub>r</sub>	Rise Time	$V_{DD} = 75 \text{ V}, I_D = 2.8 \text{ A},$	1.3	10	ns
t <sub>d(off)</sub>	Turn-Off Delay Time	$V_{GS} = 10 \text{ V}, R_{GEN} = 6 \Omega$	9.8	20	ns
t <sub>f</sub>	Fall Time		2.4	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V <sub>GS</sub> = 0 V to 10 V	4.9	7	nC
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0 \text{ V to 5 V}$ $V_{DD} = 75 \text{ V},$ $I_{D} = 2.8 \text{ A}$	2.8	4	nC
Q <sub>gs</sub>	Total Gate Charge	I <sub>D</sub> = 2.0 A	1.4		nC
$Q_{gd}$	Gate to Drain "Miller" Charge		1.3		nC

#### **Drain-Source Diode Characteristics**

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_S = 2.8 \text{ A}$ (Note 2)	0.82	1.3	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>E</sub> = 2.8 A. di/dt = 100 A/μs	48	77	ns
$Q_{rr}$	Reverse Recovery Charge	iF = 2.6 A, αί/αι = 100 A/μs	44	70	nC

#### NOTES

<sup>1.</sup>  $R_{\theta JA}$  is determined with the device mounted on a 1 in 2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a) 55 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b) 118 °C/W when mounted on a minimum pad of 2 oz copper

<sup>2.</sup> Pulse Test: Pulse Width < 300  $\mu\text{s},$  Duty cycle < 2.0%.

<sup>3.</sup> Starting T  $_{J}$  = 25 °C; N-ch: L = 1 mH, I  $_{AS}$  = 5 A, V  $_{DD}$  = 135 V, V  $_{GS}$  = 10 V.

# Typical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted

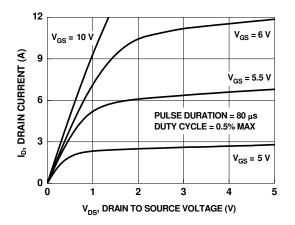


Figure 1. On Region Characteristics

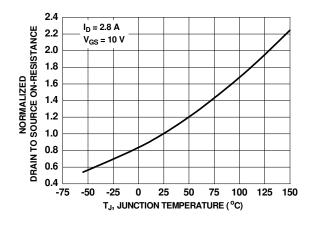


Figure 3. Normalized On Resistance vs Junction Temperature

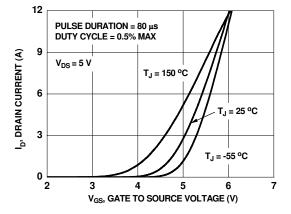


Figure 5. Transfer Characteristics

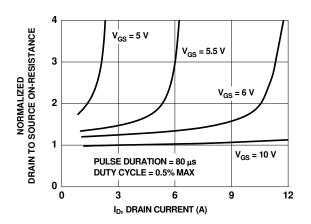


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

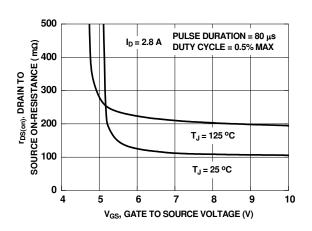


Figure 4. On-Resistance vs Gate to Source Voltage

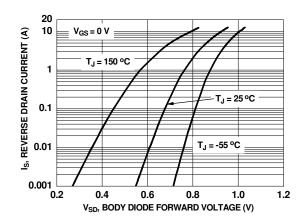


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

# **Typical Characteristics** $T_J = 25$ °C unless otherwise noted

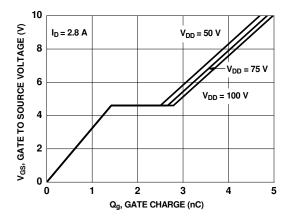


Figure 7. Gate Charge Characteristics

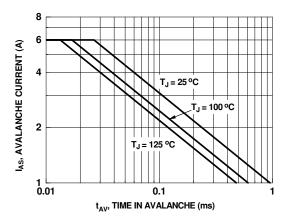


Figure 9. Unclamped Inductive Switching Capability

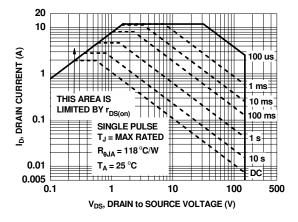


Figure 11. Forward Bias Safe Operating Area

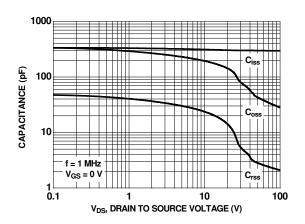


Figure 8. Capacitance vs Drain to Source Voltage

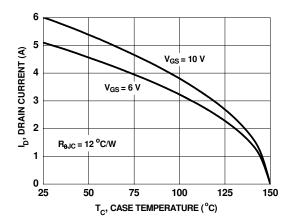


Figure 10. Maximum Continuous Drain Current vs Case Temperature

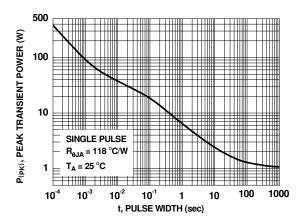


Figure 12. Single Pulse Maximum Power Dissipation

# Typical Characteristics T<sub>J</sub> = 25 °C unless otherwise noted

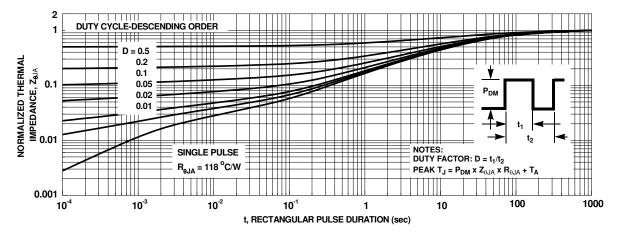
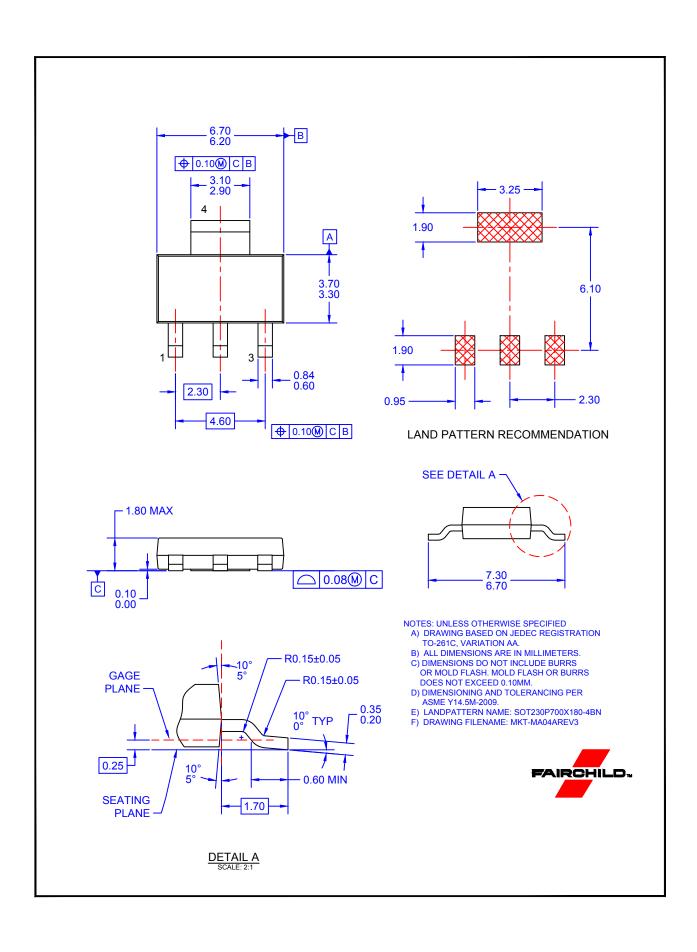


Figure 13. Junction-to-Ambient Transient Thermal Response Curve



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