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# FDW2507NZ

## Common Drain N-Channel 2.5V specified PowerTrench® MOSFET

### General Description

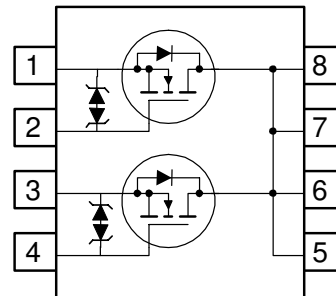
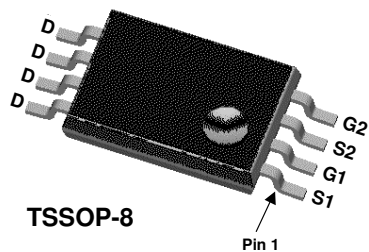
This monolithic common drain N-Channel MOSFET has been designed using Fairchild Semiconductor's advanced PowerTrench process to optimize the  $R_{DS(ON)}$  @  $V_{GS} = 2.5V$  on special TSSOP-8 lead frame with all the drains on one side of the package.

### Applications

- Li-Ion Battery Pack

### Features

- 7.5 A, 20 V  $R_{DS(ON)} = 19\text{ m}\Omega$  @  $V_{GS} = 4.5\text{ V}$   
 $R_{DS(ON)} = 23\text{ m}\Omega$  @  $V_{GS} = 2.5\text{ V}$
- Isolated source and drain pins
- ESD protection diode (note 3)
- High performance trench technology for extremely low  $R_{DS(ON)}$  @  $V_{GS} = 2.5\text{ V}$
- Low profile TSSOP-8 package



### Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
$V_{DSS}$	Drain-Source Voltage	20	V
$V_{GSS}$	Gate-Source Voltage	$\pm 12$	V
$I_D$	Drain Current – Continuous (Note 1a) – Pulsed	7.5	A
		30	
$P_D$	Power Dissipation for Single Operation (Note 1a) (Note 1b)	1.6	W
		1.1	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1a)	77	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1b)	114	$^\circ\text{C/W}$

### Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape width	Quantity
2507NZ	FDW2507NZ	13"	12mm	3000 units

**Electrical Characteristics** $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		-13		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{ V}, V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSSF}$	Gate–Body Leakage, Forward	$V_{GS} = 12\text{ V}, V_{DS} = 0\text{ V}$			10	$\mu\text{A}$
$I_{GSSR}$	Gate–Body Leakage, Reverse	$V_{GS} = -12\text{ V}, V_{DS} = 0\text{ V}$			-10	$\mu\text{A}$

**On Characteristics** (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.6	0.8	1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$		4		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = 4.5\text{ V}, I_D = 7.5\text{ A}$ $V_{GS} = 2.5\text{ V}, I_D = 6.8\text{ A}$ $V_{GS} = 4.5\text{ V}, I_D = 7.5\text{ A}, T_J = 125^\circ\text{C}$		15 17 20	19 23 27	m $\Omega$
$I_{D(on)}$	On–State Drain Current	$V_{GS} = 4.5\text{ V}, V_{DS} = 5\text{ V}$	30			A
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 7.5\text{ A}$		31		S

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		2152		pF
$C_{oss}$	Output Capacitance			512		pF
$C_{riss}$	Reverse Transfer Capacitance			263		pF

**Switching Characteristics** (Note 2)

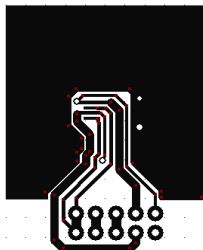
$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 10\text{ V}, I_D = 1\text{ A},$ $V_{GS} = 4.5\text{ V}, R_{GEN} = 6\ \Omega$		12	22	ns
$t_r$	Turn–On Rise Time			13	23	ns
$t_{d(off)}$	Turn–Off Delay Time			35	56	ns
$t_f$	Turn–Off Fall Time			19	34	ns
$Q_g$	Total Gate Charge	$V_{DS} = 10\text{ V}, I_D = 7.5\text{ A},$ $V_{GS} = 4.5\text{ V}$		20	28	nC
$Q_{gs}$	Gate–Source Charge			3		nC
$Q_{gd}$	Gate–Drain Charge			5		nC

**Drain–Source Diode Characteristics and Maximum Ratings**

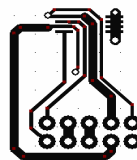
$I_S$	Maximum Continuous Drain–Source Diode Forward Current			1.3		A
$V_{SD}$	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 1.3\text{ A}$ (Note 2)		0.6	1.2	V
$t_{rr}$	Diode Reverse Recovery Time	$I_F = 7.5\text{ A}$		26		nS
$Q_{rr}$	Diode Reverse Recovery Charge	$dI_F/dt = 100\text{ A}/\mu\text{s}$ (Note 2)		21		nC

**Notes:**

1.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



- a)  $77^\circ\text{C}/\text{W}$  when mounted on a  $1\text{ in}^2$  pad of 2 oz copper



- b)  $114^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width <  $300\ \mu\text{s}$ , Duty Cycle < 2.0%

3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

### Typical Characteristics

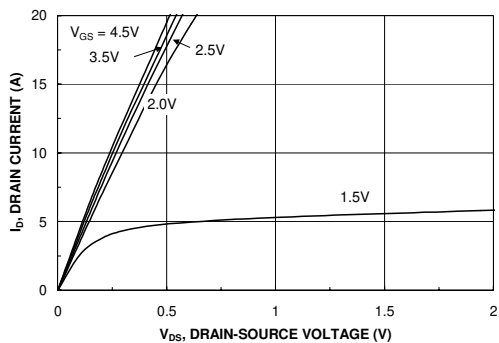


Figure 1. On-Region Characteristics.

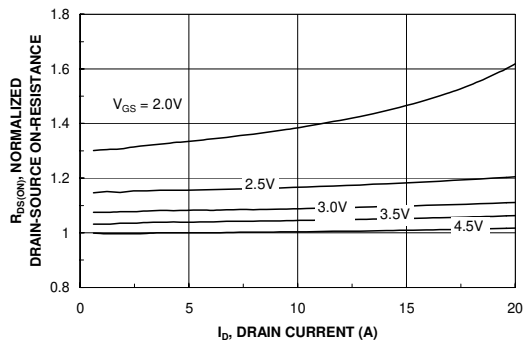


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage.

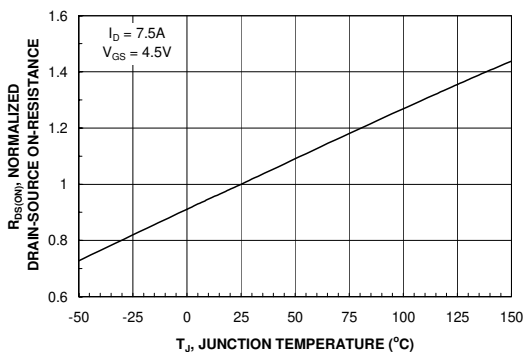


Figure 3. On-Resistance Variation with Temperature.

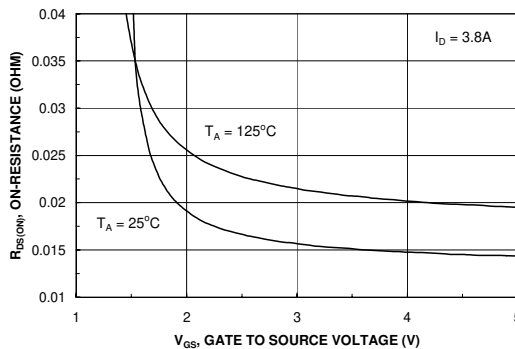


Figure 4. On-Resistance Variation with Gate-to-Source Voltage.

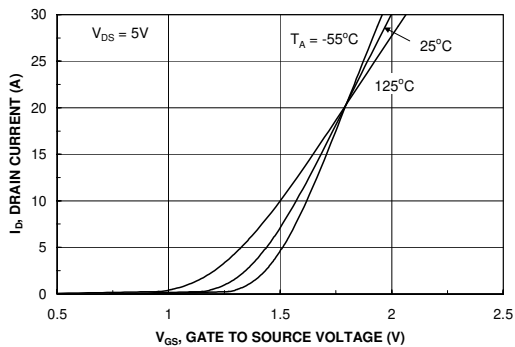


Figure 5. Transfer Characteristics.

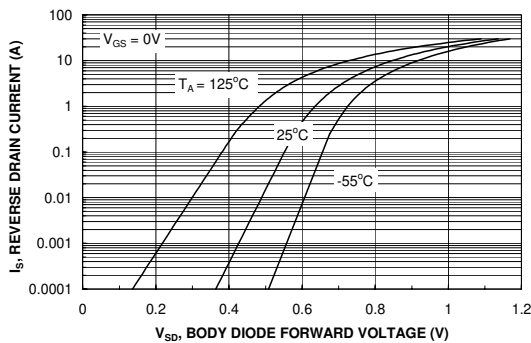


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature.

### Typical Characteristics

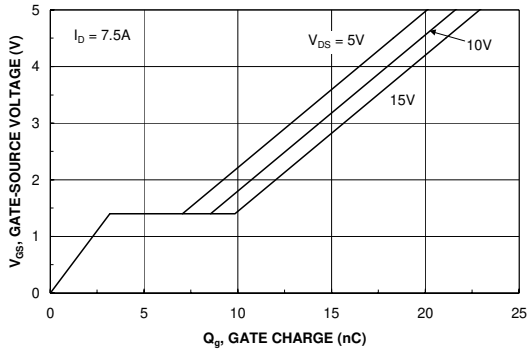


Figure 7. Gate Charge Characteristics.

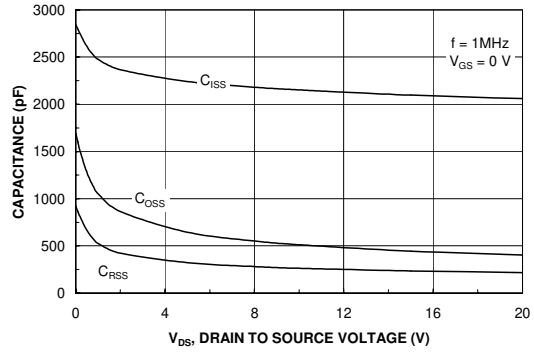


Figure 8. Capacitance Characteristics.

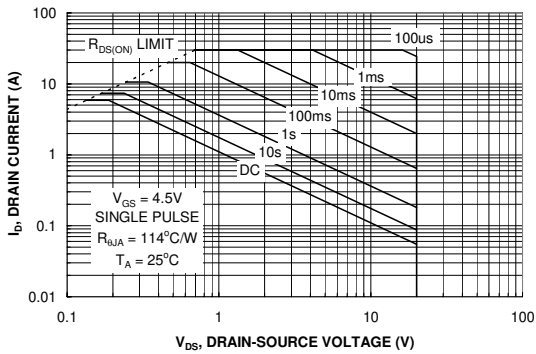


Figure 9. Maximum Safe Operating Area.

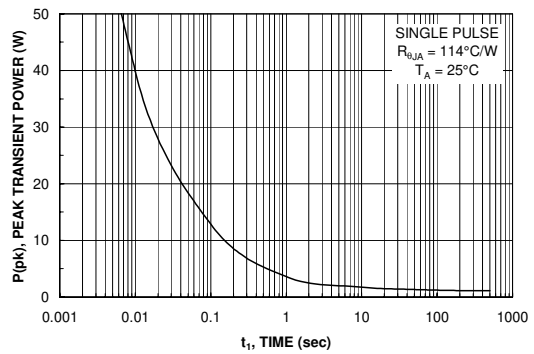


Figure 10. Single Pulse Maximum Power Dissipation.

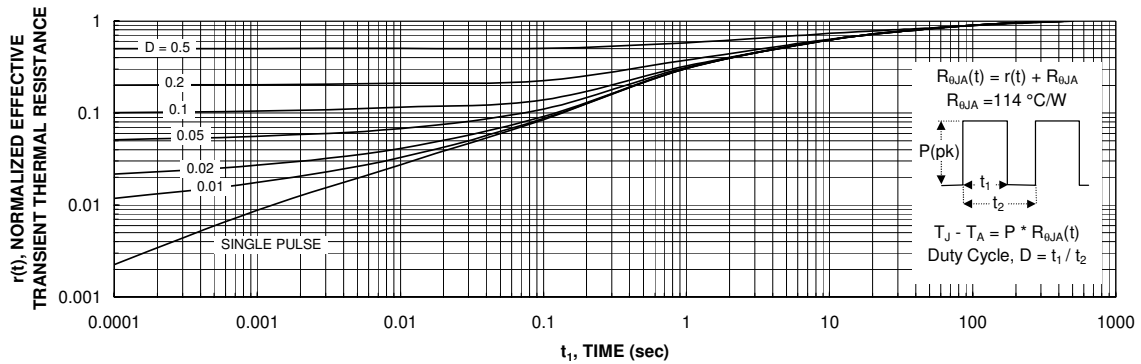


Figure 11. Transient Thermal Response Curve.

Thermal characterization performed using the conditions described in Note 1b. Transient thermal response will change depending on the circuit board design.

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