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FAIRCHILD SEMICONDUCTOR®

June 2007

# FDZ2554P

## Monolithic Common Drain P-Channel 2.5V Specified Power Trench® BGA MOSFET -20V, -6.5A, 28mΩ

### Features

- Max $r_{DS(on)}$ = 28mΩ at $V_{GS}$ = -4.5V, $I_D$ = -6.5A
- Max $r_{DS(on)}$ = 45mΩ at $V_{GS}$ = -2.5V, $I_D$ = -5A
- Occupies only 0.10 $cm^2$ of PCB area: 1/3 the area of SO-8
- Ultra-thin package: less than 0.80 mm height when mounted to PCB
- Outstanding thermal transfer characteristics: significantly better than SO-8
- Ultra-low Qg x $r_{DS(on)}$ figure-of-merit
- High power and current handling capability
- RoHS Compliant

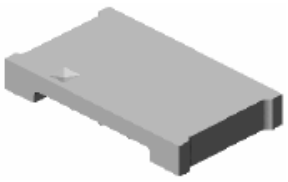
### General Description

Combining Fairchild's advanced 2.5V specified PowerTrench process with state-of-the-art BGA packaging, the FDZ2554P minimizes both PCB space and $r_{DS(on)}$. This monolithic common drain BGA MOSFET embodies a breakthrough in packaging technology which enables the device to combine excellent thermal transfer characteristics, high current handling capability, ultra-low profile packaging, low gate charge, and low $r_{DS(on)}$.

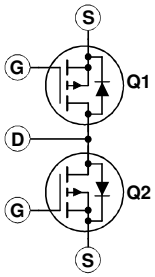
### Applications

- Battery management
- Load Switch
- Battery protection

Bottom



Top




## MOSFET Maximum Ratings $T_A$ = 25°C unless otherwise noted

| Symbol | Parameter | | Ratings | Units |
|---|---|---|---|---|
| $V_{DS}$ | Drain to Source Voltage | | -20 | V |
| $V_{GS}$ | Gate to Source Voltage | | ±12 | V |
| $I_D$ | Drain Current -Continuous | (Note 1a) | -6.5 | A |
| | -Pulsed | | -20 | |
| $P_D$ | Power Dissipation (Steady State) | (Note 1a) | 2.1 | W |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | -55 to +150 | °C |

### Thermal Characteristics

| | | | | |
|---|---|---|---|---|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case | (Note 1) | 0.6 | °C/W |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | (Note 1a) | 60 | |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient | (Note 1b) | 108 | |
| $R_{\theta JB}$ | Thermal Resistance, Junction to Ball | (Note 1) | 6.3 | |

### Package Marking and Ordering Information

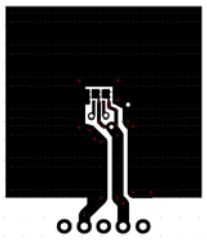
| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|
| 2554P | FDZ2554P | BGA 2.5X4.0 | 7" | 12 mm | 3000 units |

## Electrical Characteristics $T_J$= 25°C unless otherwise noted

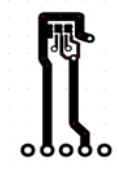
| Symbol | Parameter | Test Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Off Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain to Source Breakdown Voltage | $I_D$ = -250μA, $V_{GS}$ = 0V | -20 | | | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = -250μA, referenced to 25°C | | -13 | | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = -16V, $V_{GS}$ = 0V | | | -1 | μA |
| $I_{GSS}$ | Gate to Source Leakage Current | $V_{GS}$ = ±12V, $V_{DS}$ = 0V | | | ±100 | nA |
| **On Characteristics** | | | | | | |
| $V_{GS(th)}$ | Gate to Source Threshold Voltage | $V_{GS}$ = $V_{DS}$, $I_D$ = -250μA | -0.6 | -0.8 | -1.5 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate to Source Threshold Voltage Temperature Coefficient | $I_D$ = -250μA, referenced to 25°C | | 3 | | mV/°C |
| $r_{DS(on)}$ | Static Drain to Source On Resistance | $V_{GS}$ = -4.5V, $I_D$ = -6.5A | | 21 | 28 | mΩ |
| | | $V_{GS}$ = -2.5V, $I_D$ = -5A | | 36 | 45 | |
| | | $V_{GS}$ = -4.5V, $I_D$ = -6.5A, $T_J$ = 125°C | | 30 | 43 | |
| $g_{FS}$ | Forward Transconductance | $V_{DD}$ = -5V, $I_D$ = -6.5A | | 24 | | S |
| **Dynamic Characteristics** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = -10V, $V_{GS}$ = 0V, f = 1MHz | | 1430 | 1900 | pF |
| $C_{oss}$ | Output Capacitance | | | 319 | 425 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 164 | 245 | pF |
| $R_g$ | Gate Resistance | $V_{GS}$ = 15mV, f = 1MHz | | 9.2 | | Ω |
| **Switching Characteristics** | | | | | | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = -10V, $I_D$ =-1A, $V_{GS}$ = -4.5V, $R_{GEN}$ = 6Ω | | 12 | 22 | ns |
| $t_r$ | Rise Time | | | 9 | 18 | ns |
| $t_{d(off)}$ | Turn-Off Delay Time | | | 62 | 100 | ns |
| $t_f$ | Fall Time | | | 37 | 60 | ns |
| $Q_g$ | Total Gate Charge | $V_{GS}$ = -4.5V , $V_{DD}$ =-10V $I_D$ = -6.5A | | 14 | 20 | nC |
| $Q_{gs}$ | Gate to Source Charge | | | 3 | | nC |
| $Q_{gd}$ | Gate to Drain “Miller” Charge | | | 4 | | nC |
| **Drain-Source Diode Characteristics** | | | | | | |
| $I_S$ | Maximum Continuous Drain-Source Diode Forward Current | | | | -1.75 | A |
| $V_{SD}$ | Source to Drain Diode Forward Voltage | $V_{GS}$ = 0V, $I_S$ = -1.75A (Note 2) | | -0.7 | -1.2 | V |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = -6.5A, di/dt = 100A/μs | | 25 | 40 | ns |
| $Q_{rr}$ | Reverse Recovery Charge | | | 20 | 32 | nC |

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 $in^2$ oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. The thermal resistance from the junction to the circuit board side of the solder ball, $R_{\theta JB}$, is defined for reference. For $R_{\theta JC}$, the thermal reference point for the case is defined as the top surface of the copper chip carrier. $R_{\theta JC}$ and $R_{\theta JB}$ are guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a. 60°C/W when mounted on a 1 $in^2$ pad of 2 oz copper.



b. 108 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300μs, Duty cycle < 2.0%.

## Typical Characteristics $T_J$ = 25°C unless otherwise noted

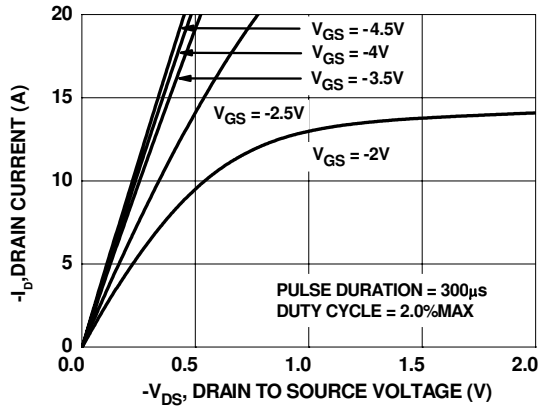



**Figure 1. On-Region Characteristics**

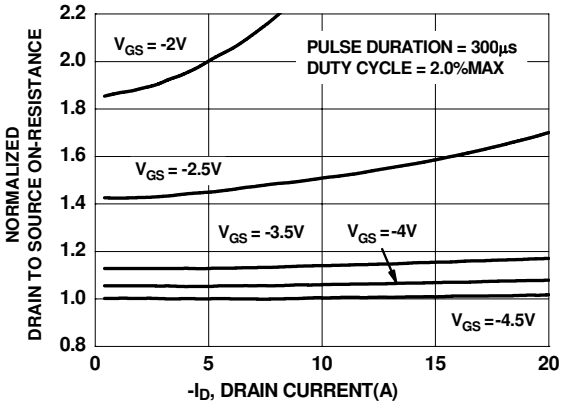



**Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage**

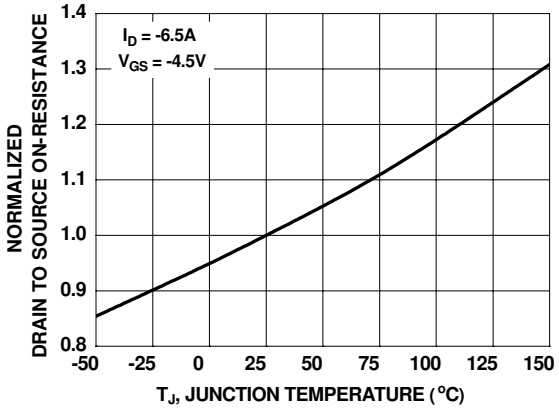



**Figure 3. Normalized On-Resistance vs Junction Temperature**

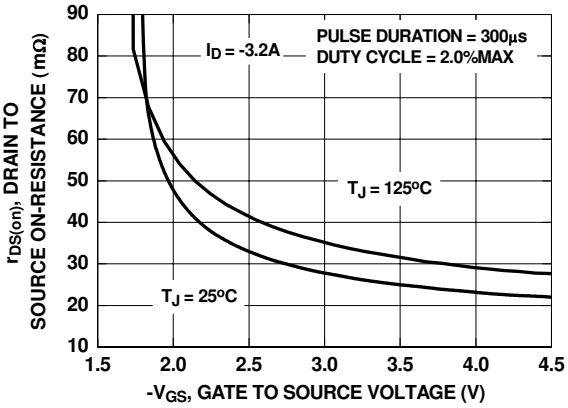



**Figure 4. On-Resistance vs Gate to Source Voltage**

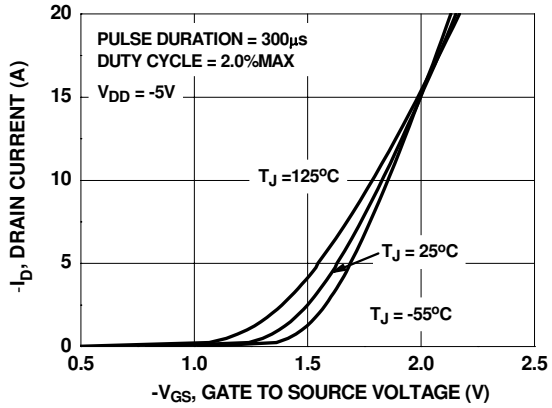



**Figure 5. Transfer Characteristics**

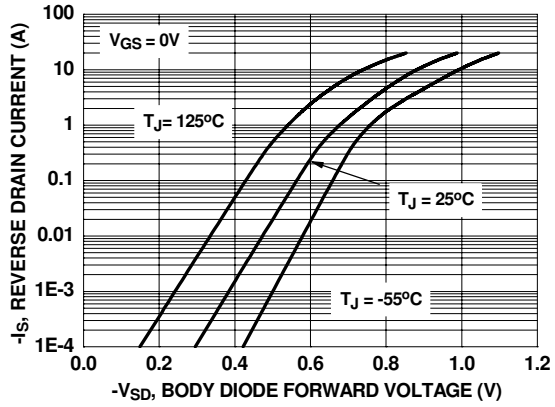



**Figure 6. Source to Drain Diode Forward Voltage vs Source Current**

## Typical Characteristics $T_J$ = 25°C unless otherwise noted

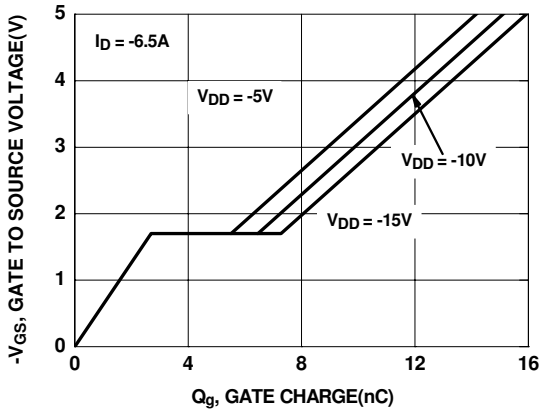



**Figure 7. Gate Charge Characteristics**

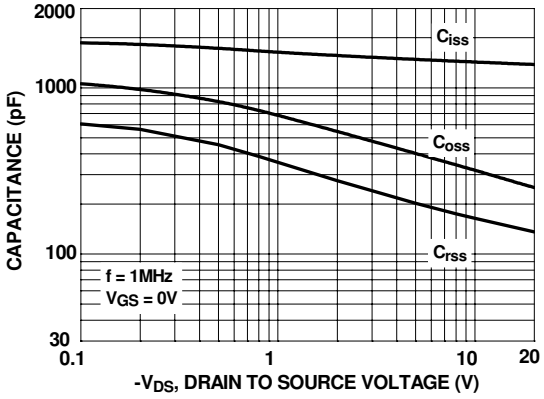



**Figure 8. Capacitance vs Drain to Source Voltage**

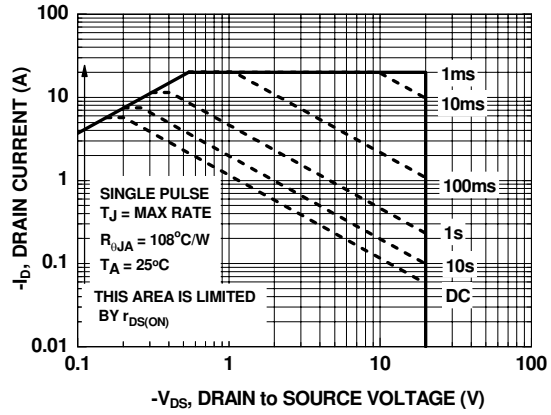



**Figure 9. Forward Bias Safe Operating Area**

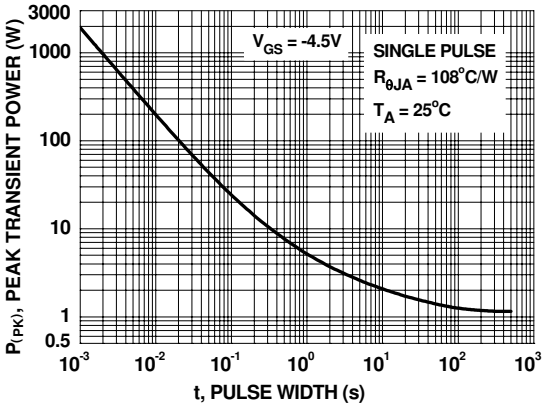



**Figure 10. Single Pulse Maximum Power Dissipation**

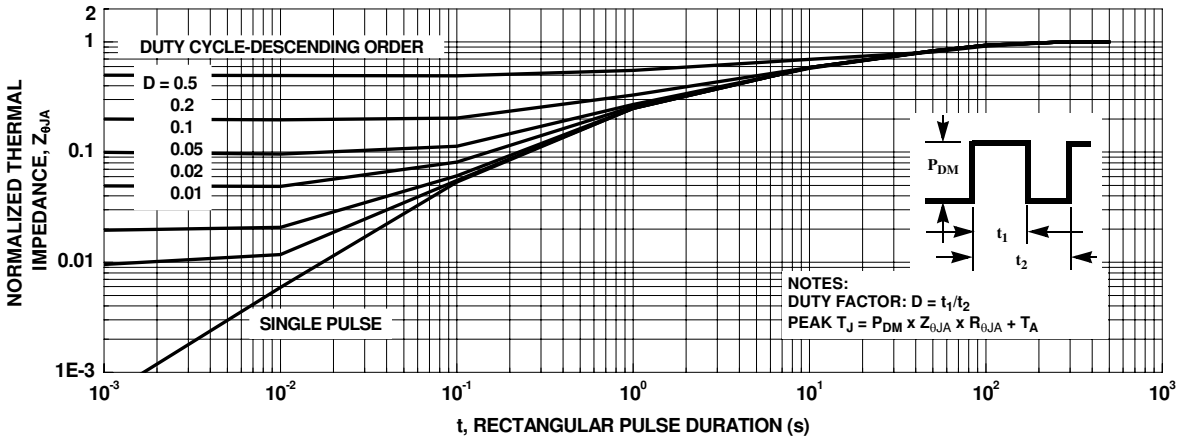
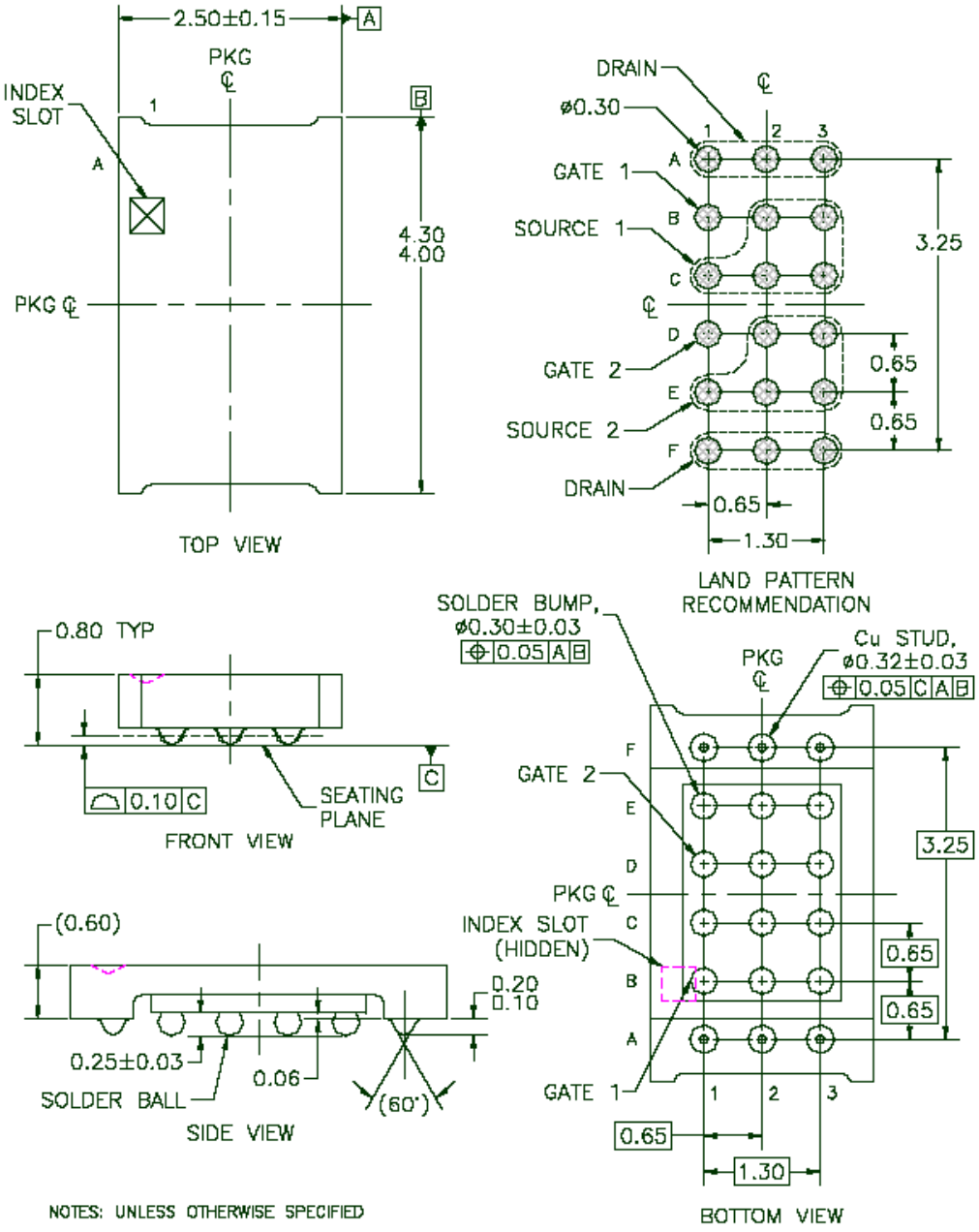



**Figure 11. Transient Thermal Response Curve**

## Dimensional Outline and Pad Layout




NOTES: UNLESS OTHERWISE SPECIFIED

A) ALL DIMENSIONS ARE IN MILLIMETERS.
B) NO JEDEC REGISTRATION REFERENCE AS OF JULY 1999.
C) BALL CONFIGURATION TABLE

| TERMINAL | DESIGNATION |
|---|---|
| A1,A2,A3,F1,F2,F3 | DRAIN |
| B1 | GATE 1 |
| B2,B3,C1,C2,C3 | SOURCE 1 |
| D1 | GATE 2 |
| D2,D3,E1,E2,E3 | SOURCE 2 |

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