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User Guide for

FEBFAN7688_I00250A Evaluation Board

FAN7688, LLC Resonant, 250 W, 400 V to 12.5 V Converter, Evaluation Board

Featured Fairchild Products:

FAN7688

FAN3225C

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Table of Contents

The following user guide supports the FEBFAN7688_I00250A, FAN7688, 250 W, and 400 V to 12.5 V Evaluation Board (EVB). It should be used in conjunction with the FAN7688 datasheet, and FAN7688 Excel®-based Design Tool.

1. Introduction

This document describes the use and performance of the FAN7688, 250 W, and 400 V to 12.5 V EVB. The input voltage range is 300 V_{DC}<V_{IN}<450V_{DC} and the output is a 12.5 V, regulated over an output current range of 0 A<I_{OUT}<20 A. The EVB allows ease of probing by making available numerous test points and options for installing current loops. Although the input voltage range is typical of the output voltage from a PFC boost power stage, the end application of this EVB is considered general purpose for the use of testing the many features of the FAN7688 LLC resonant controller. This document contains a general description of the FAN7688 LLC resonant controller, EVB specification, power-on and off procedure, schematic, Bill of Materials (BOM), and typical EVB performance characteristics.

1.1. General Description of FAN7688

The FAN7688 is a secondary-side, LLC resonant, Pulse Frequency Modulated (PFM) controller with dedicated Synchronous Rectification (SR) gate drive, offering best in class efficiency for isolated DC/DC converters. The primary resonant current is sensed and integrated to employ a type of peak current mode control known as charge control. The integrated resonant current is combined with a triangular waveform generated from an internal oscillator to determine the switching frequency. This provides a better control-to-output transfer function of the power stage making the feedback loop design easy and allows true input power limit capability. The FAN7688 also incorporates a closed loop soft-start function that uses an adaptive soft-start current to prevent saturation of the error amplifier which allows monotonic startup of the output voltage independent of load current. A dual edge tracking, adaptive SR drive technique minimizes body-diode conduction of the SR MOSFETs thereby maximizing overall efficiency.

1.2. FAN7688 Internal Block Diagram

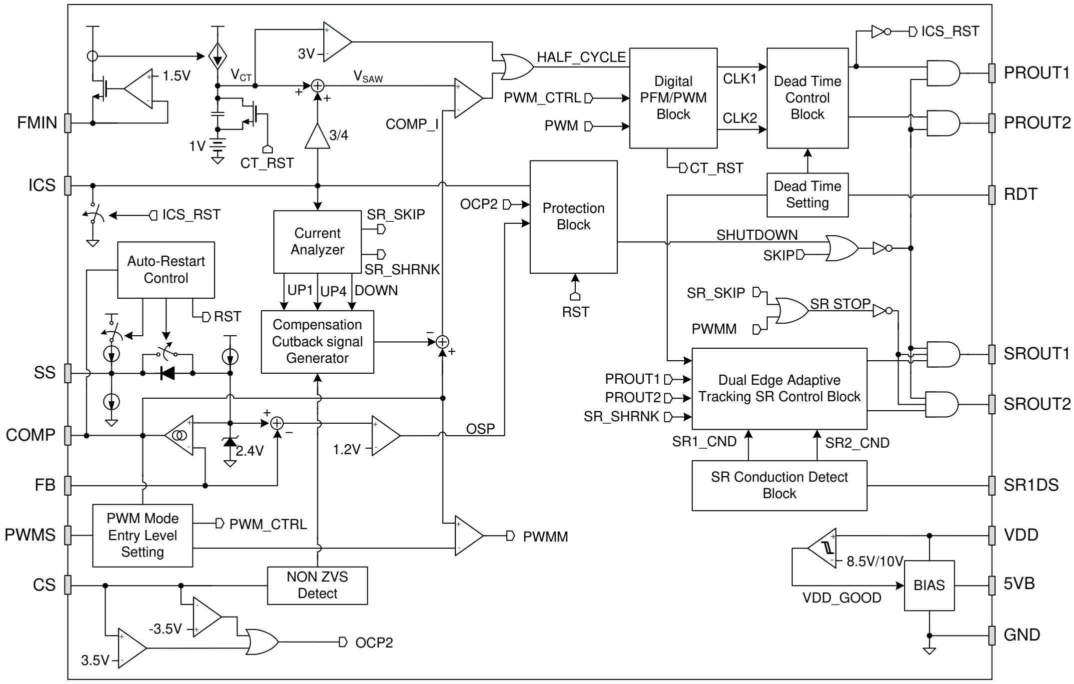


Figure 1. FAN7688 Internal Block Diagram

1.3. FAN7688 Controller Features

The FAN7688 is a secondary side controller designed to modulate the frequency to control a DC to DC isolated LLC converter. Secondary side control offers several unique advantages over primary side control. Direct sensing of the SR drain is necessary for accurate SR timing optimization and better SR reliability under all operating conditions. The output voltage is also directly sensed by the controller which allows accurate closed loop soft-start, direct interface to the load and output short circuit overload protection during startup. And since no optocoupler is required, there is no variation in loop gain due to the variation in optocoupler Current Transfer Ration (CTR).

The FAN7688 uses a hybrid control scheme where, depending upon line or load conditions (COMP voltage), operation can occur using either fixed frequency PWM mode or traditional PFM mode. PFM mode commands highest switching frequency during light load and startup. High frequency switching losses are dominant during light load. Light load efficiency is therefore improved when the power stage is controlled using fixed frequency, PWM mode. The transition between PWM and PFM is seamless and can be programmed as a function of load current via the PWMS pin. This allows custom efficiency tailoring around a particular light load efficiency point of interest.

Further light load efficiency improvements can be realized by disabling SR switching at a particular minimum load point. The FAN7688 SR_SKIP function is programmable through the ICS pin. When the peak value of the integrated current sense is less than the SR_SKIP enable threshold, SR switching is disabled. Whenever the SRs are disabled, load current will flow through the SR body diodes or parallel Schottky rectifiers can be used as an option for even higher light load efficiency.

A comprehensive set of auto-restart protection functions includes: pulse-by-pulse Over-Current Protection (OCP), Output Short Protection (OSP), non-Zero Voltage Switching (ZVS) Protection (NZP), Overload Protection (OLP) and Over-Temperature Protection (OTP). Capacitive region operation can be detrimental to an LLC converter. During light load PFM mode, the frequency decreases as the voltage gain is increasing to maintain output regulation. Inevitably, operation deep below resonance occurs where, at some minimum frequency, the maximum peak gain is obtained, pushing the converter into the capacitive region. Loss of ZVS, DC gain inversion and body diode reverse recovery are some of the problems associated with capacitive region operation. The FAN7688 FMIN pin allows the minimum frequency to be programmed. By setting a stop before the absolute maximum gain is obtained, capacitive region operation can easily be prevented.

2. Overview of the Evaluation Board

The FEBFAN7688_I00250A EVB uses a four-layer Printed Circuit Board (PCB) designed for 250 W (12.5 V / 20 A) rated power. The EVB dimensions are 163 mm x 89 mm x 25 mm (LxWxH). The maximum rated power is designed for 250 W but the maximum power limit is set to 375 W. The EVB is a DC to DC converter and operates from a 400 V input, typical of the voltage produced from an off-line PFC boost converter. The output voltage is set to regulate at 12.5 V. An input bulk capacitor, C1, is included but in the case of operating from a PFC output, C1 would be redundant since the PFC output would include a similar size bulk capacitor necessary for hold up. The EVB also requires an external 12 V bias supply voltage for operation. Connections for the DC input voltage, DC output voltage and DC bias supply voltage are made possible through J9, J6, J15 and J16. Remote sense connections (J7, J26) are also available for accurately monitoring output voltage. Control loop measurements can easily be made by injecting a perturbation signal across a 49.9 Ω (R6) resistor through +Loop (J8) and –Loop (J10). Primary resonant current can be measured by removing R4 and soldering a loop of wire (minimum AWG#22) into the plated through holes located on each R4 conductive pad. Similarly, secondary AC current can be measured by removing R5 and soldering a loop of wire (minimum AWG#16) onto the conductive R4 SMD pads. Primary side gate drive can be monitored for the high-side MOSFET (floating) between J5 and the source lead of Q1 and for the low-side MOSFET (GND referenced) between J13 and J17. On the secondary side, the SR MOSFET gate drives can be monitored between J11 and J14 for Q3 and between J12 and J14 for Q4. All 16 pins of the FAN7688 can easily be probed at J18-J36 and there are five secondary side ground pins (J14, J26-7, J35-6). In summary, the EVB allows ease of probing at the signals most important for understanding the FAN7688 operation and allows additional board space for ease of soldering external components or circuit modifications.

2.1. Photographs

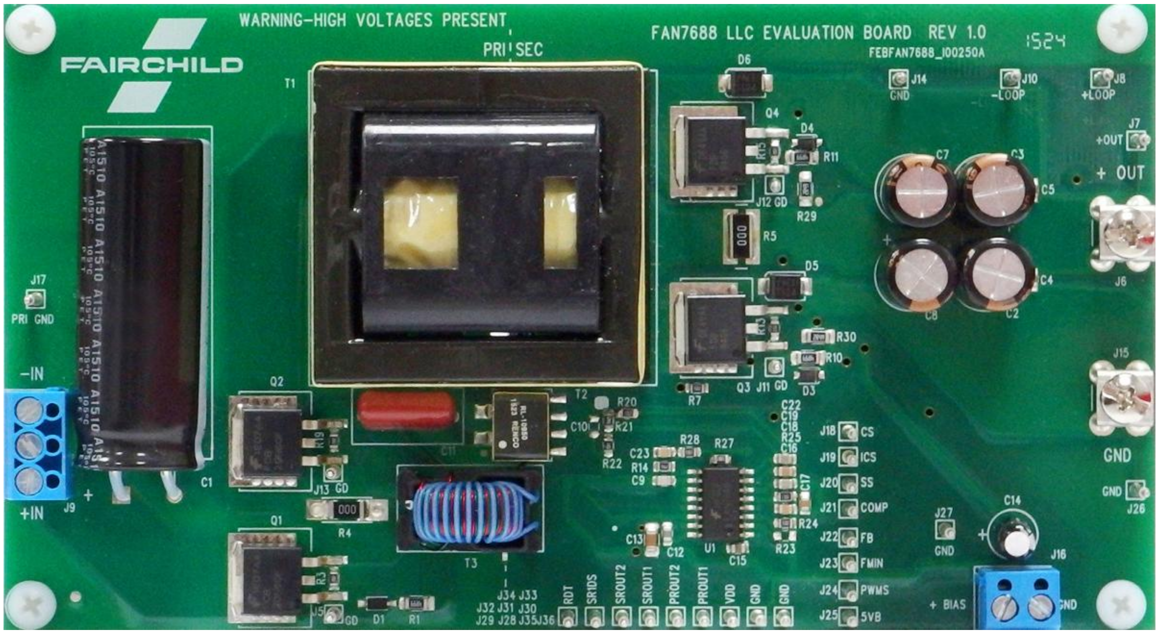


Figure 2. Top View, 163 mm x 89 mm

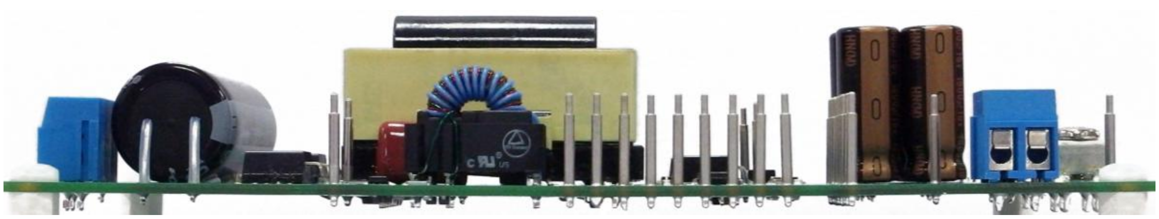


Figure 3. Side View, Cross Section, 30 mm

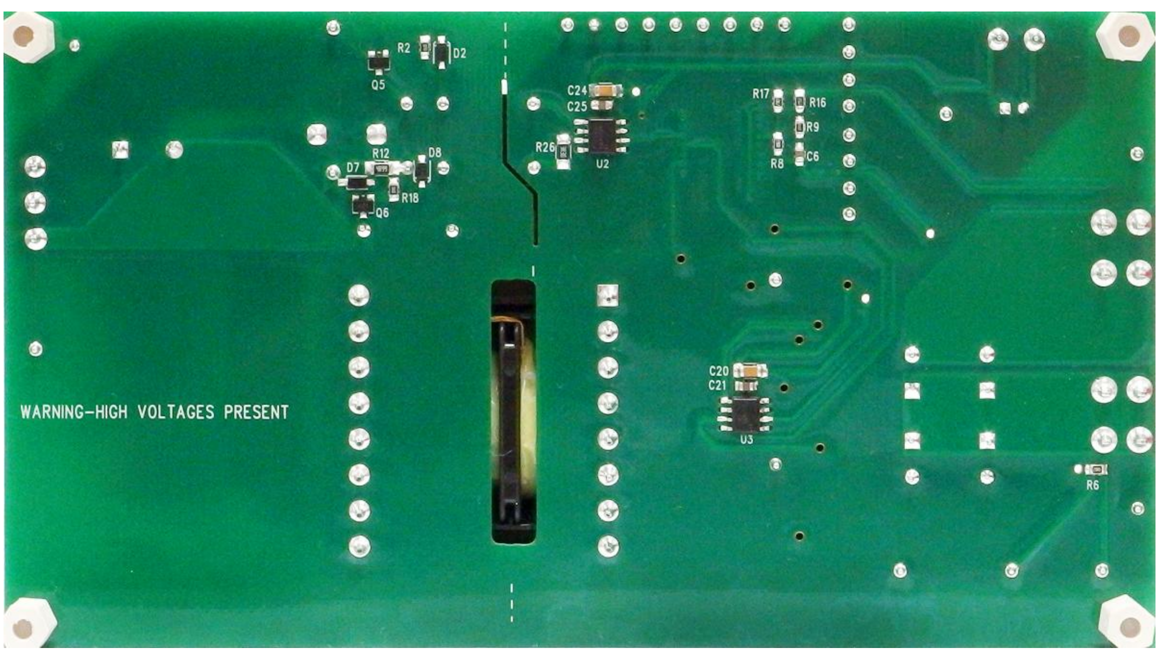


Figure 4. Bottom View, 163 mm x 89 mm

3. Specifications

The evaluation board has been designed and optimized for the conditions in Table 1.

Table 1. Electrical and Mechanical Specifications

Parameter	Min.	Typ.	Max.	Unit
V_{IN}	300	400	450	V_{DC}
V_{OUT}	12.4	12.5	12.6	V_{DC}
I_{OUT}	0		20	A
P_{OUT_MAX}			250	W
F_{RES} V_{IN}=375 V		105		kHz
f_{PWM}		250		kHz
$f_{SW(PFM)}$ 300 V<V_{IN}<450 V	80		140	kHz
SR_{SHRINK} 10% P_{OUT_MAX}		25		W
SR_{ENABLE} 25% P_{OUT_MAX}		60		W
I_{OUT_OCP} Below Res V_{IN}=300 V			22	A
I_{OUT_OCP} Above Res V_{IN}=425 V			30	A
t_{SS} 400 V, 20 A		55	60	ms
t_{HU} 400 V, 20 A	16	75		ms
η_400 V P_{OUT}=50 W 20% P_{OUT_MAX}		95		%
η_400 V P_{OUT}=125 W 50% P_{OUT_MAX}		97		%
η_400V P_{OUT}=250 W 100% P_{OUT_MAX}		96		%
Mechanical and Thermal				
Height			25 mm	
θ_{JC} Use of Fan for I_{OUT}>20 A			80°C	

4. Test Procedure

Before applying power to the FEBFAN7688_I00250A EVB; the DC bias supply voltage, DC source input voltage and DC electronic load should be connected to the board as shown in Figure 5. Optionally a Digital Volt Meter (DVM1) (set to measure DC voltage) can be connected to J7 and J26 to measure the output voltage and a second DVM (DVM2, set to measure ≤2.5 V_{DC}) can be connected across an external current sensing shunt (R_{SHUNT}=100 mΩ) to measure DC output current. Note that most ammeter settings are limited to 10 A_{DC}. Measuring the DC output current using a direct connection into a DVM ammeter can damage the DVM and/or blow the fuse.

4.1. Safety Precautions

The FEBFAN7688_I00250A EVB operates from a high voltage DC supply and the bulk input capacitor stores significant charge. Please be extra careful when probing and handling the module and observe the following safety precautions:

- Start with a clean working surface, clear of any conductive material.
- Never probe or move a probe on the EVB while the DC supply voltage is present.
- Ensure the input and output capacitors are fully discharged before disconnecting the test leads.

Power-On Procedure

1. Connect an electronic load (12.5 V, 0-30 A) to J6 and J15. Set the electronic load to Constant Current (CC) with an initial setting of 0-1A.
2. Connect DVM1to Kelvin connections, J7 and J26.
3. As shown in Figure 5, connect a resistive shunt in series with the electronic load + or electronic load -. If efficiency is not being measured, the shunt can be omitted.
4. Connect DVM2 across the resistive shunt.
5. Connect a 400 V, DC power supply (300~450 V) to J9, pins 1 and 3.
6. Connect an optional power meter between the 400 V, DC power supply and J9. If a power meter is not available, 2 DVMs can also be used to measure input current and input voltage.
7. Connect a 12 V bias DC power supply to J16, pins 1 and 2.
8. Set the input voltage source to 400 V and turn on the input voltage source.
9. Set the electronic load to draw 1 A of CC and turn on the electronic load.
10. Set the 12 V bias DC power supply to 12 V and turn on the bias power supply.
11. Verify the output voltage reading on DVM1 is now 12.5 V.
12. Vary the load current (0~20 A) as desired and verify normal output voltage regulation.
13. **Prolonged operation near or above 20 A requires use of fan.**
14. Vary the input voltage as desired (300 V~450 V) and verify normal output voltage regulation.

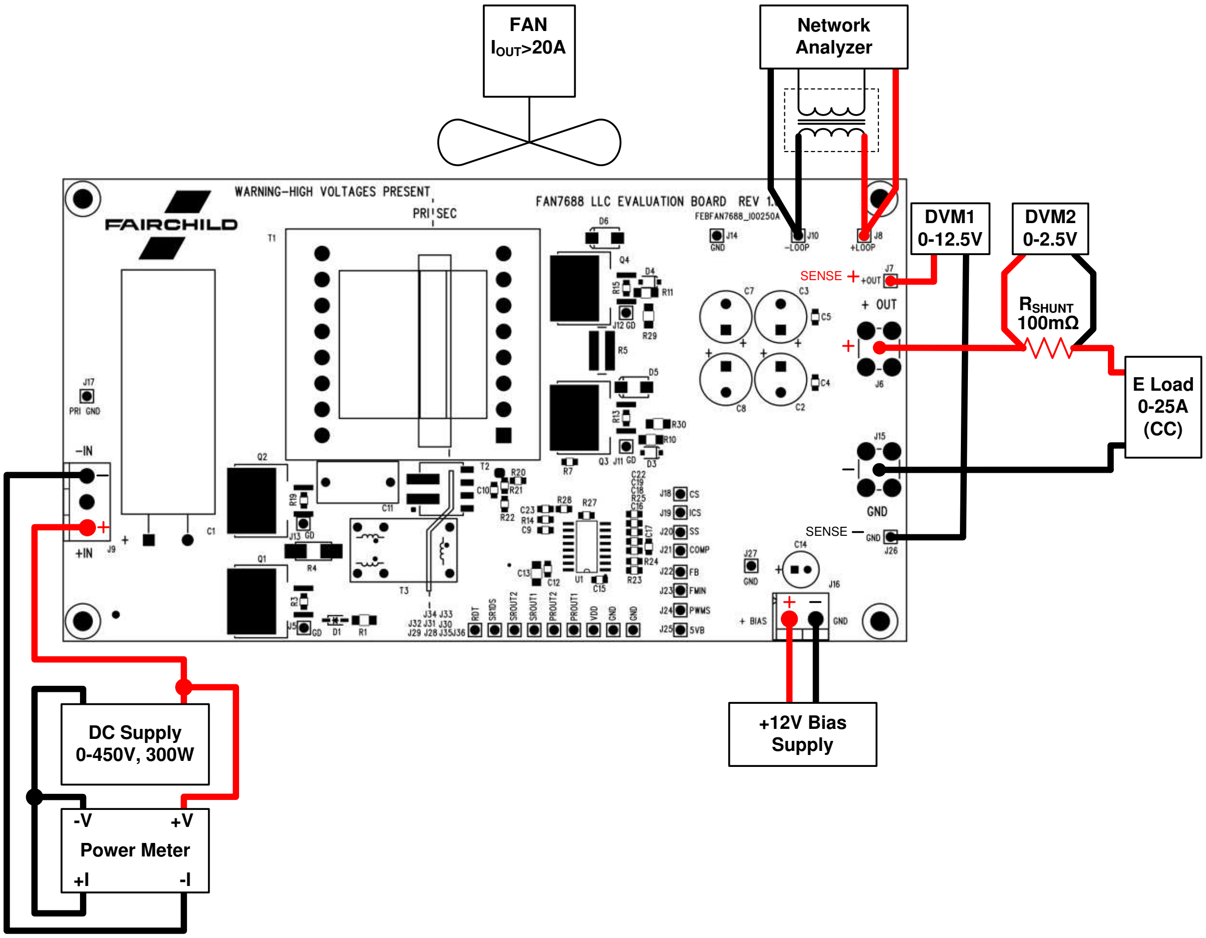


Figure 5. Recommended EVB Test Configuration

All efficiency data shown was taken using the test set up shown in Figure 5.

Power-Off Procedure

1. Make sure the electronic load is ON and set to draw at least 5 A of CC.
2. Disconnect (shutdown) the 400 V DC supply voltage.
3. Disconnect (shutdown) the 12 V bias DC power supply.
4. Disconnect (shutdown) DC electronic load last to ensure the output capacitors are fully discharged before handling the evaluation module.
5. Verify that DVM1 reads 0 V.
6. Verify that the power meter (or DVM measuring input voltage) reads 0 V. If not, wait until the input capacitor (C1) is fully discharged or manually discharge C1 using an appropriate sized low value (~200 Ω) power resistor (>10 W).

5. Schematic

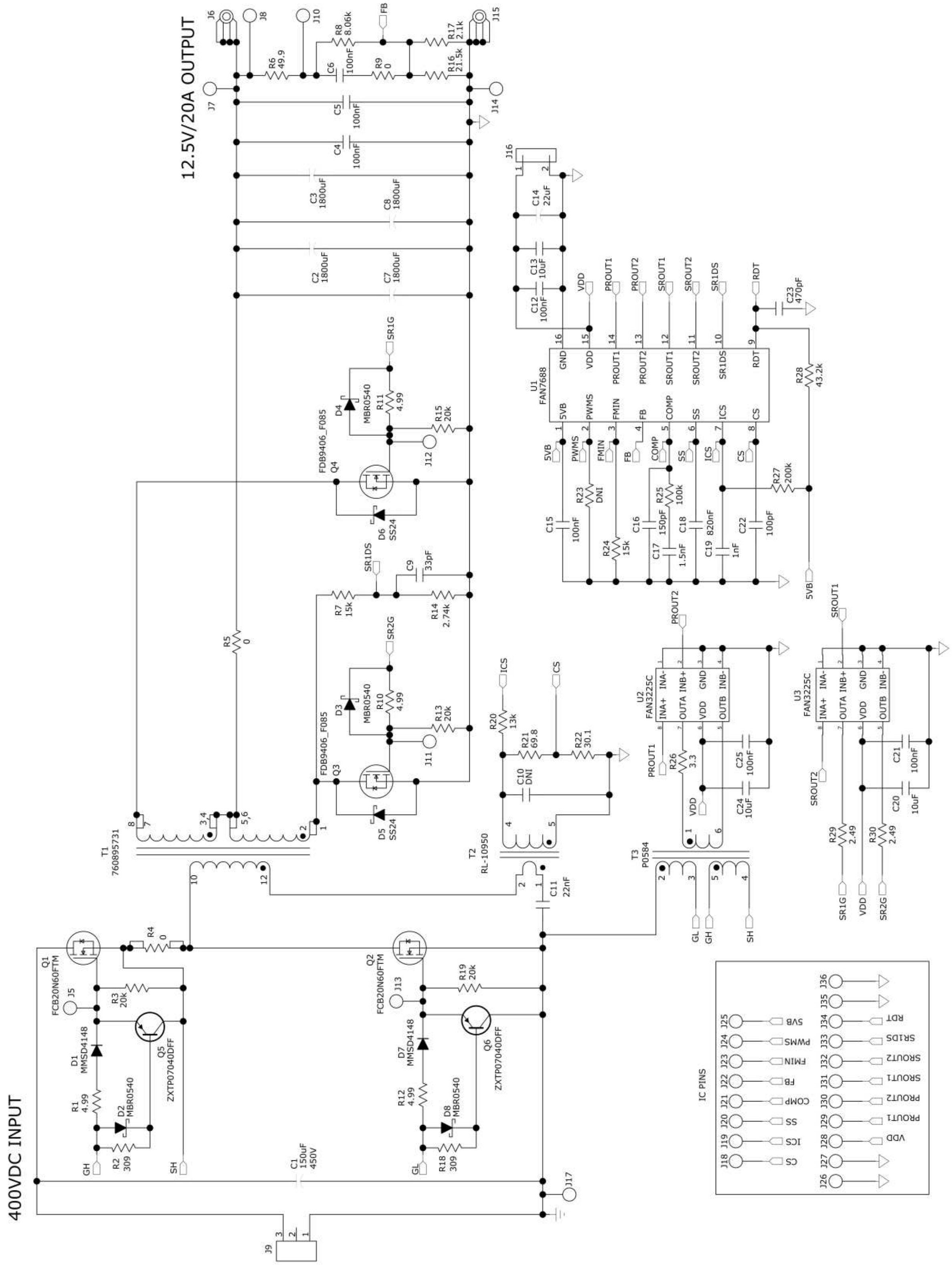


Figure 6. Evaluation Board Schematic

6. List of Test Points

Table 2. List of Test Points

Test Point	Name	Description
J5	GD	Primary upper MOSFET, Q1, floating gate
J7	+OUT	+12.5 V output Kelvin sense
J8	+Loop	Network analyzer perturbation loop injection +
J10	-Loop	Network analyzer perturbation loop injection -
J11	GD	SR, Q3, gate, secondary ground referenced
J12	GD	SR, Q4, gate, secondary ground referenced
J13	GD	Primary lower MOSFET, Q1, gate, primary ground referenced
J14	GND	Secondary ground, use for J11-2 gate drive
J17	PRI GND	Primary ground, use for J13 gate drive
J18	CS	FAN7688 CS pin, current sensing for OCP
J19	ICS	FAN7688 ICS pin, integrated current sense for charge control
J20	SS	FAN7688 SS pin, soft-start
J21	COMP	FAN7688 COMP pin, error amplifier output
J22	FB	FAN7688 FB pin, divided down sensed output voltage
J23	FMIN	FAN7688 FMIN pin, minimum frequency setting
J24	PWMS	FAN7688 PWMS pin, PWM entry point
J25	5VB	FAN7688 5VB pin, 5 V reference
J26	GND	Secondary ground, +12.5 V output return Kelvin sense
J27	GND	Secondary ground
J28	VDD	FAN7688 VDD pin, VDD bias
J29	PROUT1	FAN7688 PROUT1 pin, PROUT1 gate drive
J30	PROUT2	FAN7688 PROUT2 pin, PROUT2 gate drive
J31	SROUT1	FAN7688 SROUT1 pin, SROUT1 gate drive
J32	SROUT2	FAN7688 SROUT2 pin, SROUT2 gate drive
J33	SR1DS	FAN7688 SR1DS pin, SR, Q3, drain-to-source sense
J34	RDT	FAN7688 RDT pin, PROUT and SROUT dead time setting
J35	GND	Secondary ground
J36	GND	Secondary ground
R4	R4	Option - remove R4, install primary drain current loop
R5	R5	Option - remove R5, install secondary AC current loop

7. Transformer Specifications

7.1. LLC Power Transformer

760895731 from Wurth Elektronik (www.we-online.com) is a LLC transformer orderable from Digikey. A split bobbin is used to incorporate the resonant inductance (leakage inductance) and magnetizing inductance into a single magnetic component.

- Core: ETD44 (A_e=172mm^2)
- Bobbin: 16 pin TH
- Magnetizing Inductance : 475 µH, ±10%
- Leakage Inductance: 100 µH, ±10%

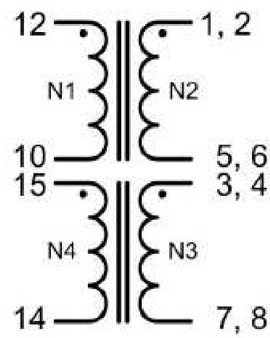


Figure 7. LLC Power Transformer (T1) in the Evaluation Board

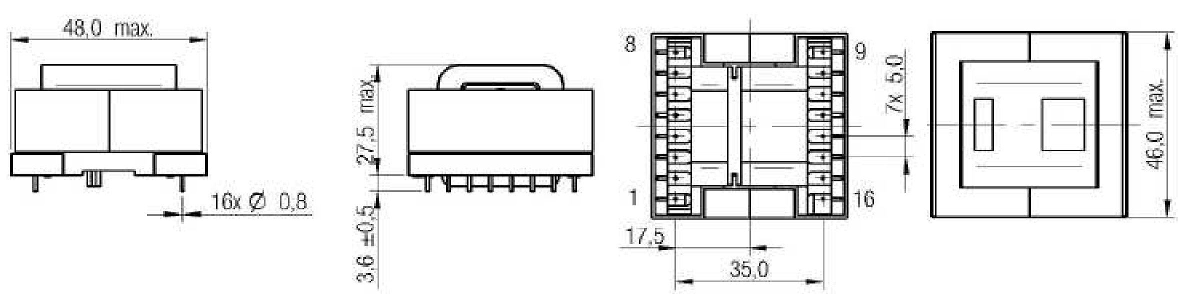


Figure 8. Wurth 760895731 Mechanical Drawing (dimensions in mm)

Table 3. Wurth 760895731 Transformer Electrical Specifications

Properties	Test conditions		Value	Unit	Tol.
Inductance	100 kHz/ 100 mV	L	475	µH	±10%
Turns ratio		n	35 : 2 : 2 : 3		±3%
Saturation current	I∆L/LI < 20%	I_{sat}	5.0	A	typ.
DC Resistance 1	@ 20°C	R_{DC1}	128	mΩ	max.
DC Resistance 2	@ 20°C	R_{DC2}	4.0	mΩ	max.
DC Resistance 3	@ 20°C	R_{DC3}	4.0	mΩ	max.
DC Resistance 4	@ 20°C	R_{DC4}	192	mΩ	max.
Leakage inductance	100 kHz/ 100 mV	L_S	100	µH	±10%
Insulation test voltage	W1,4 => W2,3	U_T	4000	V (AC)	

7.2. Current Sense Transformer

RL-10950 from Renco Electronics (www.rencousa.com) is a custom designed current sense transformer (CT). Most "off-the-shelf" CTs have primary to secondary isolation of <1000 V because they are not intended to operate across the isolation barrier. The RL-10950 is a 1:50 CT, specifically designed with 2500 V primary to secondary isolation which makes it more suitable for applcations such as the FAN7688 where the controller is on the secondary side and current sensing is coming from the primary side.

- Core: EP7 (A_e=9mm^2)
- Bobbin: 16 pin TH
- Magnetizing Inductance : 2.75mH, +40%/-20%

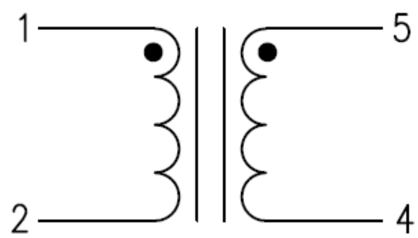


Figure 9. Current Sense Transformer (T2) in the Evaluation Board

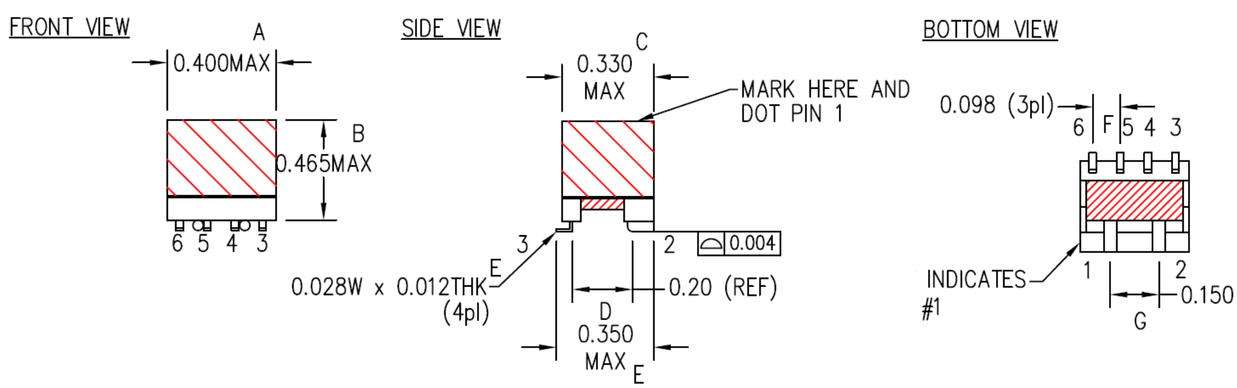


Figure 10. Renco RL-10950 Mechanical Drawing (dimensions in inches)

Table 4. RL-10950 Transformer Electrical Specifications

Parameter	Test Conditions	Ref,	Value	Unit	Tolerance
Inductance	100 kHz, 0,1 V_{AC}	L	2.75	mH	+40% / -20%
Turns Ratio			1:50		
DC Resistance 1	Pins 1-2, @25°C	$R_{DC(1-2)}$	7.5	mΩ	±25%
DC Resistance 2	Pins 5-4, @25°C	$R_{DC(5-4)}$	1.15	Ω	Max.
Isolation	2500 V_{AC} @ 60 Hz for 2s, Pins 1-5		2500	V_{AC}	Min.

8. Four-Layer PCB and Assembly Images

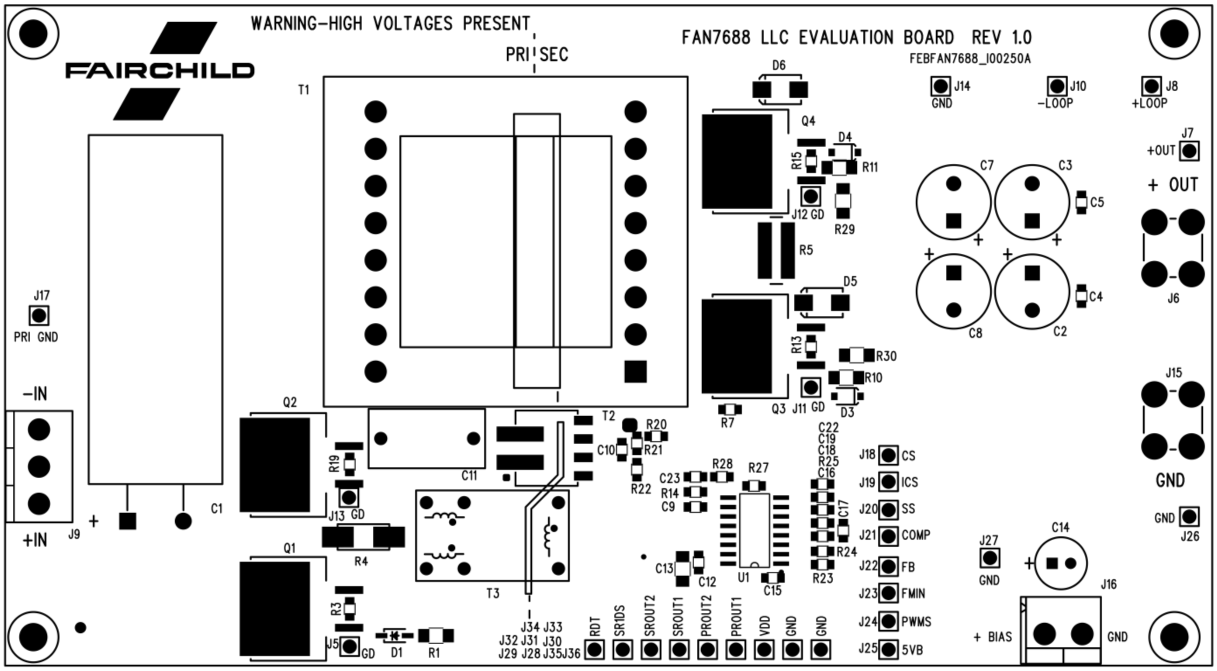


Figure 11. Layer 1 – Top Assembly Layer

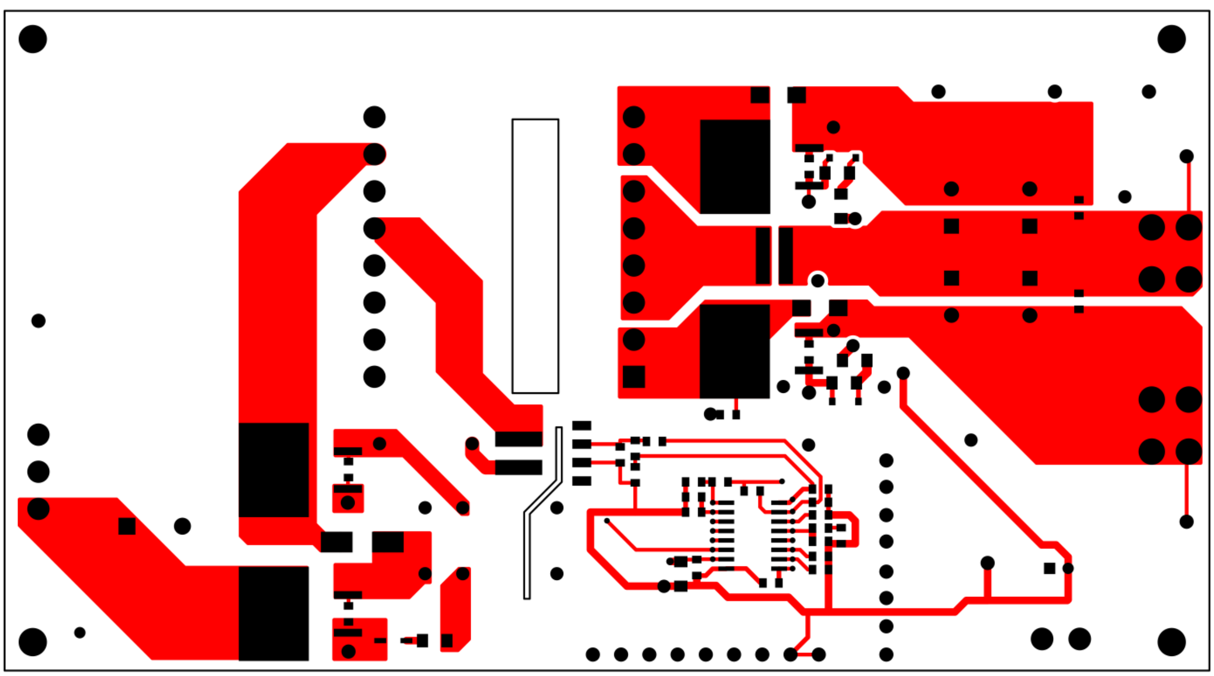


Figure 12. Layer 1 – Top Copper Layer

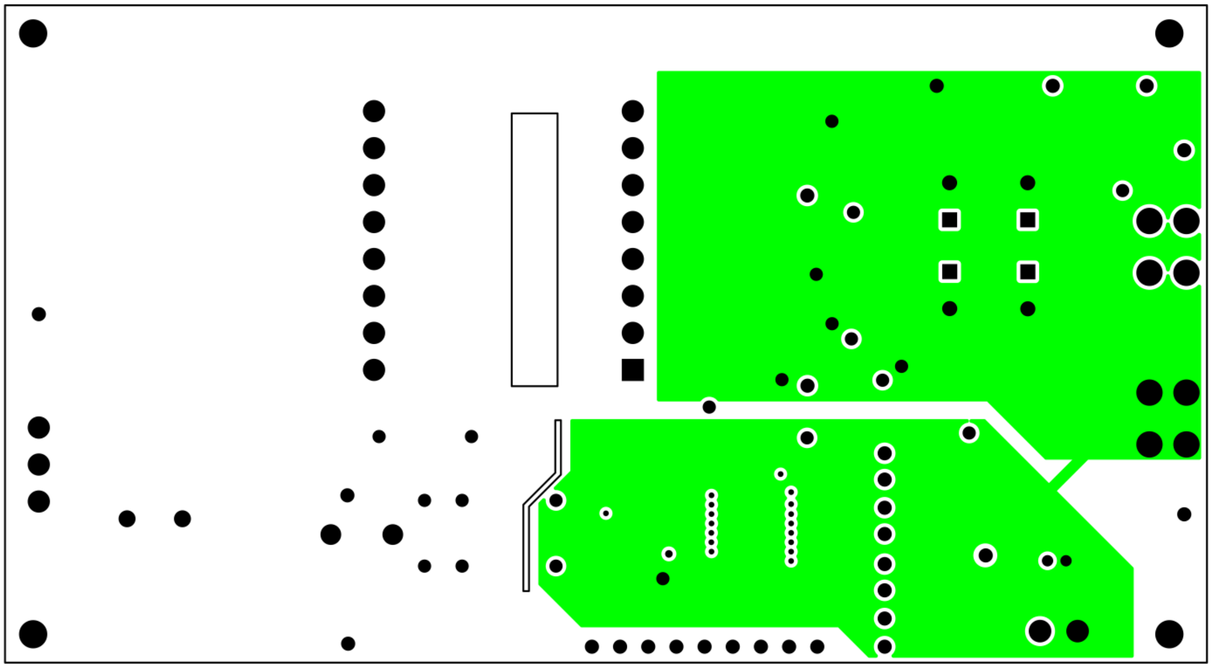


Figure 13. Layer 2 – Internal Copper Layer

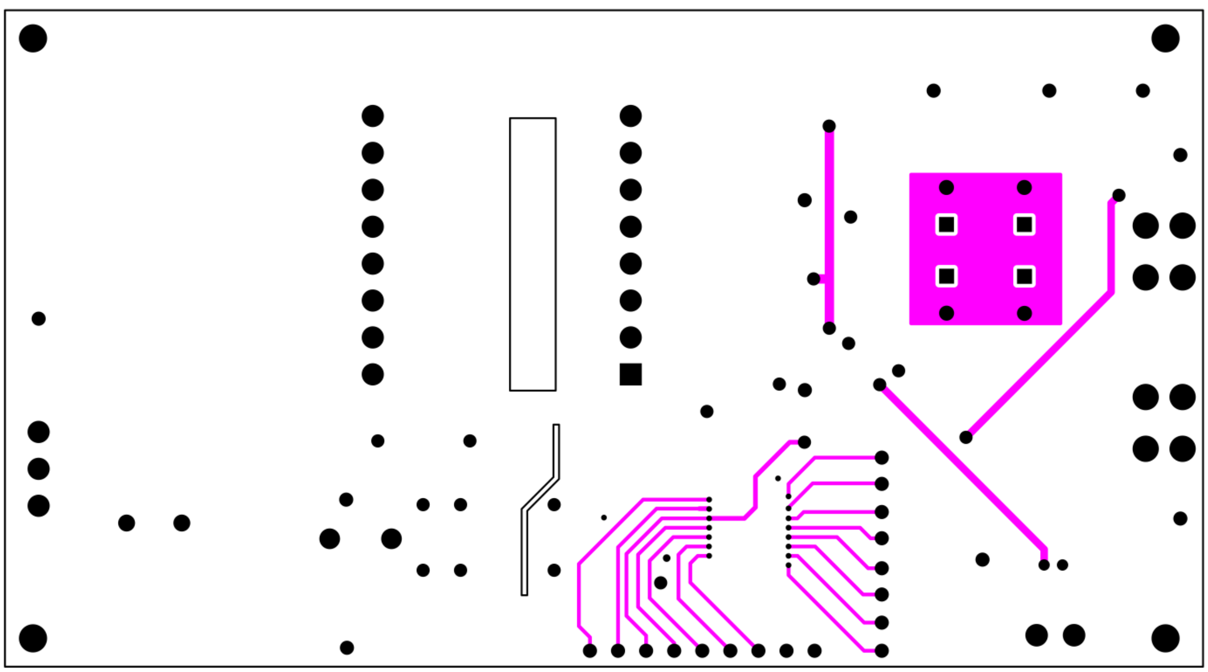


Figure 14. Layer 3 – Internal Copper Layer

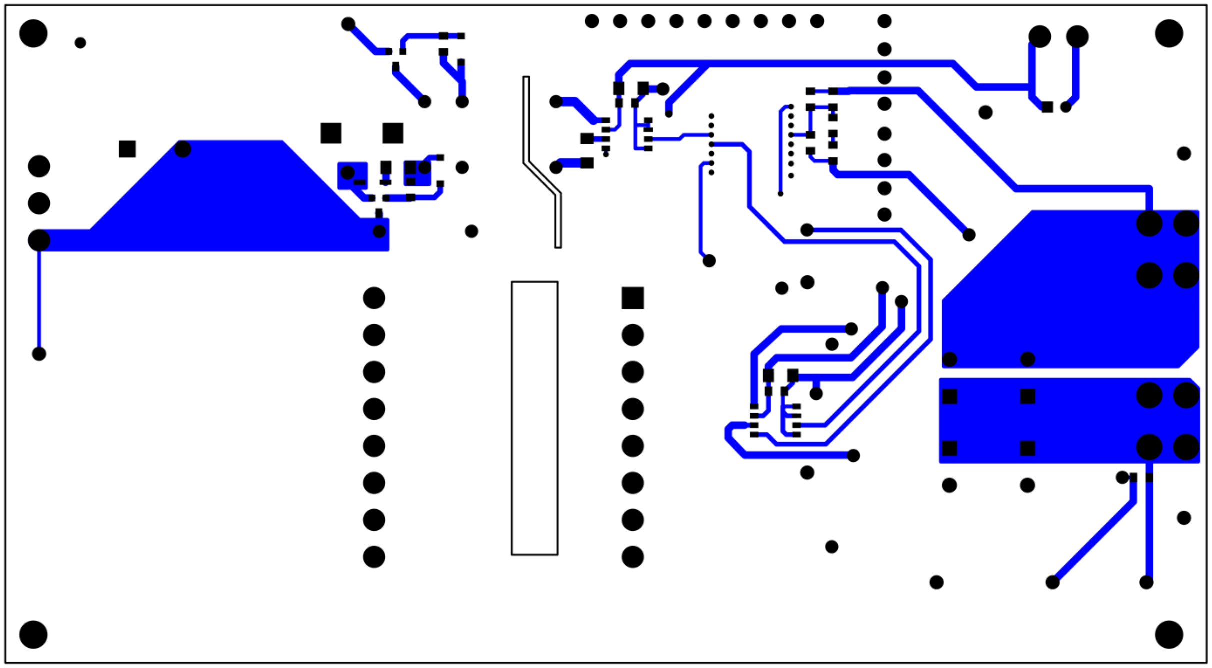


Figure 15. Layer 4 – Bottom Copper Layer

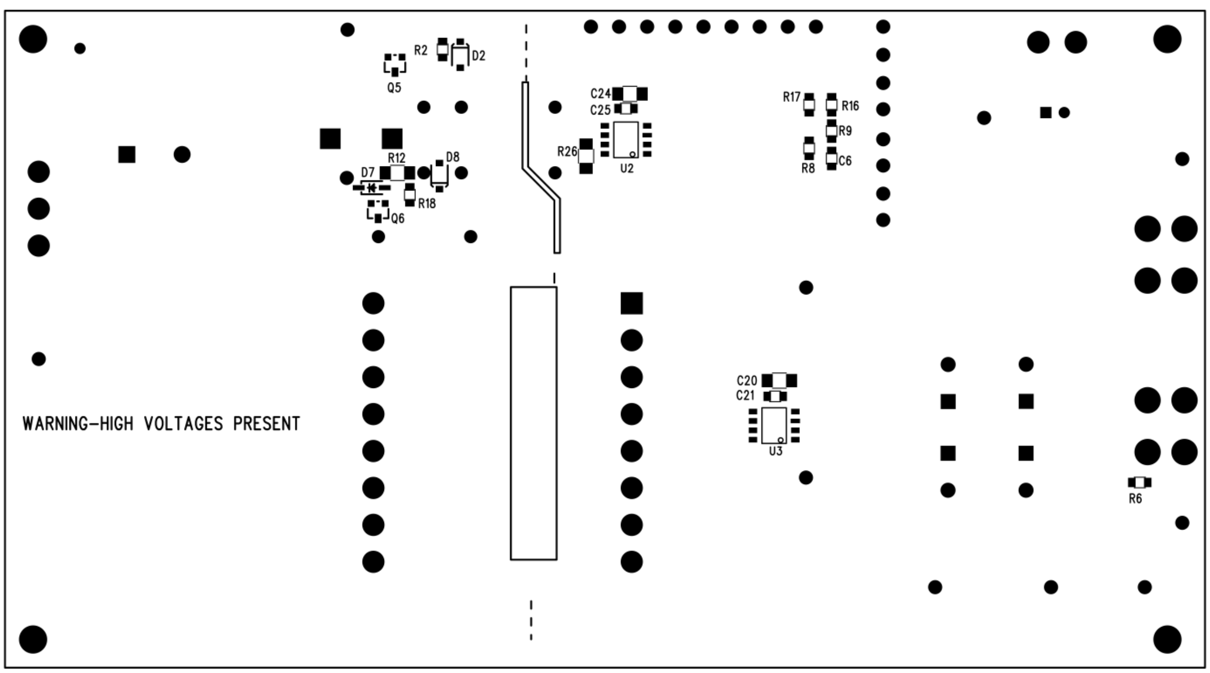


Figure 16. Layer 4 – Bottom Assembly Layer

9. Bill of Materials (BOM)

Table 5. Bill of Materials

Item	Qty.	Reference	Value	Part Number	Description	Manufacturer	Package
1	1	C1	150 µF	450BXW150MEFC18X45	Cap, Alum, 450 V, 20%	Rubycon	Thru-Hole
2	4	C2-3, C7-8	1800 µF	UHN1C182MPD	Cap, Alum, 16 V, 20%	Nichicon	Thru-Hole
3	7	C4-6, C12, C15, C21, C25	100 nF		CAP, SMD, CERAMIC, 25 V, X7R	STD	805
4	1	C9	33 pF		CAP, SMD, CERAMIC, 25 V, X7R	STD	805
5	0	C10	**DNI**		CAP, SMD, CERAMIC	STD	805
6	1	C11	22 nF	ECW-H8223HA	Cap, 800VDC, Metal Poly Film, 3%	Panasonic	Radial
7	3	C13, C20, C24	10 µF		CAP, SMD, CERAMIC, 25 V, X7R	STD	1206
8	1	C14	22 µF	EEA-GA1E220B	Cap, Alum, 25 V, 20%	Panasonic	Axial
9	1	C16	150 pF		CAP, SMD, CERAMIC, 25 V, X7R	STD	805
10	1	C17	1.5 nF		CAP, SMD, CERAMIC, 25 V, X7R	STD	805
11	1	C18	820 nF		CAP, SMD, CERAMIC, 25 V, X7R	STD	805
12	1	C19	1 nF		CAP, SMD, CERAMIC, 25 V, X7R	STD	805
13	1	C22	100 pF		CAP, SMD, CERAMIC, 25 V, X7R	STD	805
14	1	C23	470 pF		CAP, SMD, CERAMIC, 25 V, X7R	STD	805
15	2	D1, D7		MMSD4148	Diode, 200 mA, 100 V, Signal Diode	Fairchild	SOD-123
16	4	D2-4, D8		MBR0540	Diode, Schottky, 40 V, 500 mA	Fairchild	SOD-123
17	2	D5-6		SS24	Diode, Schottky, 40 V, 2 A	Fairchild	SMB
18	28	J5, J7-8, J10-14, J17-36		3103-2-00-21-00-00-08-0	Test pin, Gold, 40 mil	Mill-Max	Thru-Hole
19	2	J6, J15		7701	Terminal, 15 A, Vertical, PC mount	Keystone	Thru-Hole
20	1	J9		ED100/3DS	Header, Vert. 3 pin, 5 mm Spacing	OST	Thru-Hole
21	1	J16		OSTTA024163	Header, 2 pin, 100 mil Spacing, 15 A	OST	Thru-Hole
22	2	Q1-2		FCB20N60FTM	MOSFE, N-CH, 600 V, 20 A, 190 mΩ	Fairchild	D2PAK
23	2	Q3-4		FDB9406_F085	MOSFE, N-CH, 40 V, 110 A, 1.8 mΩ	Fairchild	D2PAK
24	2	Q5-6		ZXTP07040DFF	Transistor, PNP, -40 V, -3 A	Diodes Inc.	SOT-23

Item	Qty.	Reference	Value	Part Number	Description	Manufacturer	Package
25	4	R1, R10-12	4.99 Ω		RES, SMD, 1/4W	STD	1206
26	2	R2 ,R18	309 Ω		RES, SMD, 1/8W	STD	805
27	4	R3, R13, R15, R19	20 kΩ		RES, SMD, 1/8W	STD	805
28	1	R4	0 Ω		RES, SMD, 1/2W	STD	2010
29	1	R5	0 Ω	12250000Z0EG	RES, SMD, 1W	Vishay	2512W
30	1	R6	20 Ω		RES, SMD, 1/8W	STD	805
31	2	R7, R24	15 kΩ		RES, SMD, 1/8W	STD	805
32	1	R8	8.06 kΩ		RES, SMD, 1/8W	STD	805
33	1	R9	0 Ω		RES, SMD, 1/8W	STD	805
34	1	R14	2.74 kΩ		RES, SMD, 1/8W	STD	805
35	1	R16	21.5 kΩ		RES, SMD, 1/8W	STD	805
36	1	R17	2.1 kΩ		RES, SMD, 1/8W	STD	805
37	1	R20	13 kΩ		RES, SMD, 1/8W	STD	805
38	1	R21	69.8 Ω		RES, SMD, 1/8W	STD	805
39	1	R22	30.1 Ω		RES, SMD, 1/8W	STD	805
40	0	R23	**DNI**		RES, SMD, 1/8W	STD	805
41	1	R25	100 kΩ		RES, SMD, 1/8W	STD	805
42	1	R26	3.3 Ω		RES, SMD, 1/4W	STD	1206
43	1	R27	200 kΩ		RES, SMD, 1/8W	STD	805
44	1	R28	43.2 kΩ		RES, SMD, 1/8W	STD	805
45	2	R29-30	2.49 Ω		RES, SMD, 1/4W	STD	1206
46	1	T1		760895731	XFMR, LLC, 475 µH, 100 µH	Wurth Elektronik	Thru-Hole
47	1	T2		RL-10950	XFMR, CT, 1:50, 35 A	Renco	SMD
48	1	T3		P0584	XFMR, Gate Drive, 1:1:1, 450 µH	Pulse	Thru-Hole
49	1	U1		FAN7688	LLC Resonant PFM Controller	Fairchild	SOIC-16DW
50	2	U2-3		FAN3225C	Driver, Low-Side, High-Speed, 4 A	Fairchild	SOIC-8
51	1	PWB		FEBFAN7688_100250A	PWB, 4-Layer, FR4, 0.062"	Custom	N/A
52	2	Sleeving,C1 HV leads		TFT20018 NA005	1.02 mm x 1.78 mm x 13 mm (IDxODxL)	Alpha Wire	N/A
53	1	N/A			Silicone adhesive bonding for C1		N/A
54	4	N/A		8441B	Hex Standoff, 6-32, Nylon, 3/8"	Keystone	Nylon
55	4	N/A		NY PMS 632 0038 PH	Machine Screw, Nylon, 6-32 x 3/8"	B&F Fastener	Nylon

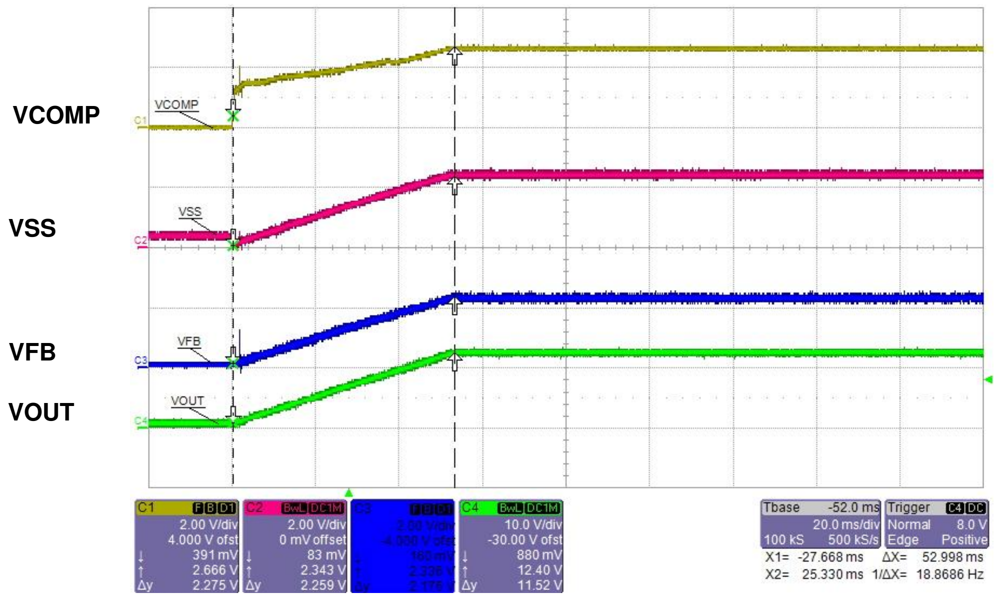
Notes:
1. STD = Standard Components
2. DNI = Do Not Install

10. Test Data

The following section shows measured wave forms, efficiency, control loop and thermal data for the EVB.

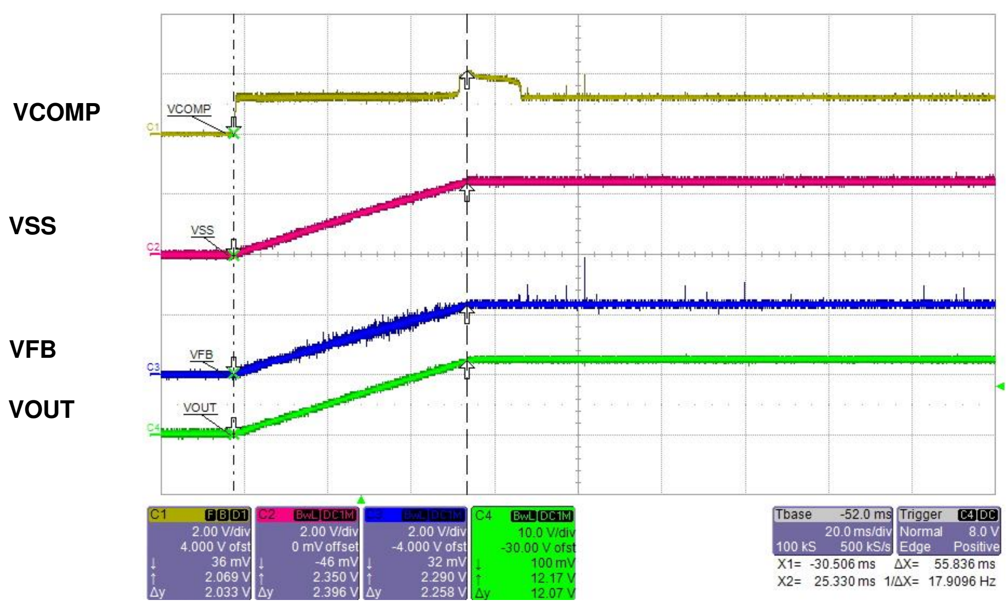
10.1. Startup

Figure 17 and Figure 18 show the monotonic soft-start operation at 400 V_{DC} line for full-load and min-load condition, respectively.



CH1: COMP Voltage (2 V/div), CH2: Soft-start Voltage (2 V/div), CH3: Feedback Voltage (2 V/div), CH4: Output Voltage (10V/div), Time (20 ms/div)

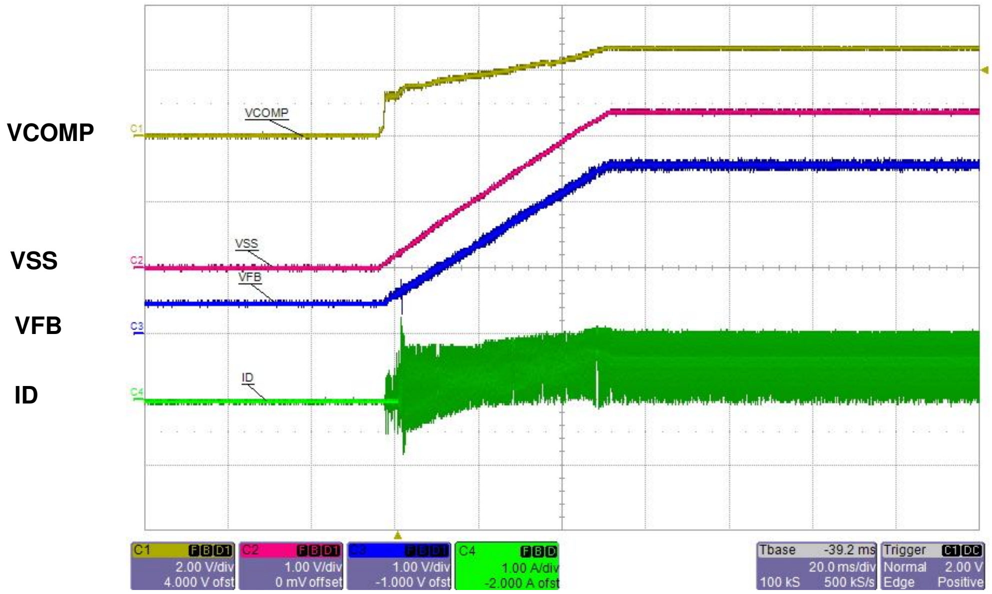
Figure 17. Full-Load (20 A) Startup at 400 V_{DC}, t_{SS} (Soft-start)=53 ms



CH1: COMP Voltage (2 V/div), CH2: Soft-start Voltage (2 V/div), CH3: Feedback Voltage (2 V/div), CH4: Output Voltage (10 V/div), Time (20 ms/div)

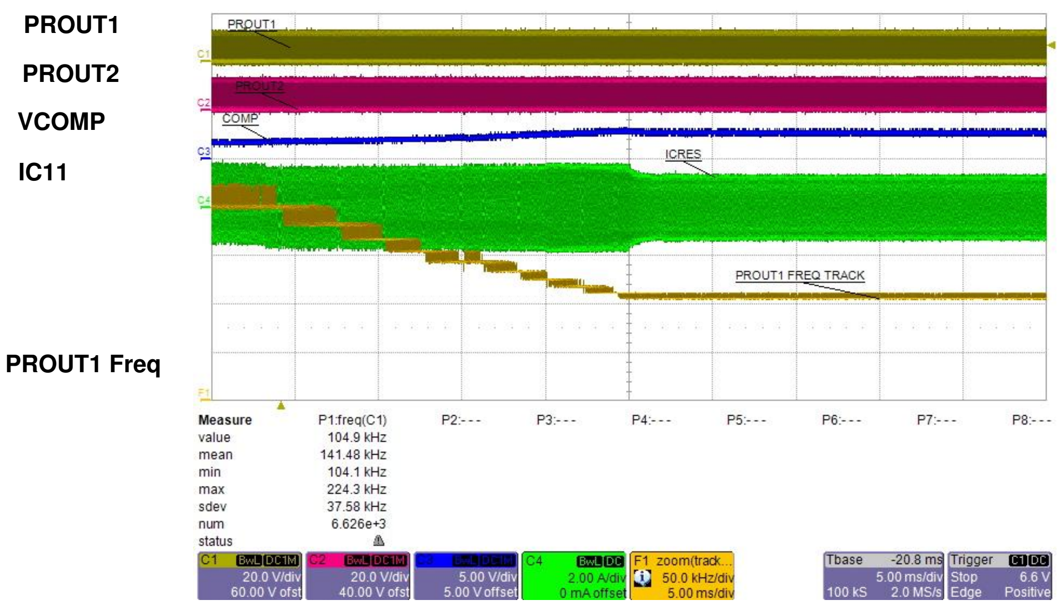
Figure 18. No-Load (0 A) Startup at 400 V_{DC}, t_{SS} (Soft-start)=55 ms

Figure 19 shows the startup operation at 400 V_{DC} for full-load. The primary drain current shows no current overshoot. No overshoot is observed for full load startup or minimum load startup. Figure 20 is captured 14 ms after startup is initiated. A frequency tracking function was used to show PROUT1 frequency variation from the initial frequency of 224 kHz (PWM mode) to steady state frequency (resonance) of 105 kHz (PFM mode). The frequency transition is smooth and shows no signs of oscillation or abnormal variation.



CH1: COMP Voltage (2 V/div), CH2: Soft-start Voltage (1 V/div), CH3: Feedback Voltage (1 V/div), CH4: Drain Current (1 A/div), Time (20 ms/div)

Figure 19. Full-Load (20 A) Startup at 400 V_{DC}, Primary Drain Current, I_{R4}

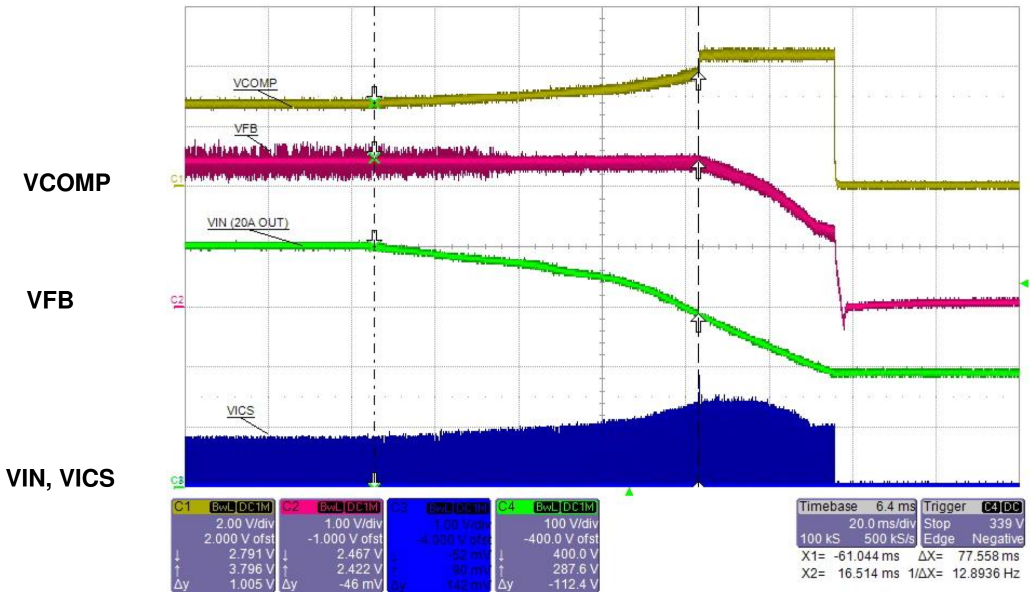


CH1: PROUT1 (20 V/div), CH2: PROUT2 (20 V/div), CH3: COMP Voltage (5 V/div), CH4: Resonant Current (2 A/div), PROUT1 Freq Track (50 kHz/div), Time (5 ms/div)

Figure 20. Full-Load (20 A) Startup at 375 V_{DC}, Frequency Track, 105 kHz<F_{PROUT1}<240 kHz

10.2. Hold-Up

Hold-up time is measured at full load from the time that VIN is removed until VOUT drops out of regulation. The feedback voltage, VFB, is proportional to VOUT and as shown in Figure 21, stays in regulation for 77 ms for 287 V_{DC}<VIN<400 V_{DC}. As VIN is decreasing, the sensed primary ICS current, VICS, is increasing. Also during this time, the converter operation transitions from above resonance to below resonance. The FAN7688 ICS voltage threshold limit shifts accordingly from 1.2 V (above resonance) to 1.45 (below resonance). This shift in ICS voltage threshold permits operation down to a lower VIN level without causing an overload limit, thus increasing the amount of available hold-up time.

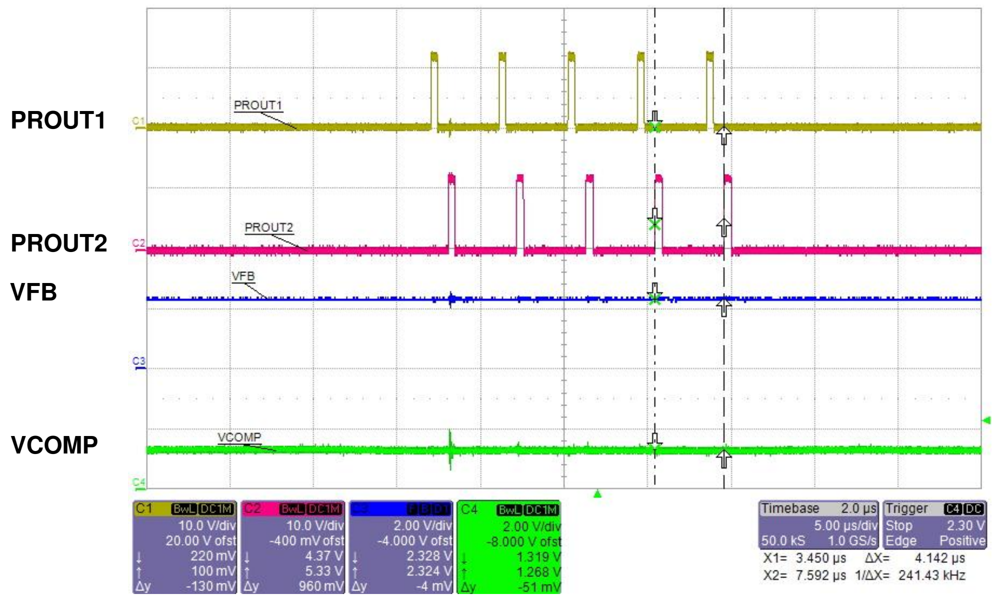


CH1: COMP Voltage (2 V/div), CH2: Feedback Voltage (1 V/div), CH3: ICS Voltage (1 V/div), CH4: Input Voltage (100 V/div), Time (20 ms/div)

Figure 21. Full-Load (20 A), VIN=400 V_{DC}, Hold-Up Time, t_{HU}=77 ms

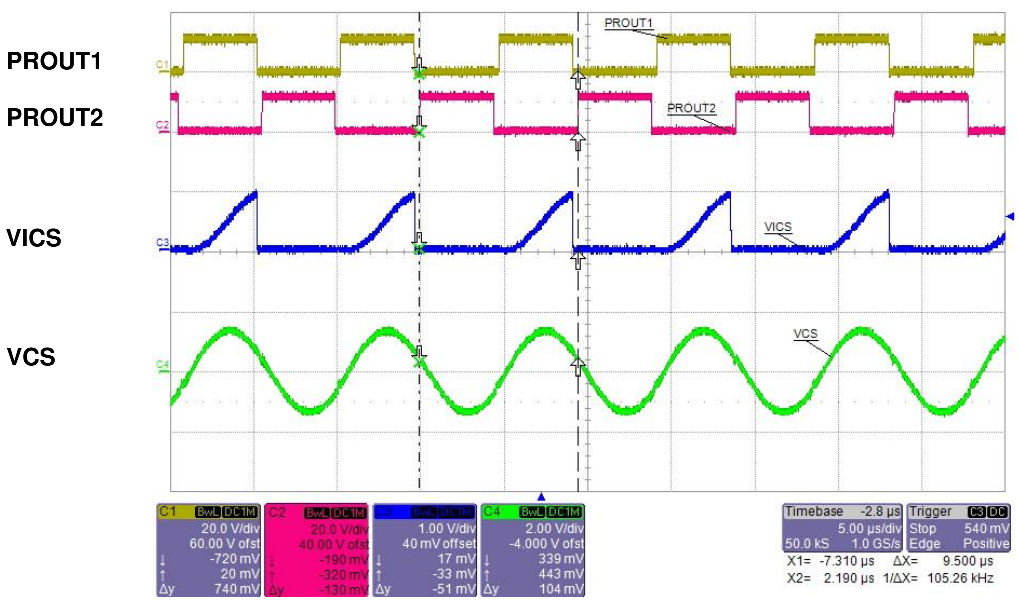
10.3. Steady-State Operation

Figure 22 through Figure 25 shows the full load, switching frequency variation for 300 V_{DC}<VIN<450 V_{DC}.



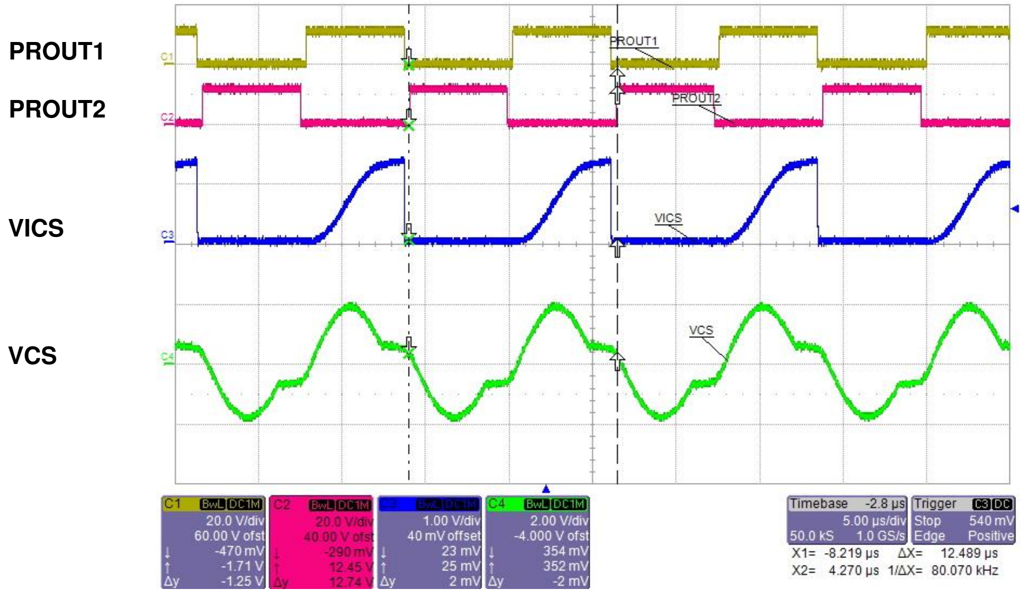
CH1: PROUT1 (10 V/div), CH2: PROUT2 (10 V/div), CH3: Feedback Voltage (2 V/div), CH4: COMP Voltage (2 V/div), Time (5 µs/div)

Figure 22. PWM Burst Mode, I_{OUT}=250 mA, VIN=400 V_{DC}, f_{PWM}=240 kHz



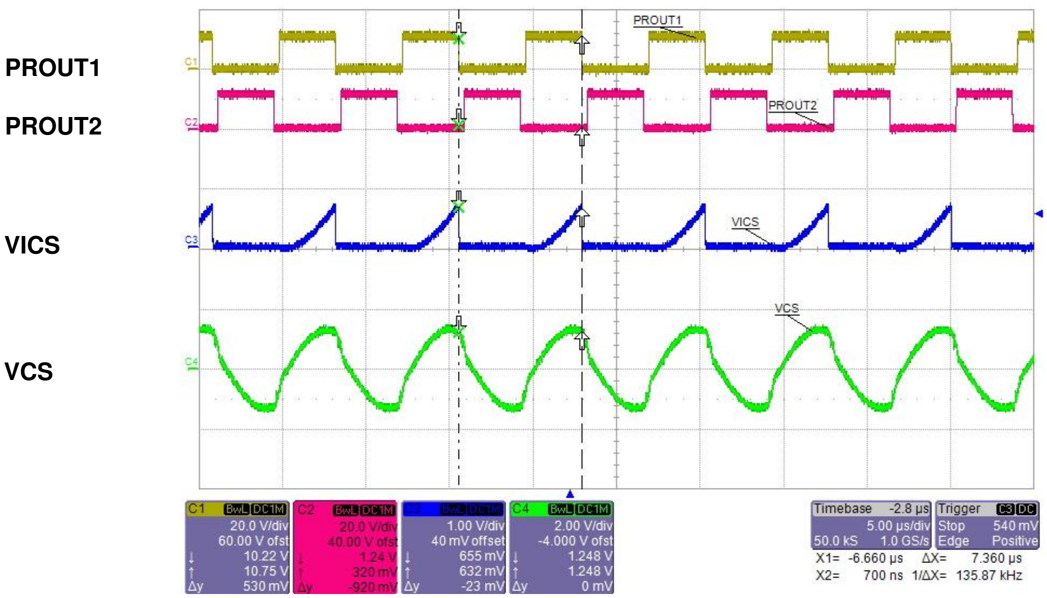
CH1: PROUT1 (20 V/div), CH2: PROUT2 (20 V/div), CH3: ICS Voltage (1 V/div), CH4: CS Voltage (2 V/div), Time (5 µs/div)

Figure 23. PFM Mode, at Resonance, I_{OUT}=20 A, VIN=375 V_{DC}, f_{RES}=105 kHz



CH1: PROUT1 (20 V/div), CH2: PROUT2 (20V/div), CH3: ICS Voltage (1 V/div), CH4: CS Voltage (2 V/div), Time (5 µs/div)

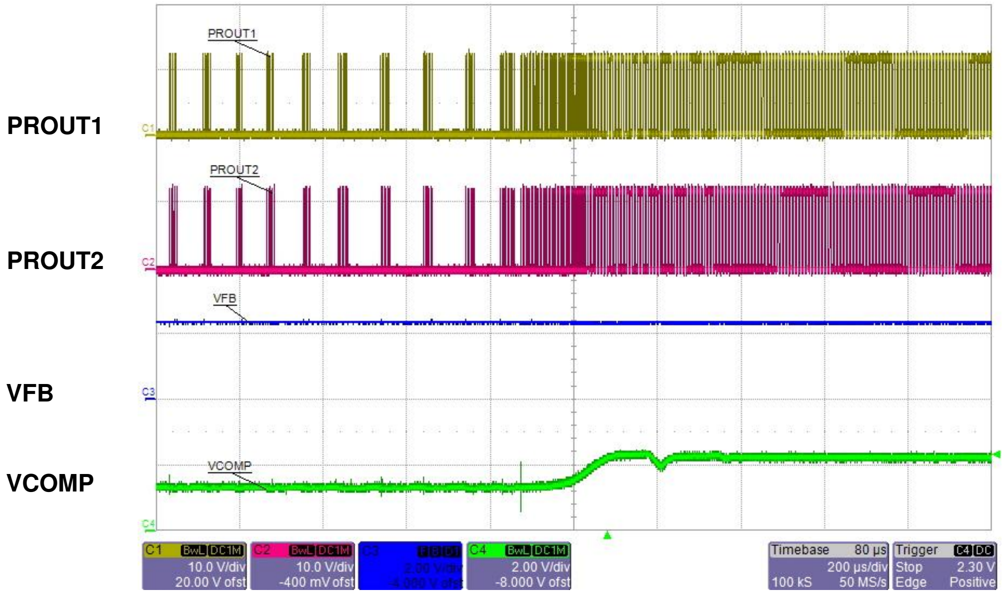
Figure 24. PFM Mode, Below Resonance, I_{OUT}=20 A, VIN=300 V_{DC}, F=80 kHz



CH1: PROUT1 (20 V/div), CH2: PROUT2 (20 V/div), CH3: ICS Voltage (1 V/div), CH4: CS Voltage (2 V/div), Time (5 µs/div)

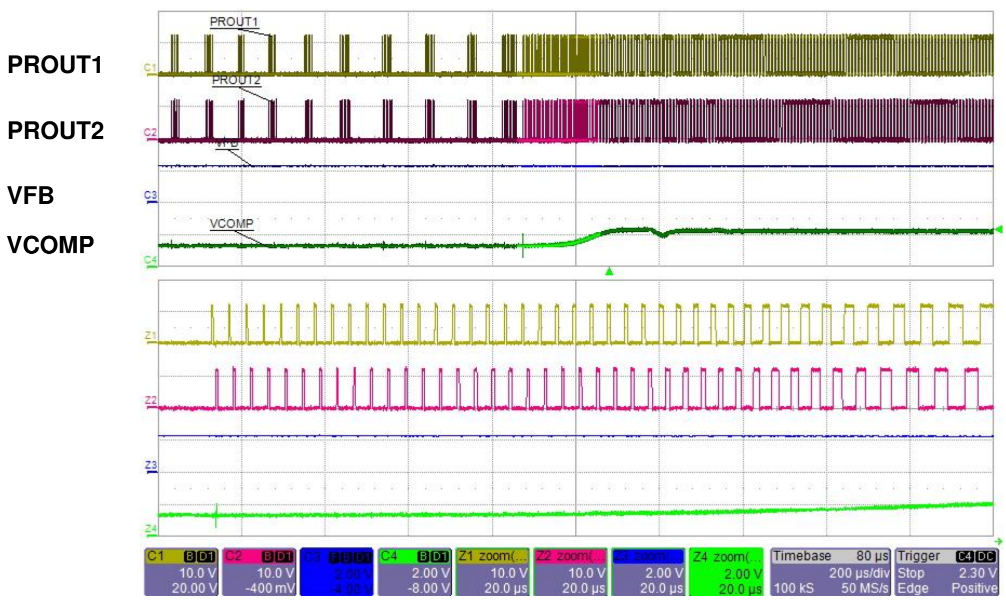
Figure 25. PFM Mode, Above Resonance, I_{OUT}=20 A, VIN=450 V_{DC}, F=136 kHz

Figure 26 shows the transition between PWM burst mode and PFM mode as a current load step from 250 mA to 5 A is introduced. Figure 27 is a zoom showing the smooth transition into the start of PFM mode. The duty cycle increases smoothly as the COMP voltage is increasing.



CH1: PROUT1 (10 V/div), CH2: PROUT2 (10 V/div), CH3: Feedback Voltage (2 V/div), CH4: COMP Voltage (2 V/div), Time (200 µs/div)

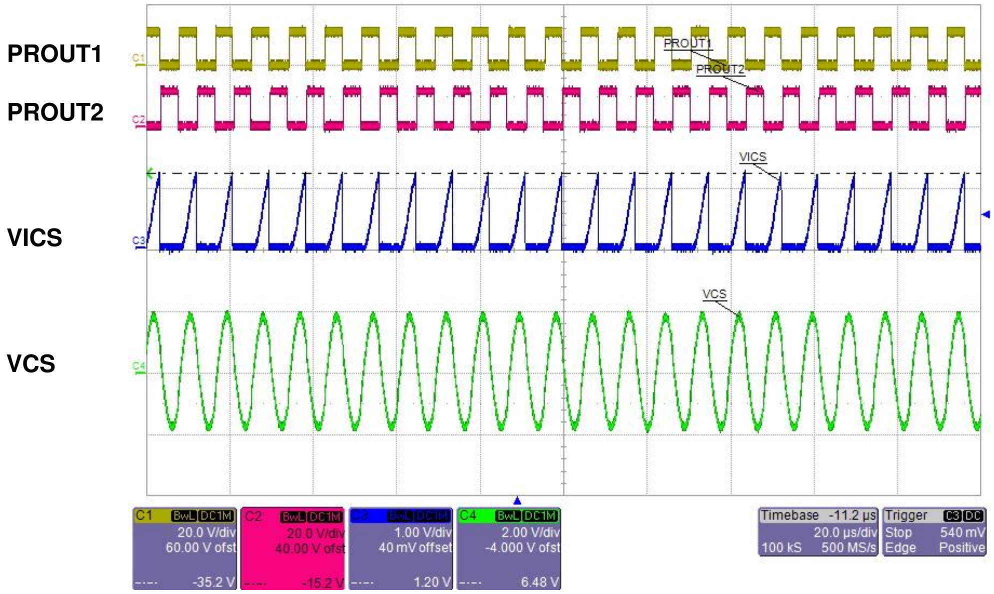
Figure 26. PWM Burst to PFM Mode Change, I_{OUT}=250 mA to 5 A Step, VIN=400 V_{DC}



CH1: PROUT1 (10 V/div), CH2: PROUT2 (10 V/div), CH3: Feedback Voltage (2 V/div), CH4: COMP Voltage (2 V/div), Time (200 µs/div), Zoom Time (20 µs/div)

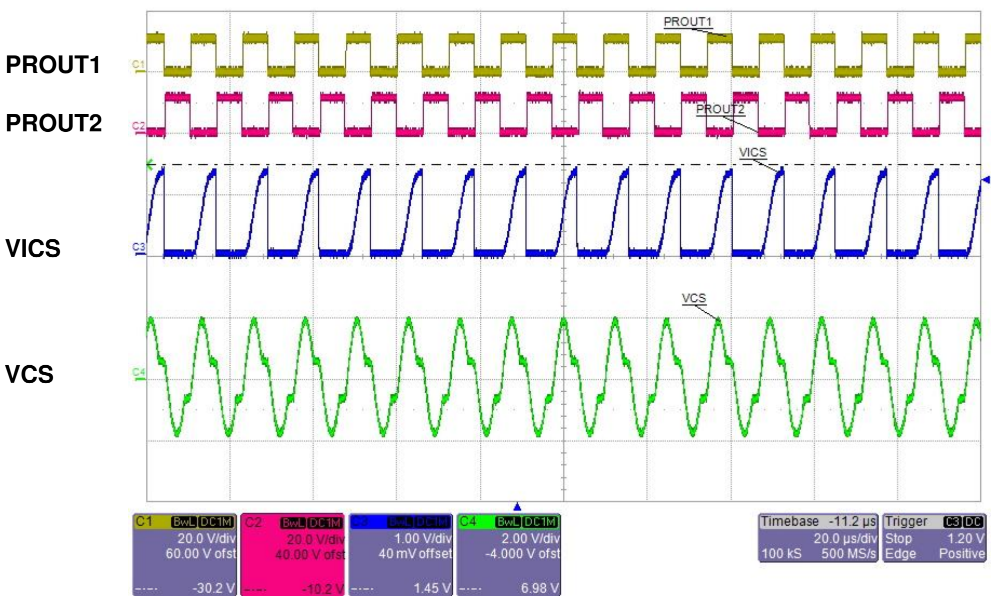
Figure 27. PWM Burst to PFM Mode Change, I_{OUT}=250 mA to 5 A Step, VIN=400 V_{DC}

Figure 28 shows the maximum load current (IOUT=29 A) just before over-current limit when operating above resonance where the VICS threshold limit (V_{OCL1}) is 1.2 V. Figure 29 shows the maximum load current (IOUT=21 A) just before over-current limit when operating below resonance where the VICS threshold limit (V_{OCL2}) is 1.45 V.



CH1: PROUT1 (20 V/div), CH2: PROUT2 (20 V/div), CH3: ICS Voltage (1 V/div), CH4: CS Voltage (2 V/div), Time (20 µs/div)

Figure 28. Just Before Over-Current Limit, Above Resonance, I_{OUT}=29 A, VIN=400 V_{DC}, VICS=1.2 V



CH1: PROUT1 (20 V/div), CH2: PROUT2 (20 V/div), CH3: ICS Voltage (1 V/div), CH4: CS Voltage (2 V/div), Time (20 µs/div)

Figure 29. Just Before Over-Current Limit, Below Resonance, I_{OUT}=21 A, VIN=300 V_{DC}, VICS=1.45 V