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FGLD12SR6040*A

Data Sheet

4.5-14.4Vdc Input, 40A, 0.45-2.0Vdc Output

The Digital ***Tomodachi*** Series of non-isolated dc-dc converters deliver exceptional electrical and thermal performance in DOSA based footprints for Point-of-Load converters. Operating from a 4.5Vdc-14.4Vdc input, these are the converters of choice for Intermediate Bus Architecture (IBA) and Distributed Power Architecture applications that require high efficiency, tight regulation, and high reliability in elevated temperature environments with low airflow. The PMBus interface supports a range of commands to both control and monitor the module. The module also includes the Tunable Loop™ feature that allows the user to optimize the dynamic response of the converter to match the load with reduced amount of output capacitance leading to savings on cost and PWB area.

The **FGLD12SR6040*A** converter of the ***Tomodachi*** Series delivers 40A of output current at a tightly regulated programmable and PMBus control output voltage of 0.45Vdc to 2.0Vdc. The thermal performance of the **FGLD12SR6040*A** is best-in-class: Little derating is needed up to 85℃, under natural convection.

Applications

- Intermediate Bus Architecture
- Telecommunications
- Data/Voice processing
- Distributed Power Architecture
- Computing (Servers, Workstations)
- Test Equipments

Features

- Compliant to RoHS EU “Directive 2011/65/EU
- Delivers up to 40A (80W)
- High efficiency, no heatsink required
- Negative and Positive ON/OFF logic
- DOSA based
- Small size: 33.02 x 13.46 x 10.9mm (1.3 in x 0.53 in x 0.429 in)
- Tape & reel packaging
- Programmable output voltage from 0.6V to 2.0V via external resistor. Digitally adjustable down to 0.45Vdc
- Digital interface through the PMBus™ # protocol
- Tunable Loop™ to optimize dynamic output voltage response
- Flexible output voltage sequencing EZ-SEQUENCE
- Power Good signal
- Fixed switching frequency with capability of external synchronization
- Auto-reset output over-current protection
- Remote ON/OFF
- Ability to sink and source current
- No minimum load required
- Start up into pre-biased output
- *UL** 60950-1 2nd Ed. Recognized, *CSA*† C22.2 No. 60950-1-07 Certified, and *VDE*‡ (EN60950-1 2nd Ed.) (Pending)
- ISO** 9001 and ISO 14001 certified manufacturing facilities

* *UL* is a registered trademark of Underwriters Laboratories, Inc.
† *CSA* is a registered trademark of Canadian Standards Association.
‡ *VDE* is a trademark of Verband Deutscher Elektrotechniker e.V.
** ISO is a registered trademark of the International Organization of Standards
# The PMBus name and logo are registered trademarks of the System Management Interface Forum (SMIF)

FGLD12SR6040*A

Data Sheet

4.5-14.4Vdc Input, 40A, 0.45-2.0Vdc Output

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings may lead to degradation in performance and reliability of the converter and may result in permanent damage.

PARAMETER	NOTES	MIN	TYP	MAX	UNITS
ABSOLUTE MAXIMUM RATINGS[1]					
Input Voltage	Continuous	-0.3		15	Vdc
SEQ, SYNC, Vs+				7	Vdc
CLK, DATA, SMBALERT				3.6	Vdc
Operating Temperature	Ambient temperature	-40		85	°C
Storage Temperature		-55		125	°C
Output Voltage		0.45		2.0	Vdc

Electrical Specifications

All specifications apply over specified input voltage, output load, and temperature range, unless otherwise noted.

PARAMETER	NOTES	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS					
Operating Input Voltage Range		4.5		14.4	Vdc
Maximum Input Current	Vin=4.5V to 14V, Io-max			24	Adc
Input No Load Current	Vout=2.0V		104		mA
	Vout=0.6V		54.7		mA
Input Stand-by Current	Vin=12V, module disabled		16.4		mA
Inrush Transient, I^2t				1	A^2s
Input Reflected-Ripple Current	Peak-to-peak (5Hz to 20MHz, 1uH source impedance; Vin=0 to 14V, Io-max		90		mAp-p
Input Ripple Rejection (120Hz)			-60		dB
Input Under Voltage Lockout					
Turn-on Threshold				3.25	Vdc
Turn-off Threshold		2.6			Vdc
Hysteresis			0.25		Vdc
PMBus Adjustable Input Under Voltage Lockout Thresholds		2.5		14	Vdc
Resolution of Adjustable Input Under Voltage Threshold				500	mV

FGLD12SR6040*A

Data Sheet

4.5-14.4Vdc Input, 40A, 0.45-2.0Vdc Output

Electrical Specifications (Continued)

PARAMETER	NOTES	MIN	TYP	MAX	UNITS
OUTPUT CHARACTERISTICS					
Output Voltage Set Point	With 0.1% tolerance for external resistor used to set output voltage	-1.0		+1.0	%Vout
Output Voltage Range	(Over all operating input voltage, resistive load and temperature conditions until end of life)	-3.0		+3.0	%Vout
Adjustment Range (selected by an external resistor)	Some output voltages may not be possible depending on the input voltage – see feature description section	0.6		2.0	Vdc
PMBus Adjustable Output Voltage Range		-25		+25	%Vout
PMBus Output Voltage Adjustment Step Size		0.4			%Vout
Remote Sense Range				0.5	Vdc
Output Regulation	Line (Vin = min to max)			6	mV
	Load (Io = min to max)			10	mV
	Temperature (Tref=min to max)		0.4		%Vout
Output Ripple and Noise	Vin=12V, Io= min to max, Co = 0.1uF+22uF ceramic capacitors				
Peak to Peak	5MHz to 20MHz bandwidth		50	100	mVp-p
RMS	5MHz to 20MHz bandwidth		20	38	mVrms
External Load Capacitance [1]	Plus full load (resistive)				%
Without the Tunable Loop	ESR ≥ 1mΩ	6x47		6x47	uF
With the Tunable Loop	ESR ≥ 0.15mΩ	6x47		7,000	uF
	ESR ≥ 10mΩ	6x47		8,500	uF
Output Current Range	(in either sink or source mode)	0		40	Adc
Output Current Limit Inception (Hiccup mode)	Current limit does not operate in sink mode		150		% Io-max
Output Short-Circuit Current	Vo ≤ 250mV, Hiccup mode		2..1		Arms
Efficiency					
Vin = 12Vdc, Ta = 25°C, Io = max	Vout=1.8Vdc		91.5		%
	Vout=1.2Vdc		88.5		%
	Vout=0.6Vdc		81.3		%

[1] External capacitors may require using the new Tunable Loop™ feature to ensure that the module is stable as well as getting the best transient response. See the Tunable Loop™ section for details.

FGLD12SR6040*A

Data Sheet

4.5-14.4Vdc Input, 40A, 0.45-2.0Vdc Output

Electrical Specifications (Continued)

PARAMETER	NOTES	MIN	TYP	MAX	UNITS
Switching Frequency			400		kHz
Frequency Synchronization					
Synchronization Frequency Range		350		480	kHz
High Level Input Voltage		2.0			V
Low Level Input Voltage				0.4	V
Input Current, SYNC				100	nA
Minimum Pulse Width, SYNC		100			nS
Maximum SYNC rise time		100			nS

General Specifications

PARAMETER	NOTES	MIN	TYP	MAX	UNITS
Calculated MTBF	Io = 0.8 * Io-max, Ta = 40°C Telecordia Issue 2 Method 1 Case 3		6,498,438		Hours
Weight			11.7(0.41)		g (oz.)

Feature Specifications

PARAMETER	NOTES	MIN	TYP	MAX	UNITS
ON/OFF Signal Interface	Vin = min to max, open collector or equivalent, Signal reference to GND				
Positive Logic					
Logic High (Module ON)					
Input High Current				10	uA
Input High Voltage		3.5		Vin-max	V
Logic Low (Module OFF)					
Input Low Current				1	mA
Input Low Voltage		-0.3		0.4	V
Negative Logic	On/Off pin is open collector/drain logic input with external pull-up resistor; signal reference to GND				
Logic High (Module OFF)					
Input High Current				1	mA
Input High Voltage		2		Vin-max	V
Logic Low (Module ON)					
Input Low Current				10	uA
Input Low Voltage		-0.2		0.4	V

FGLD12SR6040*A

Data Sheet

4.5-14.4Vdc Input, 40A, 0.45-2.0Vdc Output

Feature Specifications

PARAMETER	NOTES	MIN	TYP	MAX	UNITS
Turn-On Delay and Rise Time	Vin = Vin-nom, Io = Io-max , Vo to within ±1% of steady state				
Case 1: On/Off input is enabled and then input power is applied	delay from instant at which Vin = Vin-min until Vo = 10% of Vo-set)		1.1		ms
Case 2: Input power is applied for at least one second and then the On/Off input is enabled	delay from instant at which Von/Off is enabled until Vo = 10% of Vo-set		700		us
Output voltage Rise time	time for Vo to rise from 10% of Vo-set to 90% of Vo-set		1.5		ms
Output voltage overshoot with or without maximum external capacitance	Ta = 25ºC, Vin = Vin-min to Vin-max, Io = Io-min to Io-max			3.0	%Vout
Over Temperature Protection	(See Thermal Considerations section)		145		°C
PMBus Over Temperature Warning Threshold *			130		°C
Tracking Accuracy	Vin-min to Vom-max, Io-min to Io-max, VSEQ < Vo				
Power-Up: 0.5V/ms				100	mV
Power-Down: 0.5V/ms				100	mV
Input Under Voltage Lockout					
Turn-on Threshold			4.25		Vdc
Turn-off Threshold			3.96		Vdc
Hysteresis			0.25		Vdc
PMBus Adjustable Input Under Voltage Lockout Thresholds		2.5		14	Vdc
Resolution of Adjustable Input Under Voltage Threshold				500	mV
PGOOD (Power Good)					
Signal Interface Open Drain, Vsupply ≤ 5VDC					
Overvoltage threshold for PGOOD ON			108		%Vout
Overvoltage threshold for PGOOD OFF			110		%Vout
Undervoltage threshold for PGOOD ON			92		%Vout
Undervoltage threshold for PGOOD OFF			90		%Vout
Pulldown resistance of PGOOD pin				50	Ω
Sink current capability into PGOOD pin				5	mA

* Over temperature Warning – Warning may not activate before alarm and unit may shutdown before warning.

FGLD12SR6040*A

Data Sheet

4.5-14.4Vdc Input, 40A, 0.45-2.0Vdc Output

Digital Interface Specifications

PARAMETER	NOTES	MIN	TYP	MAX	UNITS
PMBus Signal Interface Characteristics					
Input High Voltage (CLK, DATA)		2.1		3.6	V
Input Low Voltage (CLK, DATA)				0.8	V
Input high level current (CLK, DATA)		-10		10	uA
Input low level current (CLK, DATA)		-10		10	uA
Output Low Voltage (CLK, DATA, SMBALERT#)	I_{OUT}=2mA			0.4	V
Output high level open drain leakage current (DATA, SMBALERT#)	V_{OUT}=3.6V	0		10	uA
Pin capacitance			0.7		pF
PMBus Operating frequency range	Slave Mode	10		400	kHz
Data hold time	Receive Mode	0			nS
	Transmit Mode	300			nS
Data setup time		250			nS
Measurement System Characteristics					
Read delay time		153	192	231	us
Output current measurement range		0		40	A
Output current measurement resolution		62.5			mA
Output current measurement gain accuracy (at 25°C)				±5	%
Output current measurement offset				0.1	A
Vout measurement range		0		2.0	V
Vout measurement resolution			16.25		mV
Vout measurement gain accuracy		-2		2	LSB
Vout measurement offset		-3		3	LSB
Vout measurement accuracy			70		mV
Vin measurement range		0		14.4	V
Vin measurement resolution			32.5		mV
Vin measurement gain accuracy		-2		2	LSB
Vin measurement offset		-5.5		1.4	LSB
Vin measurement accuracy			±3		%

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Data Sheet

4.5-14.4Vdc Input, 40A, 0.45-2.0Vdc Output

Design Considerations

Input Filtering

The **FGLD12SR6040*A** converter should be connected to a low ac-impedance source. A highly inductive source can affect the stability of the module. An input capacitance must be placed directly adjacent to the input pin of the module, to minimize input ripple voltage and ensure module stability.

To minimize input voltage ripple, ceramic capacitors are recommended at the input of the module. Fig-1 shows the input ripple voltage for various output voltages at 40A of load current with 4x47uF, 6x47uF or 8x47uF ceramic capacitors and an input of 12V.

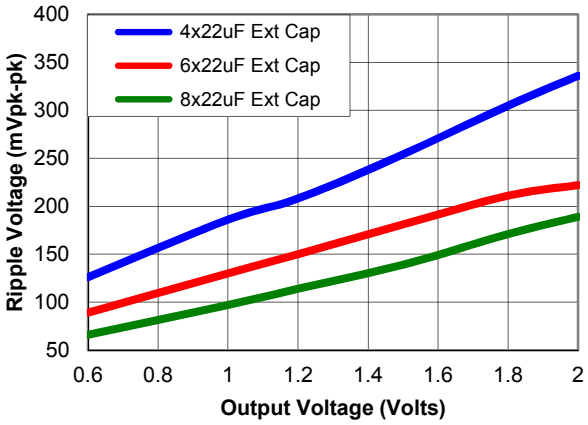


Fig-1: Input ripple voltage for various output voltages with various external ceramic capacitors at the input (40A load). Input voltage is 12V. Scope Bandwidth limited to 20MHz.

Output Filtering

The **FGLD12SR6040*A** is designed for low output ripple voltage and will meet the maximum output ripple specification with 0.1uF ceramic and 47uF ceramic capacitors at the output of the module. However, additional output filtering may be required by the system designer for a number of reasons. First, there may be a need to further reduce the output ripple and noise of the module. Second, the dynamic response characteristics may need to be customized to a particular load step change.

To reduce the output ripple and improve the dynamic response to a step load change, additional capacitance at the output can be used. Low ESR polymer and ceramic capacitors are recommended to improve the dynamic response of the module. Fig-2 provides output ripple information for different external capacitance values at various Vo and a full load current of 40A. For stable operation of the module, limit the capacitance to less than the maximum output capacitance as specified in the electrical specification table. Optimal performance of the module can be achieved by using the Tunable Loop™ feature described later in this data sheet.

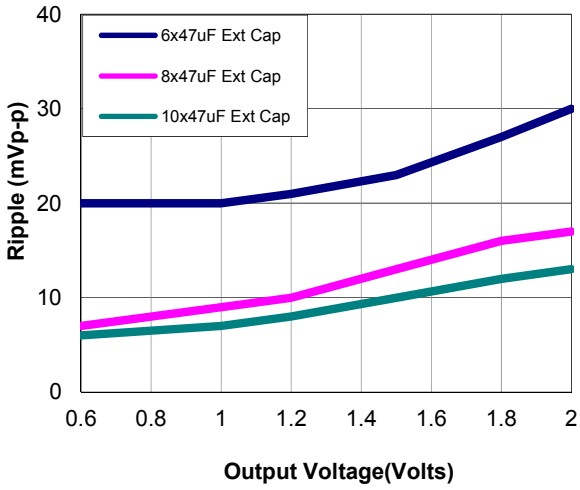


Fig-2: Output ripple voltage for various output voltages with external 6x47uF, 8x47uF or 10x47uF ceramic capacitors at the output (40A load). Input voltage is 12V. Scope Bandwidth limited to 20MHz.

Safety Consideration

For safety agency approval the power module must be installed in compliance with the spacing and separation requirements of the end-use safety agency standards, i.e., UL 60950-1 2nd, CSA C22.2 No. 60950-1-07, DIN EN 60950-1:2006 + A11 (VDE0805 Teil 1 + A11):2009-11; EN 60950-1:2006 + A11:2009-03. (Pending)

For the converter output to be considered meeting the requirements of safety extra-low voltage (SELV), the input must meet SELV requirements. The power module has extra-low voltage (ELV) outputs when all inputs are ELV.

The input to these units is to be provided with a fast acting fuse with a maximum rating of 30A, 100V (for example, Littlefuse 456 series) in the positive input lead.

FGLD12SR6040*A

4.5-14.4Vdc Input, 40A, 0.45-2.0Vdc Output

Data Sheet

Analog Feature Descriptions

Remote On/Off

The module can be turned ON and OFF either by using the ON/OFF pin (Analog interface) or through the PMBus interface (Digital). The module can be configured in a number of ways through the PMBus interface to react to the two ON/OFF inputs:

- Module ON/OFF can be controlled only through the analog interface (digital interface ON/OFF commands are ignored)
- Module ON/OFF can be controlled only through the PMBus interface (analog interface is ignored)
- Module ON/OFF can be controlled by either the analog or digital interface

The default state of the module (as shipped from the factory) is to be controlled by the analog interface only. If the digital interface is to be enabled, or the module is to be controlled only through the digital interface, this change must be made through the PMBus. These changes can be made and written to non-volatile memory on the module so that it is remembered for subsequent use.

Analog ON/OFF

The **FGLD12SR6040*A** power modules feature an On/Off pin for remote On/Off operation. Two On/Off logic options are available. In the Positive Logic On/Off option, (device code suffix “P” - see Ordering Information), the module turns ON during a logic High on the On/Off pin and turns OFF during a logic Low. With the Negative Logic On/Off option, (device code suffix “N” - see Ordering Information), the module turns OFF during logic High and ON during logic Low. The On/Off signal should be always referenced to ground. For either On/Off logic option, leaving the On/Off pin disconnected will turn the module ON when input voltage is present.

For positive logic modules, the circuit configuration for using the On/Off pin is shown in Fig-3.

For negative logic On/Off modules, the circuit configuration is shown in Fig-4.

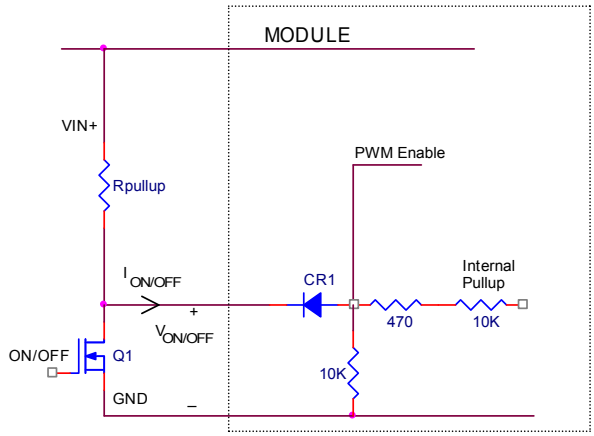


Fig-3: Circuit configuration for using positive On/Off logic.

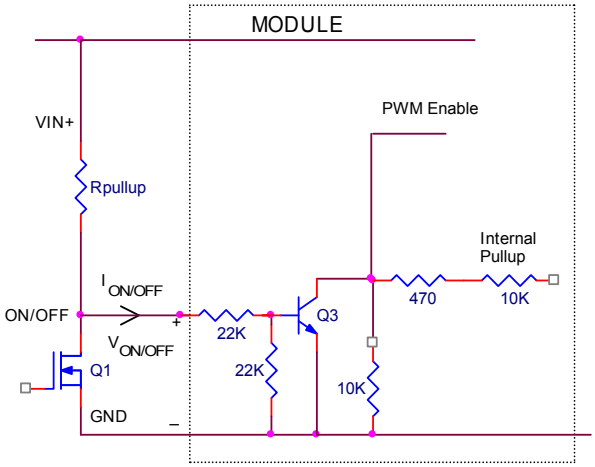


Fig-4: Circuit configuration for using negative On/Off logic.

Digital ON/OFF

Please see the Digital Feature Descriptions section.

Monotonic Start-up and Shut-down

The module has monotonic start-up and shutdown behavior for any combination of rated input voltage, output current and operating temperature range.

Startup into Pre-biased Output

The module can start into a prebiased output as long as the prebias voltage is 0.5V less than the set output voltage.

FGLD12SR6040*A

Data Sheet

4.5-14.4Vdc Input, 40A, 0.45-2.0Vdc Output

Analog Output Voltage Programming

The output voltage of the module is programmable to any voltage from 0.6dc to 2.0Vdc by connecting a resistor between the Trim and SIG_GND pins of the module. Certain restrictions apply on the output voltage set point depending on the input voltage. These are shown in the Output Voltage vs. Input Voltage Set Point Area plot in Fig-5. The Upper Limit curve shows that for output voltages lower than 1V, the input voltage must be lower than the maximum of 14.4V. The Lower Limit curve shows that for output voltages higher than 0.6V, the input voltage needs to be larger than the minimum of 4.5V.

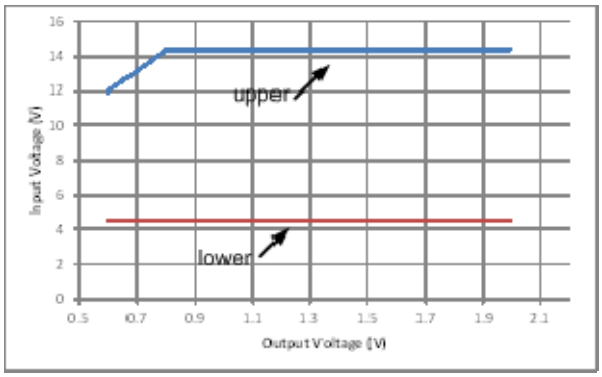
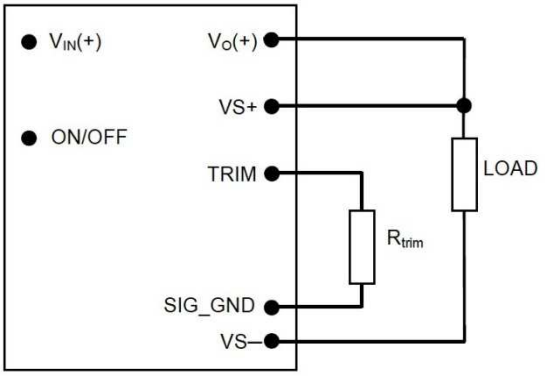


Fig-5: Output Voltage vs. Input Voltage Set Point Area plot showing limits where the output voltage can be set for different input voltages.



Caution *– Do not connect SIG_GND to GND elsewhere in the layout.*

Fig-6: Circuit configuration for programming output voltage using an external resistor.

Without an external resistor between Trim and SIG_GND pins, the output of the module will be 0.6Vdc. To calculate the value of the trim resistor, *Rtrim* for a desired output voltage, should be as per the following equation:

$$R_{TRIM} = \frac{12}{(V_{O\text{-}REQ} - 0.6)} \ [k\,\Omega]$$

Rtrim is the external resistor in kohm
Vo-req is the desired output voltage

Note that the tolerance of a trim resistor will affect the tolerance of the output voltage. Standard 1% or 0.5% resistors may suffice for most applications; however, a tighter tolerance can be obtained by using two resistors in series instead of one standard value resistor.

Table 1 provide Rtrim values required for some common output voltages.

Table 1: Trim Resistor Value

$V_{O\text{-}REG}$ [V]	R_{TRIM} [kΩ]
0.6	Open
0.9	40
1.0	30
1.2	20
1.5	13.33
1.8	10

Digital Output Voltage Adjustment

Please see the Digital Feature Descriptions section.

Remote Sense

The power module has a Remote Sense feature to minimize the effects of distribution losses by regulating the voltage between the sense pins (VS+ and VS-). The voltage drop between the sense pins and the Vout and GND pins of the module should not exceed 0.5V.

Analog Voltage Margining

Output voltage margining can be implemented in the module by connecting a resistor, Rmargin-up, from the Trim pin to the ground pin for margining-up the output voltage and by connecting a resistor, Rmargin-down, from the Trim pin to output pin for margining-down. Fig-7 shows the circuit configuration for output voltage margining. The POL Programming Tool, available at www.fdk.com under the Downloads section, also calculates the values of Rmargin-up and Rmargin-down for a specific output voltage and % margin. Please consult your local FDK FAE for additional details.

FGLD12SR6040*A

4.5-14.4Vdc Input, 40A, 0.45-2.0Vdc Output

Data Sheet

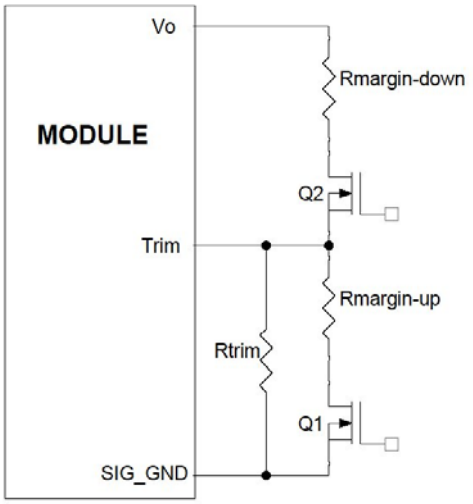


Fig-7: Circuit Configuration for margining Output Voltage.

Digital Output Voltage Margining

Please see the Digital Feature Descriptions section.

Output Voltage Sequencing

The power module includes a sequencing feature, EZSEQUENCE that enables users to implement various types of output voltage sequencing in their applications. This is accomplished via an additional sequencing pin. When not using the sequencing feature, leave it unconnected.

The voltage applied to the SEQ pin should be scaled down by the same ratio as used to scale the output voltage down to the reference voltage of the module. This is accomplished by an external resistive divider connected across the sequencing voltage before it is fed to the SEQ pin as shown in Fig-8. In addition, a small capacitor (suggested value 100pF) should be connected across the lower resistor R1.

For all ***Tomodachi*** modules, the minimum recommended delay between the ON/OFF signal and the sequencing signal is 10ms to ensure that the module output is ramped up according to the sequencing signal. This ensures that the module soft-start routine is completed before the sequencing signal is allowed to ramp up.

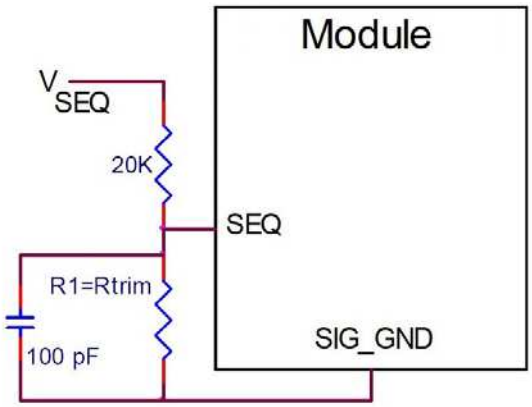


Fig-8: Circuit showing connection of the sequencing signal to the SEQ pin.

When the scaled down sequencing voltage is applied to the SEQ pin, the output voltage tracks this voltage until the output reaches the set-point voltage. The final value of the sequencing voltage must be set higher than the set-point voltage of the module. The output voltage follows the sequencing voltage on a one-to-one basis. By connecting multiple modules together, multiple modules can track their output voltages to the voltage applied on the SEQ pin.

The module's output can track the SEQ pin signal with slopes of up to 0.5V/msec during power-up or power-down.

To initiate simultaneous shutdown of the modules, the SEQ pin voltage is lowered in a controlled manner. The output voltage of the modules tracks the voltages below their set-point voltages on a one-to-one basis. A valid input voltage must be maintained until the tracking and output voltages reach ground potential.

Note that in all digital ***Tomodachi*** series of modules, the PMBus Output Undervoltage Fault will be tripped when sequencing is employed. This will be detected using the STATUS_WORD and STATUS_VOUT PMBus commands. In addition, the SMBALERT# signal will be asserted low as occurs for all faults and warnings. To avoid the module shutting down due to the Output Undervoltage Fault, the module must be set to continue operation without interruption as the response to this fault (see the description of the PMBus command VOUT_UV_FAULT_RESPONSE for additional information).

Over-Current Protection

To provide protection in a fault (output overload) condition, the unit is equipped with internal current-limiting circuitry and can endure current limiting continuously. At the point of current-limit inception, the unit enters hiccup mode. The unit operates normally once the output current is brought back into its specified range.

Digital Adjustable Overcurrent Warning

Please see the Digital Feature Descriptions section.

Over-Temperature Protection

To provide protection in a fault condition, the unit is equipped with a thermal shutdown circuit. The unit will shut down if the over-temperature threshold of 145ºC (typ) is exceeded at the thermal reference point Tref. Once the unit goes into thermal shutdown it will then wait to cool before attempting to restart.

Digital Temperature Status via PMBus

Please see the Digital Feature Descriptions section.

Digitally Adjustable Output Over and Under Voltage Protection

Please see the Digital Feature Descriptions section.

Input Under-Voltage Lockout (UVLO)

At input voltages below the input under-voltage lockout limit, the module operation is disabled. The module will begin to operate at an input voltage above the under-voltage lockout turn-on threshold.

Digitally Adjustable Input Undervoltage Lockout

Please see the Digital Feature Descriptions section.

Digitally Adjustable Power Good Thresholds

Please see the Digital Feature Descriptions section.

Synchronization

The module switching frequency can be synchronized to a signal with an external frequency within a specified range. Synchronization can be done by using the external signal applied to the SYNC pin of the module as shown in Fig-9, with the converter being synchronized by the rising edge of the external signal. The Electrical Specifications table specifies the requirements of the external SYNC signal. If the SYNC pin is not used, the module should free run at the default switching frequency. **If synchronization is not being used, connect the SYNC pin to GND**.

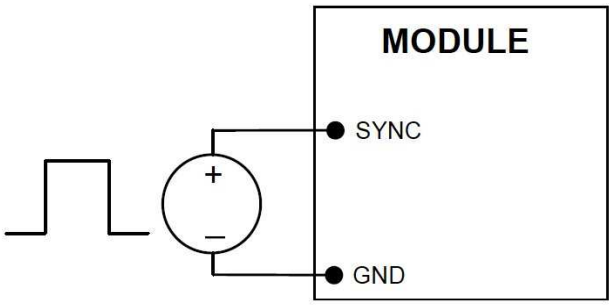


Fig-9: External source connections to synchronize switching frequency of the module.

Paralleling with Active Load Sharing (-P Option)

For additional power requirements, the FGLD12SR6040*A power module is also equipped with paralleling capability. Up to five modules can be configured in parallel, with active load sharing.
To implement paralleling, the following conditions must be satisfied.

- All modules connected in parallel **must** be frequency synchronized where they are switching at the same frequency. This is done by using the SYNC function of the module and connecting to an external frequency source. Modules can be interleaved to reduce input ripple/filtering requirements.
- The share pins of all units in parallel must be connected together. The path of these connections should be as direct as possible.
- The remote sense connections to all modules should be made that to the same points for the output, i.e. all VS+ and VS- terminals for all modules are connected to the power bus at the same points.

Some special considerations apply for design of converters in parallel operation:

- When sizing the number of modules required for parallel operation, take note of the fact that current sharing has some tolerance. In addition, under transient conditions such as a dynamic load change and during startup, all converter output currents will not be equal. To allow for such

variation and avoid the likelihood of a converter shutting off due to a current overload, the total capacity of the paralleled system should be no more than 90% of the sum of the individual converters. As an example, for a system of four FGLS converters in parallel, the total current drawn should be less that 90% of (3 x 40A), i.e. less than 108 A. Similarly, four units can support a load less than 144A.

- All modules should be turned ON and OFF together. This is so that all modules come up at the same time avoiding the problem of one converter sourcing current into the other leading to an overcurrent trip condition. To ensure that all modules come up simultaneously, the on/off pins of all paralleled converters should be tied together and the converters enabled and disabled using the on/off pin. Note that this means that converters in parallel cannot be digitally turned ON as that does not ensure that all modules being paralleled turn on at the same time.
- If digital trimming is used to adjust the overall output voltage, the adjustments need to be made in a series of small steps to avoid shutting down the output. Each step should be no more than 20mV for each module. For example, to adjust the overall output voltage in a setup with two modules (A and B) in parallel from 1V to 1.1V, module A would be adjusted from 1.0 to 1.02V followed by module B from 1.0 to 1.02V, then each module in sequence from 1.02 to 1.04V and so on until the final output voltage of 1.1V is reached.
- If the Sequencing function is being used to start-up and shut down modules and the module is being held to 0V by the tracking signal then there may be small deviations on the module output. This is due to controller duty cycle limitations encountered in trying to hold the voltage down near 0V.
- The share bus is not designed for redundant operation and the system will be non-functional upon failure of one of the units when multiple units are in parallel. In particular, if one of the converters shuts down during operation, the other converters may also shut down due to their outputs hitting current limit. In such a situation, unless a coordinated restart is ensured, the system may never properly restart since different converters will try to restart at different times causing an overload condition and subsequent shutdown. This situation can be avoided by having an external output voltage monitor circuit that detects a shutdown condition and forces all converters to shut down and restart together.

When not using the active load share feature, share pins should be left unconnected.

Measuring Output Current, Output Voltage and Input Voltage

Please see the Digital Feature Descriptions section.

Dual Layout

Identical dimensions and pin layout of Analog and Digital ***Tomodachi*** modules permit migration from one to the other without needing to change the layout. In both cases the trim resistor is connected between trim and signal ground.

Power Good

The module provides a Power Good (PGOOD) signal that is implemented with an open-drain output to indicate that the output voltage is within the regulation limits of the power module. The PGOOD signal will be de-asserted to a low state if any condition such as overtemperature, overcurrent or loss of regulation occurs that would result in the output voltage going ±10% outside the setpoint value. The PGOOD terminal can be connected through a pullup resistor (suggested value 100KΩ) to a source of 5VDC or lower.

Tunable Loop™

The module has a feature that optimizes transient response of the module called Tunable Loop™

External capacitors are usually added to the output of the module for two reasons: to reduce output ripple and noise (see Fig-2) and to reduce output voltage deviations from the steady-state value in the presence of dynamic load current changes. Adding external capacitance however affects the voltage control loop of the module, typically causing the loop to slow down with sluggish response. Larger values of external capacitance could also cause the module to become unstable.

The Tunable Loop™ allows the user to externally adjust the voltage control loop to match the filter network connected to the output of the module. The Tunable Loop™ is implemented by connecting a series R-C between the SENSE and TRIM pins of the module, as shown in Fig-10. This R-C allows the user to externally adjust the voltage loop feedback compensation of the module.

FGLD12SR6040*A

4.5-14.4Vdc Input, 40A, 0.45-2.0Vdc Output

Data Sheet

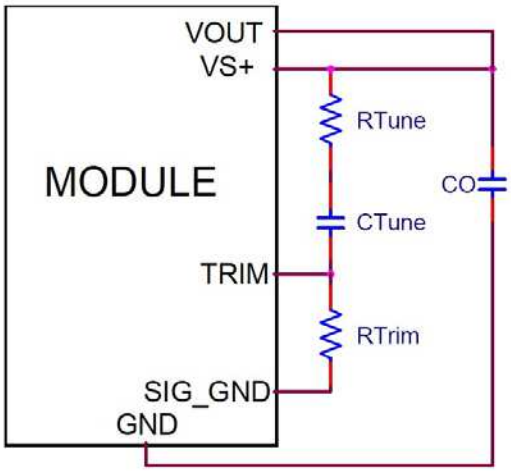


Fig-10: Circuit diagram showing connection of R_{TUNE} and C_{TUNE} to tune the control loop of the module.

Recommended values of R_{TUNE} and C_{TUNE} for different output capacitor combinations are given in Table 2. Table 2 shows the recommended values of R_{TUNE} and C_{TUNE} for different values of ceramic output capacitors up to 1,000uF that might be needed for an application to meet output ripple and noise requirements. Selecting R_{TUNE} and C_{TUNE} according to Table 2 will ensure stable operation of the module.

In applications with tight output voltage limits in the presence of dynamic current loading, additional output capacitance will be required. Table 3 lists recommended values of R_{TUNE} and C_{TUNE} in order to meet 2% output voltage deviation limits for some common output voltages in the presence of a 10A to 40A step change (50% of full load), with an input voltage of 12V.

Please contact your FDK technical representative to obtain more details of this feature as well as for guidelines on how to select the right value of external R-C to tune the module for best transient performance and stable operation for other output capacitance values.

Table 2: General recommended value of R_{TUNE} and C_{TUNE} for Vin=12V and various external ceramic capacitor combinations.

Co	6x47uF	8x47uF	10x47uF	12x47uF	20x47uF
R_{TUNE}	330Ω	330Ω	330Ω	330Ω	200Ω
C_{TUNE}	330pF	820pF	1200pF	1500pF	3300pF

Table 3: Recommended values of R_{TUNE} and C_{TUNE} to obtain transient deviation of 2% of Vout for a 20A step load with Vin=12V.

Vo	1.8V	1.2V	0.6V
Co	4x47uF+ 6x330uF Polymer	4x47uF+ 11x330uF Polymer	4x47uF+ 12x680uF Polymer
R_{TUNE}	220Ω	200 Ω	180 Ω
C_{TUNE}	5600pF	12nF	47nF
△V	34mV	22mV	12mV

Note: The capacitors used in the Tunable Loop tables are 47 uF/3 mΩ ESR ceramic, 330 uF/12 mΩ ESR polymer capacitor and 680uF/12 mΩ polymer capacitor.

FGLD12SR6040*A

Data Sheet

4.5-14.4Vdc Input, 40A, 0.45-2.0Vdc Output

Digital Feature Description

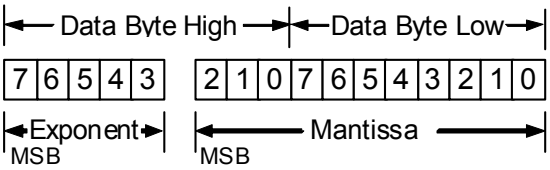
PMBus Interface Capability

The 40A Digital ***Tomodachi*** power modules have a PMBus interface that supports both communication and control. The PMBus Power Management Protocol Specification can be obtained from www.pmbus.org. The modules support a subset of version 1.1 of the specification (see Table 6 for a list of the specific commands supported). Most module parameters can be programmed using PMBus and stored as defaults for later use.

All communication over the module PMBus interface must support the Packet Error Checking (PEC) scheme. The PMBus master must generate the correct PEC byte for all transactions, and check the PEC byte returned by the module.
The module also supports the SMBALERT# response protocol whereby the module can alert the bus master if it wants to talk. For more information on the SMBus alert response protocol, see the System Management Bus (SMBus) specification.
The module has non-volatile memory that is used to store configuration settings. Not all settings programmed into the device are automatically saved into this non-volatile memory, only those specifically identified as capable of being stored can be saved (see Table 6 for which command parameters can be saved to non-volatile storage).

PMBus Data Format

For commands that set thresholds, voltages or report such quantities, the module supports the "Linear" data format among the three data formats supported by PMBus. The Linear Data Format is a two byte value with an 11-bit, two's complement mantissa and a 5-bit, two's complement exponent. The format of the two data bytes is shown below:



The value is of the number is then given by
Value = Mantissa x $2^{Exponent}$

PMBus Addressing

The power module can be addressed through the PMBus using a device address. The module has 64 possible addresses (0 to 63 in decimal) which can be set using resistors connected from the ADDR0 and ADDR1 pins to SIG_GND. Note that some of these addresses (0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11 12, 40, 44, 45, 55 in decimal) are reserved according to the SMBus specifications and may not be useable. The address is set in the form of two octal (0 to 7) digits, with each pin setting one digit. The ADDR1 pin sets the high order digit and ADDR0 sets the low order digit. The resistor values suggested for each digit are shown in Table 4 (1% tolerance resistors are recommended). Note that if either address resistor value is outside the range specified in Table 4, the module will respond to address 127.

Table 4:

Digit	Resistor Value [kΩ]
0	10
1	15.4
2	23.7
3	36.5
4	54.9
5	84.5
6	130
7	200

The user must know which I^2C addresses are reserved in a system for special functions and set the address of the module to avoid interfering with other system operations. Both 100kHz and 400kHz bus speeds are supported by the module. Connection for the PMBus interface should follow the High Power DC specifications given in section 3.1.3 in the SMBus specification V2.0 for the 400kHz bus speed or the Low Power DC specifications in section 3.1.2. The complete SMBus specification is available from the SMBus web site, smbus.org.

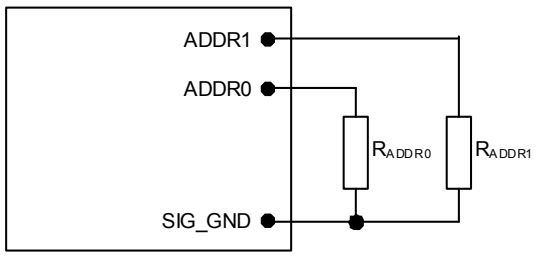


Fig-11: Circuit showing connection of resistors used to set the PMBus address of the module.

PMBus Enabled On/Off

The module can also be turned on and off via the PMBus interface. The OPERATION command is used to actually turn the module on and off via the PMBus, while the ON_OFF_CONFIG command configures the combination of analog ON/OFF pin input and PMBus commands needed to turn the module on and off. Bit [7] in the OPERATION command data byte enables the module, with the following functions:

0 : Output is disabled
1 : Output is enabled

This module uses the lower five bits of the ON_OFF_CONFIG data byte to set various ON/OFF options as follows:

Bit Position	4	3	2	1	0
Access	r/w	r/w	r/w	r/w	r
Function	PU	CMD	CPR	POL	CPA
Default Value	***1***	***0***	***1***	***1***	***1***

PU: Sets the default to either operate any time input power is present or for the ON/OFF to be controlled by the analog ON/OFF input and the PMBus OPERATION command. This bit is used together with the CP, CMD and ON bits to determine startup.

Bit Value	Action
0	Module powers up any time power is present regardless of state of the analog ON/OFF pin
1	Module does not power up until commanded by the analog ON/OFF pin and the OPERATION command as programmed in bits [2:0] of the ON_OFF_CONFIG register.

CMD: The CMD bit controls how the device responds to the OPERATION command.

Bit Value	Action
0	Module ignores the ON bit in the OPERATION command
1	Module responds to the ON bit in the OPERATION command

CPR: Sets the response of the analog ON/OFF pin. This bit is used together with the CMD, PU and ON bits to determine startup.

Bit Value	Action
0	Module ignores the analog ON/OFF pin, i.e. ON/OFF is only controlled through the PMBUS via the OPERATION command
1	Module requires the analog ON/OFF pin to be asserted to start the unit

PMBus Adjustable Soft Start Rise Time

The soft start rise time can be adjusted in the module via PMBus. When setting this parameter, make sure that the charging current for output capacitors can be delivered by the module in addition to any load current to avoid nuisance tripping of the overcurrent protection circuitry during startup. The TON_RISE command sets the rise time in ms, and allows choosing soft start times between 600us and 9ms, with possible values listed in Table 5. Note that the exponent is fixed at -4 (decimal) and the upper two bits of the mantissa are also fixed at 0.

Table 5

Rise Time	Exponent	Mantissa
600us	11100	00000001010
900us	11100	00000001110
1.2ms	11100	00000010011
1.8ms	11100	00000011101
2.7ms	11100	00000101011
4.2ms	11100	00001000011
6.0ms	11100	00001100000
9.0ms	11100	00010010000

Output Voltage Adjustment Using the PMBus

The VOUT_SCALE_LOOP parameter is important for a number of PMBus commands related to output voltage trimming, margining, over/under voltage protection and the PGOOD thresholds. The output voltage of the module is set as the combination of the voltage divider formed by RTrim and a 20kΩ upper divider resistor inside the module, and the internal reference voltage of the module. The reference voltage V_{REF} is nominally set at 600mV, and the output regulation voltage is then given by

$$V_{OUT} = \left[\frac{20000 + RTrim}{RTrim}\right] \times V_{REF}$$

Hence the module output voltage is dependent on the value of RTrim which is connected external to the module. The information on the output voltage divider ratio is conveyed to the module through the VOUT_SCALE_LOOP parameter which is calculated as follows:

$$VOUT\_SCALE\_LOOP = \frac{RTrim}{20000 + RTrim}$$

The VOUT_SCALE_LOOP parameter is specified using the “Linear” format and two bytes. The upper five bits [7:3] of the high byte are used to set the exponent which is fixed at –9 (decimal). The remaining three bits of the high byte [2:0] and the eight bits of the lower byte are used for the mantissa. The default value of

the mantissa is 00100000000 corresponding to 256 (decimal), corresponding to a divider ratio of 0.5. The maximum value of the mantissa is 512 corresponding to a divider ratio of 1. Note that the resolution of the VOUT_SCALE_LOOP command is 0.2%.

When PMBus commands are used to trim or margin the output voltage, the value of V_{REF} is what is changed inside the module, which in turn changes the regulated output voltage of the module.

The nominal output voltage of the module can be adjusted with a minimum step size of 0.4% over a ±25% range from nominal using the VOUT_TRIM command over the PMBus.

The VOUT_TRIM command is used to apply a fixed offset voltage to the output voltage command value using the "Linear" mode with the exponent fixed at –10 (decimal). The value of the offset voltage is given by

$$V_{OUT(offset)} = VOUT\_TRIM \times 2^{-10}$$

This offset voltage is added to the voltage set through the divider ratio and nominal VREF to produce the trimmed output voltage. The valid range in two's complement for this command is –4000h to 3999h. The high order two bits of the high byte must both be either 0 or 1. If a value outside of the +/-25% adjustment range is given with this command, the module will set it's output voltage to the nominal value (as if VOUT_TRIM had been set to 0), assert SMBALRT#, set the CML bit in STATUS_BYTE and the invalid data bit in STATUS_CML.

Output Voltage Margining Using the PMBus

The module can also have its output voltage margined via PMBus commands. The command VOUT_MARGIN_HIGH sets the margin high voltage, while the command VOUT_MARGIN_LOW sets the margin low voltage. Both the VOUT_MARGIN_HIGH and VOUT_MARGIN_LOW commands use the "Linear" mode with the exponent fixed at –10 (decimal). Two bytes are used for the mantissa with the upper bit [7] of the high byte fixed at 0. The actual margined output voltage is a combination of the VOUT_MARGIN_HIGH or VOUT_MARGIN_LOW and the VOUT_TRIM values as shown below.

$$V_{OUT(MH)} = (VOUT\_MARGIN\_HIGH + VOUT\_TRIM) \times 2^{-10}$$

$$V_{OUT(ML)} = (VOUT\_MARGIN\_LOW + VOUT\_TRIM) \times 2^{-10}$$

Note that the sum of the margin and trim voltages cannot be outside the ±25% window around the nominal output voltage. The data associated with VOUT_MARGIN_HIGH and VOUT_MARGIN_LOW can be stored to non-volatile memory using the STORE_DEFAULT_ALL command.

The module is commanded to go to the margined high or low voltages using the OPERATION command. Bits [5:2] are used to enable margining as follows:

00XX : Margin Off
0101 : Margin Low (Ignore Fault)
0110 : Margin Low (Act on Fault)
1001 : Margin High (Ignore Fault)
1010 : Margin High (Act on Fault)

PMBus Adjustable Overcurrent Warning

The module can provide an overcurrent warning via the PMBus. The threshold for the overcurrent warning can be set using the parameter IOUT_OC_WARN_LIMIT. This command uses the "Linear" data format with a two byte data word where the upper five bits [7:3] of the high byte represent the exponent and the remaining three bits of the high byte [2:0] and the eight bits in the low byte represent the mantissa. The exponent is fixed at –1 (decimal). The upper four bits of the mantissa are fixed at 0 while the lower seven bits are programmable with a default value of 55.5A (decimal). For production codes after April 2013, the value for IOUT_OC_WARN_LIMIT will be fixed at 57A. For earlier production codes the actual value for IOUT_OC_WARN_LIMIT will vary from module to module due to calibration during production testing. The resolution of this warning limit is 500mA. The value of the IOUT_OC_WARN_LIMIT can be stored to non-volatile memory using the STORE_DEFAULT_ALL command.

Temperature Status via PMBus

The module can provide information related to temperature of the module through the STATUS_TEMPERATURE command. The command returns information about whether the pre-set over temperature fault threshold and/or the warning threshold have been exceeded.

PMBus Adjustable Output Over and Under Voltage Protection

The module has output over and under voltage protection capability. The PMBus command VOUT_OV_FAULT_LIMIT is used to set the output over voltage threshold from four possible values: 108%, 110%, 112% or 115% of the commanded output voltage. The command

VOUT_UV_FAULT_LIMIT sets the threshold that causes an output under voltage fault and can also be selected from four possible values: 92%, 90%, 88% or 85%. The default values are 112% and 88% of commanded output voltage. Both commands use two data bytes formatted as two's complement binary integers. The "Linear" mode is used with the exponent fixed to –10 (decimal) and the effective over or under voltage trip points given by:

$$V_{OUT(OV\_REQ)} = (VOUT\_OV\_FAULT\_LIMIT) \times 2^{-10}$$

$$V_{OUT(UV\_REQ)} = (VOUT\_UV\_FAULT\_LIMIT) \times 2^{-10}$$

Values within the supported range for over and undervoltage detection thresholds will be set to the nearest fixed percentage. Note that the correct value for VOUT_SCALE_LOOP must be set in the module for the correct over or under voltage trip points to be calculated.

In addition to adjustable output voltage protection, the 40A Digital ***Tomodachi*** module can also be programmed for the response to the fault. The VOUT_OV_FAULT_RESPONSE and VOUT_UV_FAULT_RESPONSE commands specify the response to the fault. Both these commands use a single data byte with the possible options as shown below.

1. Continue operation without interruption (Bits [7:6] = 00, Bits [5:3] = xxx)
2. Continue for four switching cycles and then shut down if the fault is still present, followed by no restart or continuous restart (Bits [7:6] = 01, Bits [5:3] = 000 means no restart, Bits [5:3] = 111 means continuous restart)
3. Immediate shut down followed by no restart or continuous restart (Bits [7:6] = 10, Bits [5:3] = 000 means no restart, Bits [5:3] = 111 means continuous restart).
4. Module output is disabled when the fault is present and the output is enabled when the fault no longer exists (Bits [7:6] = 11, Bits [5:3] = xxx).

Note that separate response choices are possible for output over voltage or under voltage faults.

PMBus Adjustable Input Undervoltage Lockout

The module allows adjustment of the input under voltage lockout and hysteresis. The command VIN_ON allows setting the input voltage turn on threshold, while the VIN_OFF command sets the input voltage turn off threshold. For the VIN_ON command, possible values are 3.5V to 14V in 0.5V steps. For the VIN_OFF command, possible values are 3V to 14V in 0.5V steps. If other values are entered for either command, they will be mapped to the closest of the allowed values.

Both the VIN_ON and VIN_OFF commands use the "Linear" format with two data bytes. The upper five bits represent the exponent (fixed at -2) and the remaining 11 bits represent the mantissa. For the mantissa, the four most significant bits are fixed at 0.

Power Good

The module provides a Power Good (PGOOD) signal that is implemented with an open-drain output to indicate that the output voltage is within the regulation limits of the power module. The PGOOD signal will be de-asserted to a low state if any condition such as overtemperature, overcurrent or loss of regulation occurs that would result in the output voltage going outside the specified thresholds. The PGOOD thresholds are user selectable via the PMBus (the default values are as shown in the Feature Specifications Section). Each threshold is set up symmetrically above and below the nominal value. The POWER_GOOD_ON command sets the output voltage level above which PGOOD is asserted (lower threshold). For example, with a 1.2V nominal output voltage, the POWER_GOOD_ON threshold can set the lower threshold to 1.14 or 1.1V. Doing this will automatically set the upper thresholds to 1.26 or 1.3V.

The POWER_GOOD_OFF command sets the level below which the PGOOD command is de-asserted. This command also sets two thresholds symmetrically placed around the nominal output voltage. Normally, the POWER_GOOD_ON threshold is set higher than the POWER_GOOD_OFF threshold.

Both POWER_GOOD_ON and POWER_GOOD_OFF commands use the "Linear" format with the exponent fixed at –10 (decimal). The two thresholds are given by

$$V_{OUT(PGOOD\_ON)} = (POWER\_GOOD\_ON) \times 2^{-10}$$

$$V_{OUT(PGOOD\_OFF)} = (POWER\_GOOD\_OFF) \times 2^{-10}$$

Both commands use two data bytes with bit [7] of the high byte fixed at 0, while the remaining bits are r/w and used to set the mantissa using two's complement representation. Both commands also use the VOUT_SCALE_LOOP parameter so it must be set correctly. The default value of POWER_GOOD_ON is set at 1.1035V and that of the POWER_GOOD_OFF is set at 1.08V. The values associated with these commands can be stored in non-volatile memory using the STORE_DEFAULT_ALL command.

The PGOOD terminal can be connected through a pullup resistor (suggested value 100KΩ) to a source of 5VDC or lower.

Measurement of Output Current, Output Voltage and Input Voltage

The module is capable of measuring key module parameters such as output current and voltage and input voltage and providing this information through the PMBus interface. Roughly every 200us, the module makes 16 measurements each of output current, voltage and input voltage. Average values of of these 16 measurements are then calculated and placed in the appropriate registers. The values in the registers can then be read using the PMBus interface.

Measuring Output Current Using the PMBus

The module measures current by using the inductor winding resistance as a current sense element. The inductor winding resistance is then the current gain factor used to scale the measured voltage into a current reading. This gain factor is the argument of the IOUT_CAL_GAIN command, and consists of two bytes in the linear data format. The exponent uses the upper five bits [7:3] of the high data byte in two-s complement format and is fixed at –15 (decimal). The remaining 11 bits in two's complement binary format represent the mantissa. During manufacture, each module is calibrated by measuring and storing the current gain factor into non-volatile storage.

The current measurement accuracy is also improved by each module being calibrated during manufacture with the offset in the current reading. The IOUT_CAL_OFFSET command is used to store and read the current offset. The argument for this command consists of two bytes composed of a 5-bit exponent (fixed at -4d) and a 11-bit mantissa. This command has a resolution of 62.5mA and a range of -4000mA to +3937.5mA.

The READ_IOUT command provides module average output current information. This command only supports positive or current sourced from the module. If the converter is sinking current a reading of 0 is provided. The READ_IOUT command returns two bytes of data in the linear data format. The exponent uses the upper five bits [7:3] of the high data byte in two-s complement format and is fixed at –4 (decimal). The remaining 11 bits in two's complement binary format represent the mantissa with the 11th bit fixed at 0 since only positive numbers are considered valid.

Note that the current reading provided by the module is not corrected for temperature. The temperature corrected current reading for module temperature T_{Module} can be estimated using the following equation.

$$I_{OUT,CORR} = \frac{I_{READ\_OUT}}{1+[(T_{IND}-30)\times 0.00393]}$$

where I_{OUT_CORR} is the temperature corrected value of the current measurement, I_{READ_OUT} is the module current measurement value, T_{IND} is the temperature of the inductor winding on the module. Since it may be difficult to measure T_{IND}, it may be approximated by an estimate of the module temperature.

Measuring Output Voltage Using the PMBus

The module can provide output voltage information using the READ_VOUT command. The command returns two bytes of data all representing the mantissa while the exponent is fixed at -10 (decimal).

During manufacture of the module, offset and gain correction values are written into the non-volatile memory of the module. The command VOUT_CAL_OFFSET can be used to read and/or write the offset (two bytes consisting of a 16-bit mantissa in two's complement format) while the exponent is always fixed at -10 (decimal). The allowed range for this offset correction is -125 to 124mV. The command VOUT_CAL_GAIN can be used to read and/or write the gain correction - two bytes consisting of a five-bit exponent (fixed at -8) and a 11-bit mantissa. The range of this correction factor is -0.125V to +0.121V, with a resolution of 0.004V. The corrected output voltage reading is then given by:

$$V_{OUT}(Final) = [V_{OUT}(Initial)\times(1+VOUT\_CAL\_GAIN)] + VOUT\_CAL\_OFFSET$$

Measuring Input Voltage Using the PMBus

The module can provide output voltage information using the READ_VIN command. The command returns two bytes of data in the linear format. The upper five bits [7:3] of the high data form the two's complement representation of the mantissa which is fixed at –5 (decimal). The remaining 11 bits are used for two's complement representation of the mantissa, with the 11th bit fixed at zero since only positive numbers are valid.

During module manufacture, offset and gain correction values are written into the non-volatile memory of the module. The command VIN_CAL_OFFSET can be used to read and/or write the offset - two bytes consisting of a five-bit exponent (fixed at -5) and a 11-bit mantissa in two's complement format. The allowed range for this offset correction is -2 to 1.968V, and the resolution is 32mV. The command VIN_CAL_GAIN can be used to read and/or write the gain correction - two bytes consisting of a five-bit exponent (fixed at -8) and a 11-bit mantissa. The range of this correction factor is -0.125V to +0.121V, with a resolution of

0.004V. The corrected output voltage reading is then given by:

$$V_{IN}(Final) = [V_{IN}(Initial) \times (1 + VIN\_CAL\_GAIN)] + VIN\_CAL\_OFFSET$$

Reading the Status of the Module using the PMBus

The module supports a number of PMBus status information commands. However, not all features are supported in these commands. A 1 in the bit position indicates the fault that is flagged.

STATUS_BYTE: Returns one byte of information with a summary of the most critical device faults.

Bit Position	Flag	Default Value
7	X	0
6	OFF	0
5	VOUT Overvoltage	0
4	IOUT Overcurrent	0
3	VIN Undervoltage	0
2	Temperature	0
1	CML (Comm. Memory Fault)	0
0	None of the above	0

STATUS_WORD: Returns two bytes of information with a summary of the module's fault/warning conditions.

Low Byte

Bit Position	Flag	Default Value
7	X	0
6	OFF	0
5	VOUT Overvoltage	0
4	IOUT Overcurrent	0
3	VIN Undervoltage	0
2	Temperature	0
1	CML (Comm. Memory Fault)	0
0	None of the above	0

High Byte

Bit Position	Flag	Default Value
7	VOUT fault or warning	0
6	IOUT fault or warning	0
5	X	0
4	X	0
3	POWER_GOOD# (is negated)	0
2	X	0
1	X	0
0	X	0

STATUS_VOUT: Returns one byte of information relating to the status of the module's output voltage related faults.

Bit Position	Flag	Default Value
7	VOUT OV Fault	0
6	X	0
5	X	0
4	VOUT UV Fault	0
3	X	0
2	X	0
1	X	0
0	X	0

STATUS_IOUT: Returns one byte of information relating to the status of the module's output voltage related faults.

Bit Position	Flag	Default Value
7	IOUT OC Fault	0
6	X	0
5	IOUT OC Warning	0
4	X	0
3	X	0
2	X	0
1	X	0
0	X	0

STATUS_TEMPERATURE: Returns one byte of information relating to the status of the module's temperature related faults.

Bit Position	Flag	Default Value
7	OT Fault	0
6	OT Warning	0
5	X	0
4	X	0
3	X	0
2	X	0
1	X	0
0	X	0

STATUS_CML: Returns one byte of information relating to the status of the module's communication related faults.

Bit Position	Flag	Default Value
7	Invalid/Unsupported Command	0
6	Invalid/Unsupported Command	0
5	Packet Error Check Failed	0
4	X	0
3	X	0
2	X	0
1	Other Communication Fault	0
0	X	0

MFR_VIN_MIN: Returns minimum input voltage as two data bytes of information in Linear format (upper five bits are exponent – fixed at -2, and lower 11 bits are mantissa in two's complement format – fixed at 12)

MFR_VOUT_MIN: Returns minimum output voltage as two data bytes of information in Linear format (upper five bits are exponent – fixed at -10, and lower 11 bits are mantissa in two's complement format – fixed at 614)

MFR_SPECIFIC_00: Returns information related to the type of module. Bits [7:2] in the Low Byte indicate the module type (000100 corresponds to the FGLD12SR6040 module). Bit [1:0] in the High Byte are used to indicate the manufacturer ID, with 01 reserved for FDK.

Low Byte

Bit Position	Flag	Default Value
7:2	Module Name	000100
1:0	Reserved	10

High Byte

Bit Position	Flag	Default Value
7:2	Module Revision Number	None
1:0	Manufacturer ID	01

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Data Sheet

4.5-14.4Vdc Input, 40A, 0.45-2.0Vdc Output

Summary of Supported PMBus Commands

Please refer to the PMBus 1.1 specification for more details of these commands.

Table 6

<table>
<tr><th>Hex Code</th><th>Command</th><th>Brief Description</th><th>Non-Volatile Memory Storage</th></tr>
<tr><td>01</td><td>OPERATION</td><td>Turn Module on or off. Also used to margin the output voltage
<table>
<tr><td>Format</td><td colspan="8">Unsigned Binary</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r/w</td><td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r</td><td>r</td></tr>
<tr><td>Function</td><td>On</td><td>X</td><td colspan="4">Margin</td><td>X</td><td>X</td></tr>
<tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>X</td><td>X</td></tr>
</table></td><td></td></tr>
<tr><td>02</td><td>ON_OFF_CONFIG</td><td>Configures the ON/OFF functionality as a combination of analog ON/OFF pin and PMBus commands
<table>
<tr><td>Format</td><td colspan="8">Unsigned Binary</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r</td></tr>
<tr><td>Function</td><td>X</td><td>X</td><td>X</td><td>pu</td><td>cmd</td><td>cpr</td><td>pol</td><td>cpa</td></tr>
<tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
</table></td><td>YES</td></tr>
<tr><td>03</td><td>CLEAR_FAULTS</td><td>Clear any fault bits that may have been set, also releases the SMBALERT# signal if the device has been asserting it.</td><td></td></tr>
<tr><td>10</td><td>WRITE_PROTECT</td><td>Used to control writing to the module via PMBus. Copies the current register setting in the module whose command code matches the value in the data byte into non-volatile memory (EEPROM) on the module
<table>
<tr><td>Format</td><td colspan="8">Unsigned Binary</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r/w</td><td>r/w</td><td>r/w</td><td>x</td><td>x</td><td>x</td><td>x</td><td>x</td></tr>
<tr><td>Function</td><td>bit7</td><td>bit6</td><td>bit5</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>X</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
</table>
Bit5: 0 – Enables all writes as permitted in bit6 or bit7
1 – Disables all writes except the WRITE_PROTECT, OPERATION and ON_OFF_CONFIG (bit 6 and bit7 must be 0)
Bit 6: 0 – Enables all writes as permitted in bit5 or bit7
1 – Disables all writes except for the WRITE_PROTECT and OPERATION commands (bit5 and bit7 must be 0)
Bit7: 0 – Enables all writes as permitted in bit5 or bit6
1 – Disables all writes except for the WRITE_PROTECT command (bit5 and bit6 must be 0)</td><td>YES</td></tr>
<tr><td>11</td><td>STORE_DEFAULT_ALL</td><td>Copies all current register settings in the module into non-volatile memory (EEPROM) on the module. Takes about 50ms for the command to execute.</td><td></td></tr>
<tr><td>12</td><td>RESTORE_DEFAULT_ALL</td><td>Restores all current register settings in the module from values in the module non-volatile memory (EEPROM)</td><td></td></tr>
<tr><td>13</td><td>STORE_DEFAULT_CODE</td><td>Copies the current register setting in the module whose command code matches the value in the data byte into non-volatile memory (EEPROM) on the module
<table>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>w</td><td>w</td><td>w</td><td>w</td><td>w</td><td>w</td><td>w</td><td>w</td></tr>
<tr><td>Function</td><td colspan="8">Command code</td></tr>
</table></td><td></td></tr>
<tr><td>14</td><td>RESTORE_DEFAULT_CODE</td><td>Restores the current register setting in the module whose command code matches the value in the data byte from the value in the module non-volatile memory (EEPROM)
<table>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>w</td><td>w</td><td>w</td><td>w</td><td>w</td><td>w</td><td>w</td><td>w</td></tr>
<tr><td>Function</td><td colspan="8">Command code</td></tr>
</table></td><td></td></tr>
<tr><td>20</td><td>VOUT_MODE</td><td>The module has MODE set to Linear and Exponent set to -10. These values cannot be changed
<table>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr>
<tr><td>Function</td><td colspan="3">Mode</td><td colspan="5">Exponent</td></tr>
<tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
</table></td><td></td></tr>
</table>

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4.5-14.4Vdc Input, 40A, 0.45-2.0Vdc Output

Data Sheet

Table 6 (continued)

<table>
<tr><th>Hex Code</th><th>Command</th><th>Brief Description</th><th>Non-Volatile Memory Storage</th></tr>
<tr><td>22</td><td>VOUT_TRIM</td><td>Apply a fixed offset voltage to the output voltage command value. Exponent is fixed at -10.
<table>
<tr><td>Format</td><td colspan="8">Linear, two’s complement binary</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr>
<tr><td>Function</td><td colspan="8">High Byte</td></tr>
<tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr>
<tr><td>Function</td><td colspan="8">Low Byte</td></tr>
<tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table></td><td>YES</td></tr>
<tr><td>25</td><td>VOUT_MARGIN_HIGH</td><td>Sets the target voltage for margining the output high. Exponent is fixed at -10.
<table>
<tr><td>Format</td><td colspan="8">Linear, two’s complement binary</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr>
<tr><td>Function</td><td colspan="8">High Byte</td></tr>
<tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr>
<tr><td>Function</td><td colspan="8">Low Byte</td></tr>
<tr><td>Default Value</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
</table></td><td>YES</td></tr>
<tr><td>26</td><td>VOUT_MARGIN_LOW</td><td>Sets the target voltage for margining the output low. Exponent is fixed at -10
<table>
<tr><td>Format</td><td colspan="8">Linear, two’s complement binary</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr>
<tr><td>Function</td><td colspan="8">High Byte</td></tr>
<tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr>
<tr><td>Function</td><td colspan="8">Low Byte</td></tr>
<tr><td>Default Value</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
</table></td><td>YES</td></tr>
<tr><td>29</td><td>VOUT_SCALE_LOOP</td><td>Sets the scaling of the output voltage – equal to the feedback resistor divider ratio
<table>
<tr><td>Format</td><td colspan="8">Linear, two’s complement binary</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r/w</td><td>r/w</td></tr>
<tr><td>Function</td><td colspan="5">Exponent</td><td colspan="3">Mantissa</td></tr>
<tr><td>Default Value</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr>
<tr><td>Function</td><td colspan="8">Mantissa</td></tr>
<tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table></td><td>YES</td></tr>
<tr><td>35</td><td>VIN_ON</td><td>Sets the value of input voltage at which the module turns on
<table>
<tr><td>Format</td><td colspan="8">Linear, two’s complement binary</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr>
<tr><td>Function</td><td colspan="5">Exponent</td><td colspan="3">Mantissa</td></tr>
<tr><td>Default Value</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr>
<tr><td>Function</td><td colspan="8">Mantissa</td></tr>
<tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td></tr>
</table></td><td>YES</td></tr>
</table>

FGLD12SR6040*A

4.5-14.4Vdc Input, 40A, 0.45-2.0Vdc Output

Data Sheet

Table 6 (continued)

<table>
<tr><th>Hex Code</th><th>Command</th><th>Brief Description</th><th>Non-Volatile Memory Storage</th></tr>
<tr><td>36</td><td>VIN_OFF</td><td>Sets the value of input voltage at which the module turns off
<table>
<tr><td>Format</td><td colspan="8">Linear, two's complement binary</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr>
<tr><td>Function</td><td colspan="5">Exponent</td><td colspan="3">Mantissa</td></tr>
<tr><td>Default Value</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr>
<tr><td>Function</td><td colspan="8">Mantissa</td></tr>
<tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
</table></td><td>YES</td></tr>
<tr><td>38</td><td>IOUT_CAL_GAIN</td><td>Returns the value of the gain correction term used to correct the measured output current
<table>
<tr><td>Format</td><td colspan="8">Linear, two's complement binary</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r/w</td></tr>
<tr><td>Function</td><td colspan="5">Exponent</td><td colspan="3">Mantissa</td></tr>
<tr><td>Default Value</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr>
<tr><td>Function</td><td colspan="8">Mantissa</td></tr>
<tr><td>Default Value</td><td colspan="8">V: Variable based on factory calibration</td></tr>
</table></td><td>YES</td></tr>
<tr><td>39</td><td>IOUT_CAL_OFFSET</td><td>Returns the value of the offset correction term used to correct the measured output current
<table>
<tr><td>Format</td><td colspan="8">Linear, two's complement binary</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r/w</td><td>r</td><td>r</td></tr>
<tr><td>Function</td><td colspan="5">Exponent</td><td colspan="3">Mantissa</td></tr>
<tr><td>Default Value</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r</td><td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr>
<tr><td>Function</td><td colspan="8">Mantissa</td></tr>
<tr><td>Default Value</td><td colspan="8">V: Variable based on factory calibration</td></tr>
</table></td><td>YES</td></tr>
<tr><td>40</td><td>VOUT_OV_FAULT_LIMIT</td><td>Sets the voltage level for an output overvoltage fault. Exponent is fixed at -10.
<table>
<tr><td>Format</td><td colspan="8">Linear, two's complement binary</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr>
<tr><td>Function</td><td colspan="8">High Byte</td></tr>
<tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr>
<tr><td>Function</td><td colspan="8">Low Byte</td></tr>
<tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
</table></td><td>YES</td></tr>
<tr><td>41</td><td>VOUT_OV_FAULT_RESPONSE</td><td>Instructs the module on what action to take in response to a output overvoltage fault
<table>
<tr><td>Format</td><td colspan="8">Unsigned Binary</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r</td><td>r</td><td>r</td></tr>
<tr><td>Function</td><td>RSP [1]</td><td>RSP [0]</td><td>RS[2]</td><td>RS[1]</td><td>RS[0]</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>Default Value</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td></tr>
</table></td><td>YES</td></tr>
</table>

FGLD12SR6040*A

4.5-14.4Vdc Input, 40A, 0.45-2.0Vdc Output

Data Sheet

Table 6 (continued)

<table>
<tr><th>Hex Code</th><th>Command</th><th>Brief Description</th><th>Non-Volatile Memory Storage</th></tr>
<tr><td>44</td><td>VOUT_UV_FAULT_LIMIT</td><td>Sets the voltage level for an output undervoltage fault. Exponent is fixed at -10.
<table>
<tr><td>Format</td><td colspan="8">Linear, two's complement binary</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr>
<tr><td>Function</td><td colspan="8">High Byte</td></tr>
<tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr>
<tr><td>Function</td><td colspan="8">Low Byte</td></tr>
<tr><td>Default Value</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr>
</table></td><td>YES</td></tr>
<tr><td>45</td><td>VOUT_UV_FAULT_RESPONSE</td><td>Instructs the module on what action to take in response to a output undervoltage fault
<table>
<tr><td>Format</td><td colspan="8">Unsigned Binary</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r</td><td>r</td><td>r</td></tr>
<tr><td>Function</td><td>RSP [1]</td><td>RSP [0]</td><td>RS[2]</td><td>RS[1]</td><td>RS[0]</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
</table></td><td>YES</td></tr>
<tr><td>46</td><td>IOUT_OC_FAULT_LIMIT</td><td>Sets the output overcurrent fault level in A (cannot be changed)
<table>
<tr><td>Format</td><td colspan="8">Linear, two's complement binary</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr>
<tr><td>Function</td><td colspan="5">Exponent</td><td colspan="3">Mantissa</td></tr>
<tr><td>Default Value</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr>
<tr><td>Function</td><td colspan="8">Mantissa</td></tr>
<tr><td>Default Value</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
</table></td><td>YES</td></tr>
<tr><td>4A</td><td>IOUT_OC_WARN_LIMIT</td><td>Sets the output overcurrent warning level in A
<table>
<tr><td>Format</td><td colspan="8">Linear, two's complement binary</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr>
<tr><td>Function</td><td colspan="5">Exponent</td><td colspan="3">Mantissa</td></tr>
<tr><td>Default Value</td><td>1</td><td>1</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr>
<tr><td>Function</td><td colspan="8">Mantissa</td></tr>
<tr><td>Default Value</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
</table></td><td>YES</td></tr>
<tr><td>5E</td><td>POWER_GOOD_ON</td><td>Sets the output voltage level at which the PGOOD pin is asserted high. Exponent is fixed at -10.
<table>
<tr><td>Format</td><td colspan="8">Linear, two's complement binary</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr>
<tr><td>Function</td><td colspan="8">High Byte</td></tr>
<tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr>
<tr><td>Function</td><td colspan="8">Low Byte</td></tr>
<tr><td>Default Value</td><td>0</td><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
</table></td><td>YES</td></tr>
</table>

FGLD12SR6040*A

4.5-14.4Vdc Input, 40A, 0.45-2.0Vdc Output

Data Sheet

Table 6 (continued)

<table>
<tr><th>Hex Code</th><th>Command</th><th>Brief Description</th><th>Non-Volatile Memory Storage</th></tr>
<tr><td>5F</td><td>POWER_GOOD_OFF</td><td>Sets the output voltage level at which the PGOOD pin is de-asserted low. Exponent is fixed at -10.
<table>
<tr><td>Format</td><td colspan="8">Linear, two's complement binary</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr>
<tr><td>Function</td><td colspan="8">High Byte</td></tr>
<tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr>
<tr><td>Function</td><td colspan="8">Low Byte</td></tr>
<tr><td>Default Value</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
</table></td><td>YES</td></tr>
<tr><td>61</td><td>TON_RISE</td><td>Sets the rise time of the output voltage during startup
<table>
<tr><td>Format</td><td colspan="8">Linear, two's complement binary</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r/w</td></tr>
<tr><td>Function</td><td colspan="5">Exponent</td><td colspan="3">Mantissa</td></tr>
<tr><td>Default Value</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td><td>r/w</td></tr>
<tr><td>Function</td><td colspan="8">Mantissa</td></tr>
<tr><td>Default Value</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
</table></td><td>YES</td></tr>
<tr><td>78</td><td>STATUS_BYTE</td><td>Returns one byte of information with a summary of the most critical module faults
<table>
<tr><td>Format</td><td colspan="8">Unsigned Binary</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr>
<tr><td>Flag</td><td>X</td><td>OFF</td><td>VOUT_OV</td><td>IOUT_OC</td><td>VIN_UV</td><td>TEMP</td><td>CML</td><td>OTHER</td></tr>
<tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table></td><td></td></tr>
<tr><td>79</td><td>STATUS_WORD</td><td>Returns two bytes of information with a summary of the module's fault/warning conditions
<table>
<tr><td>Format</td><td colspan="8">Unsigned binary</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr>
<tr><td>Flag</td><td>VOUT</td><td>IOUT_OC</td><td>X</td><td>X</td><td>PGOOD</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr>
<tr><td>Flag</td><td>X</td><td>OFF</td><td>VOUT_OV</td><td>IOUT_OC</td><td>VIN_UV</td><td>TEMP</td><td>CML</td><td>OTHER</td></tr>
<tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table></td><td></td></tr>
<tr><td>7A</td><td>STATUS_VOUT</td><td>Returns one byte of information with the status of the module's output voltage related faults
<table>
<tr><td>Format</td><td colspan="8">Unsigned Binary</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr>
<tr><td>Flag</td><td>VOUT_OV</td><td>X</td><td>X</td><td>VOUT_UV</td><td>X</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table></td><td></td></tr>
<tr><td>7B</td><td>STATUS_IOUT</td><td>Returns one byte of information with the status of the module's output current related faults
<table>
<tr><td>Format</td><td colspan="8">Unsigned Binary</td></tr>
<tr><td>Bit Position</td><td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr>
<tr><td>Access</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td><td>r</td></tr>
<tr><td>Flag</td><td>IOUT_OC</td><td>X</td><td>X</td><td>X</td><td>IOUT_OC_WARN</td><td>X</td><td>X</td><td>X</td></tr>
<tr><td>Default Value</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr>
</table></td><td></td></tr>
</table>