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# FHP3130, FHP3230, FHP3430

## Single, Dual, and Quad, High-Speed, 2.7V to 12V, Rail-to-Rail Amplifiers

### Features at ±5V

- 2.5mA supply current per amplifier
- 0.008%/0.01° differential gain/phase
- 10MHz 0.1dB bandwidth
- Output voltage range at  $R_L = 150\Omega$ : -4.8V to 4.8V
- Input includes negative rail
- 110V/ $\mu$ s slew rate
- ±100mA output current
- 17nV/ $\sqrt{\text{Hz}}$  input voltage noise
- >100dB PSRR, CMRR, and open-loop gain
- FHP3130 – improved replacement for KM4100
- FHP3230 – improved replacement for KM4200
- FHP3130 lead-free package options (SOT23-5, SOIC-8)
- FHP3230 lead-free package options (MSOP-8, SOIC-8)
- FHP3430 lead-free package options (TSSOP-14, SOIC-14)
- RoHS compliant
- Fully specified at +3V, +5V, and ±5V supplies

### Applications

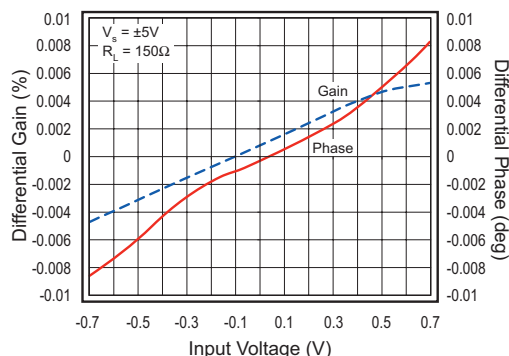
- A/D driver
- Active filters
- CCD imaging systems
- CD/DVD ROM
- Coaxial cable drivers
- Portable/battery-powered applications
- Twisted-pair driver
- Video driver

### Description

The FHP3130 (single), FHP3230 (dual), and FHP3430 (quad) are low-cost, high-performance, voltage feedback amplifiers that consume only 2.5mA of supply current per channel, while providing ±100mA of output current. These amplifiers are designed to operate from 2.7V to 12V (±6V) supplies. The common mode voltage range includes the negative rail and the output provides rail-to-rail performance.

The FHP3130, FHP3230, and FHP3430 are designed on a complimentary bipolar process and provide 170MHz of bandwidth and 110V/ $\mu$ s of slew rate at a supply voltage of ±5V. The combination of low power, rail-to-rail performance, low-voltage operation, and tiny package options make these amplifiers well suited for use in many general-purpose, high-speed applications.

These amplifiers also provide excellent video specifications. They offer extremely low differential gain and phase (0.008%/0.01°) and 0.1dB gain flatness to 10MHz for superb standard definition video performance. Their output drive capability effortlessly supports four video loads.

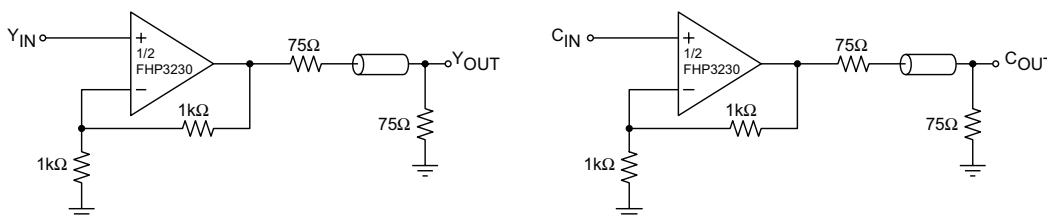


### Ordering Information

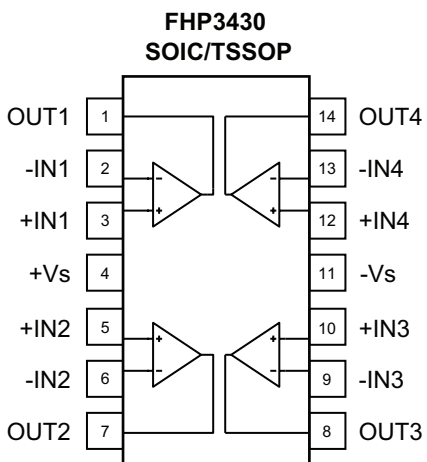
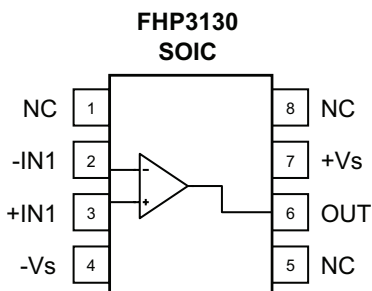
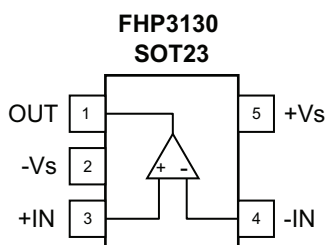
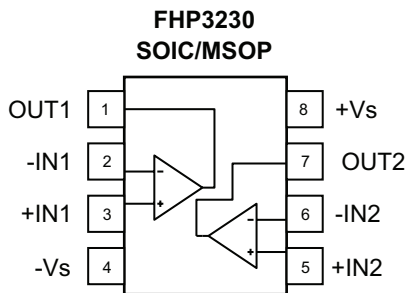
Part Number	Package	Pb-Free	Operating Temperature Range	Packaging Method
FHP3130IS5X	SOT23-5	Yes	-40°C to +85°C	Reel
FHP3130IM8X	SOIC-8	Yes	-40°C to +85°C	Reel
FHP3230IMU8X	MSOP-8	Yes	-40°C to +85°C	Reel
FHP3230IM8X	SOIC-8	Yes	-40°C to +85°C	Reel
FHP3430IMTC14X	TSSOP-14	Yes	-40°C to +85°C	Reel
FHP3430IM14X	SOIC-14	Yes	-40°C to +85°C	Reel

Moisture sensitivity level for all parts is MSL-1.

## Typical Application - YC Video Line Driver



## Pin Configurations



## Pin Assignments

FHP3230		
Pin #	Name	Description
1	OUT1	Output, channel 1
2	-IN1	Negative Input, channel 1
3	+IN1	Positive Input, channel 1
4	-Vs	Negative supply
5	+IN2	Positive Input, channel 2
6	-IN2	Negative Input, channel 2
7	OUT2	Output, channel 2
8	+Vs	Positive supply

FHP3130		
Pin # SOT/SOIC	Name	Description
1 / 6	OUT	Output
2 / 4	-Vs	Negative supply
3 / 3	+IN	Positive Input
4 / 2	-IN	Negative Input
5 / 7	+Vs	Positive supply
na / 1, 5, 8	NC	No Connect

FHP3430		
Pin #	Name	Description
1	OUT1	Output, channel 1
2	-IN1	Negative Input, channel 1
3	+IN1	Positive Input, channel 1
4	+Vs	Positive supply
5	+IN2	Positive Input, channel 2
6	-IN2	Negative Input, channel 2
7	OUT2	Output, channel 2
8	OUT3	Output, channel 3
9	-IN3	Negative Input, channel 3
10	+IN3	Positive Input, channel 3
11	-Vs	Negative supply
12	+IN4	Positive Input, channel 4
13	-IN4	Negative Input, channel 4
14	OUT4	Output, channel 4

## Absolute Maximum Ratings

The “Absolute Maximum Ratings” are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The “Recommended Operating Conditions” table defines the conditions for actual device operation.

Parameter	Min.	Max.	Unit
Supply Voltage	0	13.3	V
Input Voltage Range	$-V_S - 0.5V$	$+V_S + 0.5V$	V

## Reliability Information

Parameter	Min.	Typ.	Max.	Unit
Junction Temperature			150	°C
Storage Temperature Range	-65		150	°C
Lead Temperature (Soldering, 10s)			300	°C
Thermal Resistance				
8-Lead SOIC <sup>(1)</sup>		155		°C/W
8-Lead MSOP <sup>(1)</sup>		246		°C/W
5-Lead SOT23 <sup>(1)</sup>		296		°C/W
14-Lead TSSOP <sup>(1)</sup>		140		°C/W
14-Lead SOIC <sup>(1)</sup>		128		°C/W

### Notes:

1. Package thermal resistance ( $\theta_{JA}$ ), JEDEC standard, multi-layer test boards, still air.

## ESD Protection

Product	FHP3130		FHP3230		FHP3430	
	SOT23	SOIC	SOIC	MSOP	SOIC	TSSOP
Package	SOT23	SOIC	SOIC	MSOP	SOIC	TSSOP
Human Body Model (HBM)	3.5kV	>4kV	3.5kV	3.5kV	3kV	5kV
Charged Device Model (CDM)	>2kV	>2kV	2kV	1.5kV	2kV	1.5kV

## Recommended Operating Conditions

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range	-40		+85	°C
Supply Voltage Range	2.7		12	V

### Electrical Characteristics at +3V

$T_A = 25^\circ\text{C}$ ,  $V_s = 3\text{V}$ ,  $R_L = 2\text{k}\Omega$  to  $V_s/2$ ,  $G = 2$ ,  $R_f = R_g = 1\text{k}\Omega$ ; unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
<b>Frequency Domain Response</b>						
UGBW	-3dB Bandwidth	$G = +1$ , $V_{OUT} = 0.2V_{pp}$		160		MHz
BW <sub>SS</sub>	-3dB Bandwidth	$G = +2$ , $V_{OUT} = 0.2V_{pp}$		50		MHz
BW <sub>LS</sub>	Full Power Bandwidth	$G = +2$ , $V_{OUT} = 1V_{pp}$		45		MHz
BW <sub>0.1dBSS</sub>	0.1dB Bandwidth	$G = +2$ , $R_L = 150\text{k}\Omega$ , $V_{OUT} = 0.2V_{pp}$		11.5		MHz
GBWP	Gain Bandwidth Product	$G = +6$ , $V_{OUT} = 0.2V_{pp}$		60		MHz
<b>Time Domain Response</b>						
$t_R, t_F$	Rise and Fall Time	$V_{OUT} = 0.2\text{V}$ step		12		ns
$t_S$	Settling Time to 0.1%	$V_{OUT} = 2\text{V}$ step		90		ns
OS	Overshoot	$V_{OUT} = 0.2\text{V}$ step		1		%
SR	Slew Rate	$V_{OUT} = 2\text{V}$ step, $G = -1$		90		V/ $\mu\text{s}$
<b>Distortion/Noise Response</b>						
HD2	2nd Harmonic Distortion	$V_{OUT} = 1V_{pp}$ , 5MHz		50		dBc
HD3	3rd Harmonic Distortion	$V_{OUT} = 1V_{pp}$ , 5MHz		50		dBc
THD	Total Harmonic Distortion	$V_{OUT} = 2V_{pp}$ , 5MHz, $R_L = 100\Omega$ , $G = -1$		50		dB
$e_n$	Input Voltage Noise	> 100kHz		17		nV/ $\sqrt{\text{Hz}}$
X <sub>TALK</sub>	Crosstalk	FHP3230, FHP3430 at 1MHz		62		dB
<b>DC Performance</b>						
$V_{IO}$	Input Offset Voltage			1		mV
$dV_{IO}$	Average Drift			5		$\mu\text{V}/^\circ\text{C}$
$I_b$	Input Bias Current			-1.8		$\mu\text{A}$
$dI_b$	Average Drift			4		nA/ $^\circ\text{C}$
$I_{IO}$	Input Offset Current			0.01		$\mu\text{A}$
PSRR	Power Supply Rejection Ratio	DC		100		dB
$A_{OL}$	Open-Loop Gain	DC, $R_L = 150\Omega$		100		dB
$I_S$	Supply Current per Amplifier			2.5		mA
<b>Input Characteristics</b>						
$R_{IN}$	Input Resistance			500		$\text{k}\Omega$
$C_{IN}$	Input Capacitance			<1.5		pF
CMIR	Input Common Mode V Range			-0.3 to 2		V
CMRR	Common Mode Rejection Ratio	DC, $V_{CM} = 0\text{V}$ to $V_s - 1.5$		95		dB
<b>Output Characteristics</b>						
$V_{OUT}$	Output Voltage Swing	$R_L = 2\text{k}\Omega$ to $V_s/2$ , $G = -1$		0.05 to 2.95		V
		$R_L = 150\Omega$ to $V_s/2$ , $G = -1$		0.1 to 2.9		V
$I_{OUT}$	Linear Output Current			$\pm 100$		mA
$I_{SC}$	Short-Circuit Output Current	$V_{OUT} = V_s/2$		$\pm 120$		mA

**Electrical Characteristics at +5V**

$T_A = 25^\circ\text{C}$ ,  $V_s = 5\text{V}$ ,  $R_L = 2\text{k}\Omega$  to  $V_s/2$ ,  $G = 2$ ,  $R_f = R_g = 1\text{k}\Omega$ ; unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
<b>Frequency Domain Response</b>						
UGBW	-3dB Bandwidth	$G = +1$ , $V_{OUT} = 0.2V_{pp}$		165		MHz
BW <sub>SS</sub>	-3dB Bandwidth	$G = +2$ , $V_{OUT} = 0.2V_{pp}$		50		MHz
BW <sub>LS</sub>	Full Power Bandwidth	$G = +2$ , $V_{OUT} = 2V_{pp}$		30		MHz
BW <sub>0.1dBSS</sub>	0.1dB Bandwidth	$G = +2$ , $R_L = 150\text{k}\Omega$ , $V_{OUT} = 0.2V_{pp}$		18		MHz
GBWP	Gain Bandwidth Product	$G = +6$ , $V_{OUT} = 0.2V_{pp}$		60		MHz
<b>Time Domain Response</b>						
$t_R$ , $t_F$	Rise and Fall Time	$V_{OUT} = 0.2\text{V}$ step		12		ns
$t_S$	Settling Time to 0.1%	$V_{OUT} = 2\text{V}$ step		90		ns
OS	Overshoot	$V_{OUT} = 0.2\text{V}$ step		1		%
SR	Slew Rate	$V_{OUT} = 2\text{V}$ step, $G = -1$		105		V/ $\mu\text{s}$
<b>Distortion / Noise Response</b>						
HD2	2nd Harmonic Distortion	$V_{OUT} = 2V_{pp}$ , 5MHz		56		dBc
HD3	3rd Harmonic Distortion	$V_{OUT} = 2V_{pp}$ , 5MHz		65		dBc
THD	Total Harmonic Distortion	$V_{OUT} = 2V_{pp}$ , 5MHz		55		dB
$e_n$	Input Voltage Noise	> 100kHz		17		nV/ $\sqrt{\text{Hz}}$
X <sub>TALK</sub>	Crosstalk	FHP3230, FHP3430 at 1MHz		62		dB
DG	Differential Gain	NTSC (3.58MHz), $R_L = 150\Omega$ , AC-coupled into 220 $\mu\text{F}$ , $V_s = \pm 2.5\text{V}$		0.02		%
DP	Differential Phase	NTSC (3.58MHz), $R_L = 150\Omega$ , AC-coupled into 220 $\mu\text{F}$ , $V_s = \pm 2.5\text{V}$		0.04		°
<b>DC Performance</b>						
$V_{IO}$	Input Offset Voltage			1		mV
$dV_{IO}$	Average Drift			5		$\mu\text{V}/^\circ\text{C}$
$I_b$	Input Bias Current			-1.8		$\mu\text{A}$
$dI_b$	Average Drift			4		nA/ $^\circ\text{C}$
$I_{IO}$	Input Offset Current			0.01		$\mu\text{A}$
PSRR	Power Supply Rejection Ratio	DC		100		dB
$A_{OL}$	Open-Loop Gain	DC, $R_L = 150\Omega$		100		dB
$I_S$	Supply Current per Amplifier			2.5		mA
<b>Input Characteristics</b>						
$R_{IN}$	Input Resistance			500		k $\Omega$
$C_{IN}$	Input Capacitance			<1.5		pF
CMIR	Input Common Mode V Range			-0.3 to 4		V
CMRR	Common Mode Rejection Ratio	DC, $V_{CM} = 0\text{V}$ to $V_s - 1.5$		95		dB
<b>Output Characteristics</b>						
$V_{OUT}$	Output Voltage Swing	$R_L = 2\text{k}\Omega$ to $V_s/2$		0.05 to 4.95		V
		$R_L = 150\Omega$ to $V_s/2$		0.1 to 4.9		V
$I_{OUT}$	Linear Output Current			$\pm 100$		mA
$I_{SC}$	Short-Circuit Output Current	$V_{OUT} = V_s/2$		$\pm 120$		mA

**Electrical Characteristics at  $\pm 5V$** 

$T_A = 25^\circ\text{C}$ ,  $V_S = \pm 5V$ ,  $R_L = 2k\Omega$  to GND,  $G = 2$ ,  $R_f = R_g = 1k\Omega$ ; unless otherwise noted.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
<b>Frequency Domain Response</b>						
UGBW	-3dB Bandwidth	$G = +1$ , $V_{OUT} = 0.2V_{pp}$		170		MHz
BW <sub>SS</sub>	-3dB Bandwidth	$G = +2$ , $V_{OUT} = 0.2V_{pp}$		50		MHz
BWLs	Full Power Bandwidth	$G = +2$ , $V_{OUT} = 2V_{pp}$		30		MHz
BW <sub>0.1dBSS</sub>	0.1dB Bandwidth	$G = +2$ , $R_L = 150\Omega$ , $V_{OUT} = 0.2V_{pp}$		10		MHz
GBWP	Gain Bandwidth Product	$G = +6$ , $V_{OUT} = 0.2V_{pp}$		60		MHz
<b>Time Domain Response</b>						
$t_R, t_F$	Rise and Fall Time	$V_{OUT} = 0.2V$ step		12		ns
$t_S$	Settling Time to 0.1%	$V_{OUT} = 2V$ step		90		ns
OS	Overshoot	$V_{OUT} = 0.2V$ step		1		%
SR	Slew Rate	$V_{OUT} = 2V$ step, $G = -1$		110		V/ $\mu$ s
<b>Distortion/Noise Response</b>						
HD2	2nd Harmonic Distortion	$V_{OUT} = 2V_{pp}$ , 5MHz		65		dBc
HD3	3rd Harmonic Distortion	$V_{OUT} = 2V_{pp}$ , 5MHz		65		dBc
THD	Total Harmonic Distortion	$V_{OUT} = 2V_{pp}$ , 5MHz		54		dB
$e_n$	Input Voltage Noise	> 100kHz		17		nV/ $\sqrt{\text{Hz}}$
X <sub>TALK</sub>	Crosstalk	FHP3230, FHP3430 at 1MHz		62		dB
DG	Differential Gain	NTSC (3.58MHz), $R_L = 150\Omega$ , AC-coupled into 220 $\mu$ F		0.008		%
DP	Differential Phase	NTSC (3.58MHz), $R_L = 150\Omega$ , AC-coupled into 220 $\mu$ F		0.01		$^\circ$
<b>DC Performance</b>						
$V_{IO}$	Input Offset Voltage <sup>(1)</sup>		-6	1	6	mV
$dV_{IO}$	Average Drift			5		$\mu$ V/ $^\circ\text{C}$
$I_b$	Input Bias Current <sup>(1)</sup>		-4	-1.8		$\mu$ A
$dI_b$	Average Drift			4		nA/ $^\circ\text{C}$
$I_{IO}$	Input Offset Current <sup>(1)</sup>		-0.8	0.01	0.8	$\mu$ A
PSRR	Power Supply Rejection Ratio <sup>(2)</sup>	DC	80	100		dB
$A_{OL}$	Open-Loop Gain <sup>(2)</sup>	DC, $R_L = 150\Omega$	80	100		dB
$I_S$	Supply Current per Amplifier <sup>(1)</sup>			2.5	3.5	mA
<b>Input Characteristics</b>						
$R_{IN}$	Input Resistance			500		k $\Omega$
$C_{IN}$	Input Capacitance			<1.5		pF
CMIR	Input Common Mode V Range			-5 to 4		V
CMRR	Common Mode Rejection Ratio <sup>(2)</sup>	DC, $V_{CM} = -5V$ to 3.5V	75	100		dB
<b>Output Characteristics</b>						
$V_{OUT}$	Output Voltage Swing	$R_L = 2k\Omega$		$\pm 4.95$		V
		$R_L = 150\Omega$ <sup>(1)</sup>	-4.65	$\pm 4.7$	4.65	V
$I_{OUT}$	Linear Output Current			$\pm 100$		mA
$I_{SC}$	Short-Circuit Output Current	$V_{OUT} = 0V$		$\pm 120$		mA

**Notes:**

- 100% tested at 25 $^\circ\text{C}$
- Min/max guaranteed by design/characterization.

### Typical Performance Characteristics

$T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{V}$ ,  $R_L = 2\text{k}\Omega$  to  $V_S/2$  for  $V_S = 5\text{V}$  and  $3\text{V}$ ,  $R_L = 2\text{k}\Omega$  to GND for  $V_S = \pm 5\text{V}$ ,  $G = 2$ ,  $R_f = R_g = 1\text{k}\Omega$ ; unless otherwise noted.

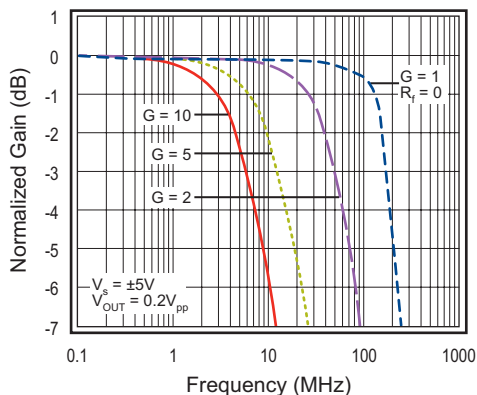


Figure 1. Non-Inverting Freq. Response ( $\pm 5\text{V}$ )

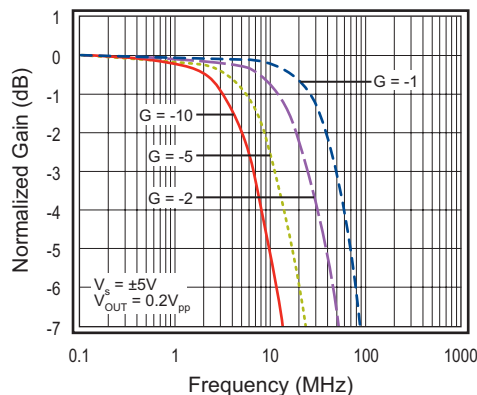


Figure 2. Inverting Freq. Response ( $\pm 5\text{V}$ )

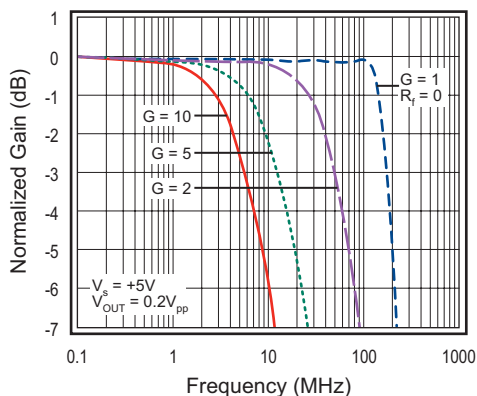


Figure 3. Non-Inverting Freq. Response ( $+5\text{V}$ )

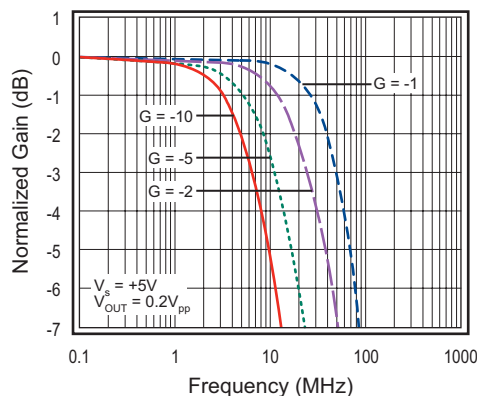


Figure 4. Inverting Freq. Response ( $+5\text{V}$ )

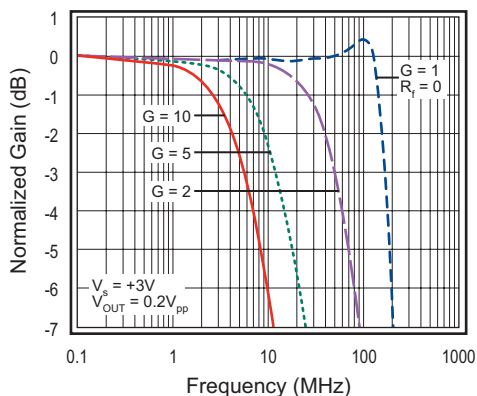


Figure 5. Non-Inverting Freq. Response ( $+3\text{V}$ )

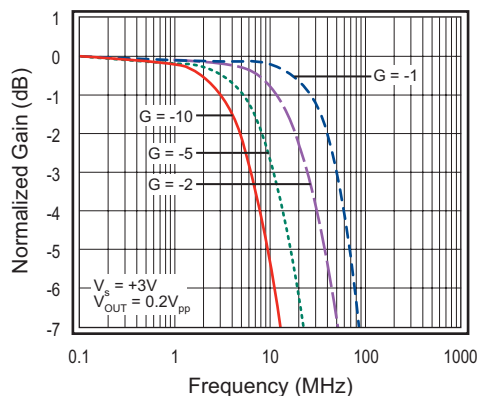


Figure 6. Inverting Freq. Response ( $+3\text{V}$ )



### Typical Performance Characteristics - Continued

$T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{V}$ ,  $R_L = 2\text{k}\Omega$  to  $V_S/2$  for  $V_S = 5\text{V}$  and  $3\text{V}$ ,  $R_L = 2\text{k}\Omega$  to GND for  $V_S = \pm 5\text{V}$ ,  $G = 2$ ,  $R_f = R_g = 1\text{k}\Omega$ ; unless otherwise noted.

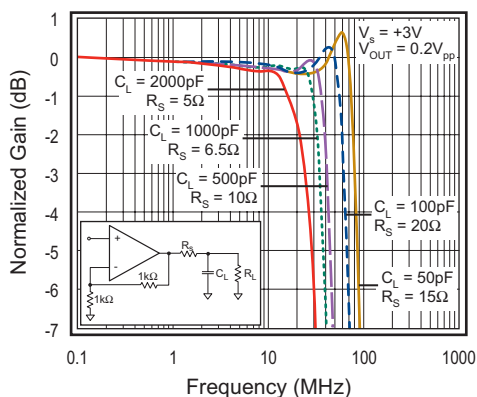


Figure 7. Frequency Response vs.  $C_L$  (+3V)

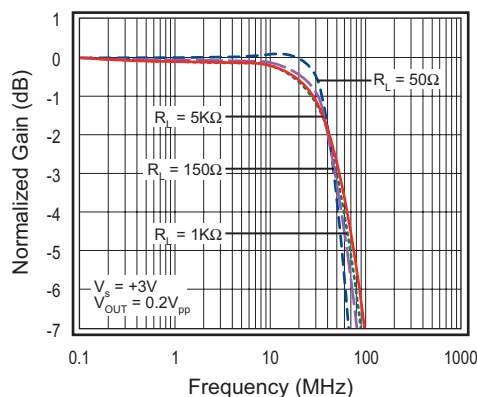


Figure 8. Frequency Response vs.  $R_L$  (+3V)

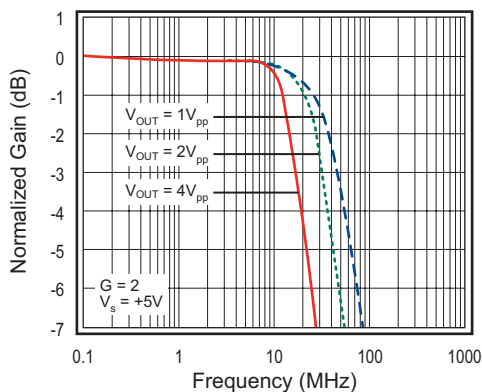


Figure 9. Large Signal Freq. Response ( $\pm 5\text{V}$ )

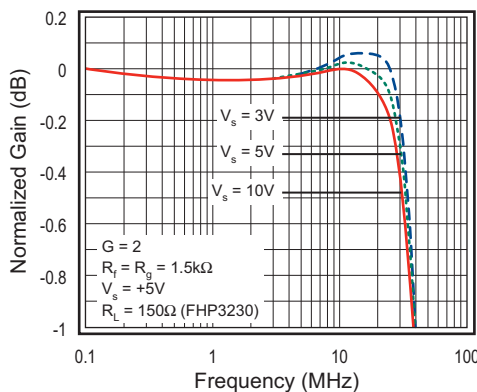


Figure 10. Gain Flatness

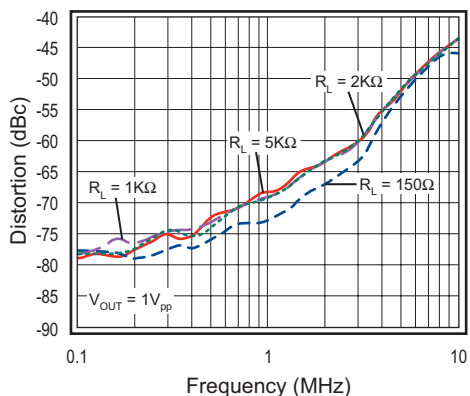


Figure 11. HD2 vs.  $R_L$  (+3V)

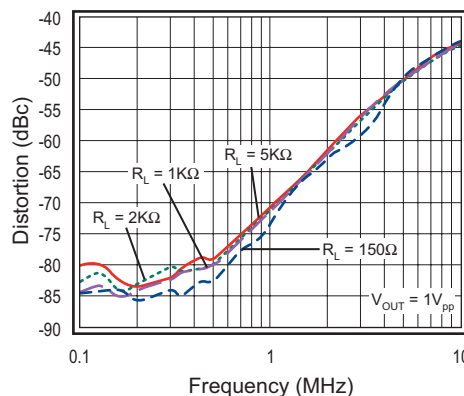


Figure 12. HD2 vs.  $R_L$  (+3V)

### Typical Performance Characteristics - Continued

$T_A = 25^\circ\text{C}$ ,  $V_s = 5\text{V}$ ,  $R_L = 2\text{k}\Omega$  to  $V_s/2$  for  $V_s = 5\text{V}$  and  $3\text{V}$ ,  $R_L = 2\text{k}\Omega$  to GND for  $V_s = \pm 5\text{V}$ ,  $G = 2$ ,  $R_f = R_g = 1\text{k}\Omega$ ; unless otherwise noted.

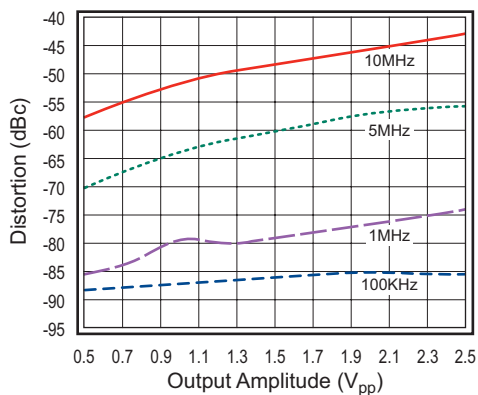


Figure 13. HD2 vs.  $V_{OUT}$  (+5V)

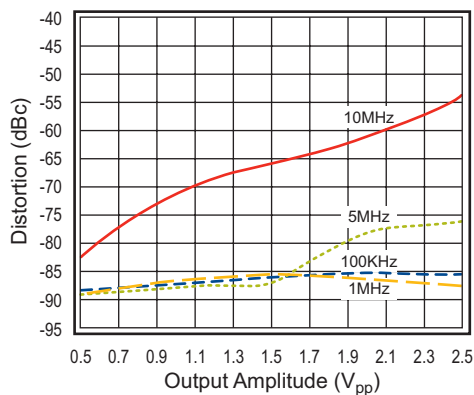


Figure 14. HD3 vs.  $V_{OUT}$  (+5V)

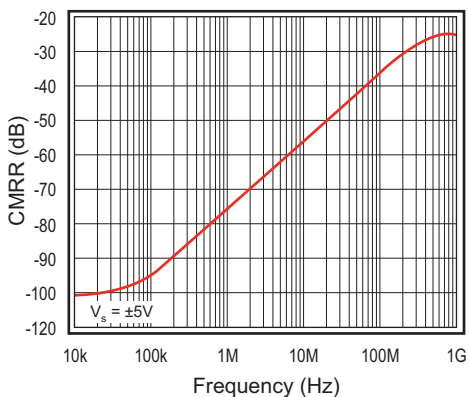


Figure 15. CMMR vs. Frequency

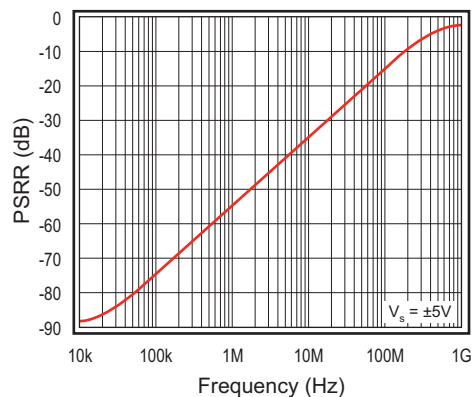


Figure 16. PSRR vs. Frequency

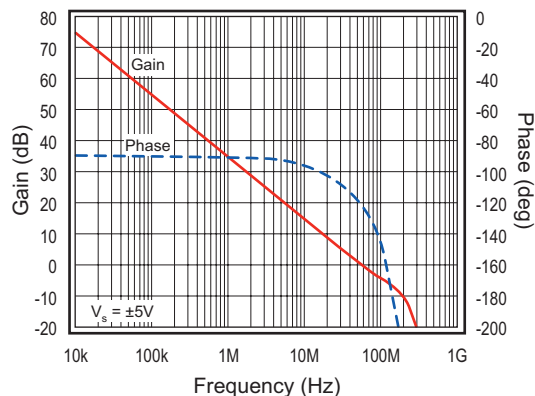


Figure 17. Open-Loop Gain and Phase

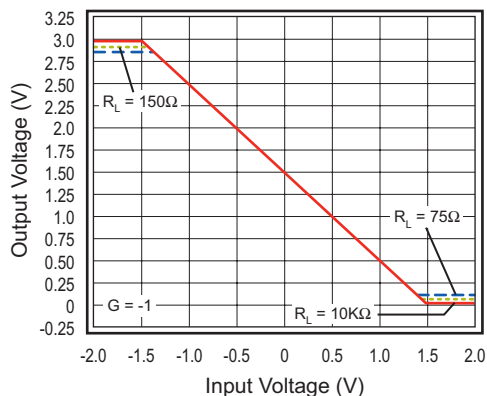
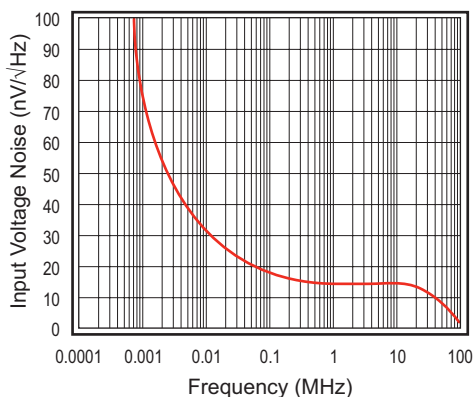


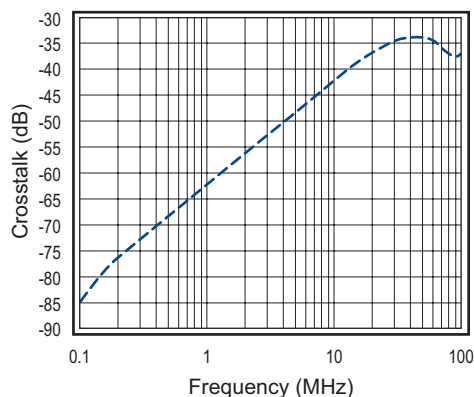
Figure 18. Output Swing vs. Load (+3V)

### Typical Performance Characteristics - Continued

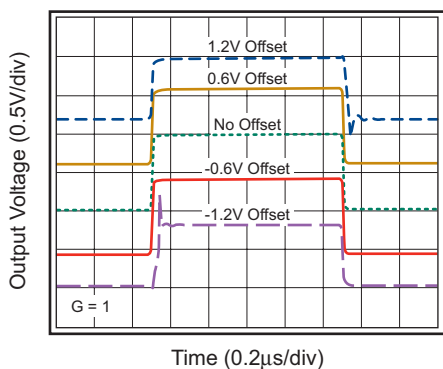
$T_A = 25^\circ\text{C}$ ,  $V_S = 5\text{V}$ ,  $R_L = 2\text{k}\Omega$  to  $V_S/2$  for  $V_S = 5\text{V}$  and  $3\text{V}$ ,  $R_L = 2\text{k}\Omega$  to GND for  $V_S = \pm 5\text{V}$ ,  $G = 2$ ,  $R_f = R_g = 1\text{k}\Omega$ ; unless otherwise noted.



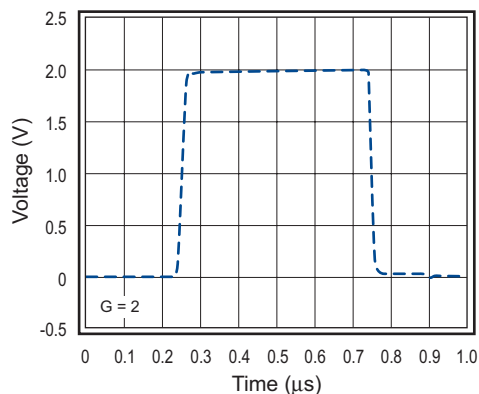
**Figure 19. Input Voltage Noise (+3V)**



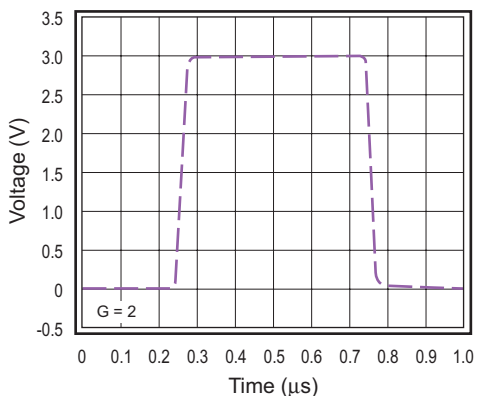
**Figure 20. Crosstalk vs. Frequency (+3V)**



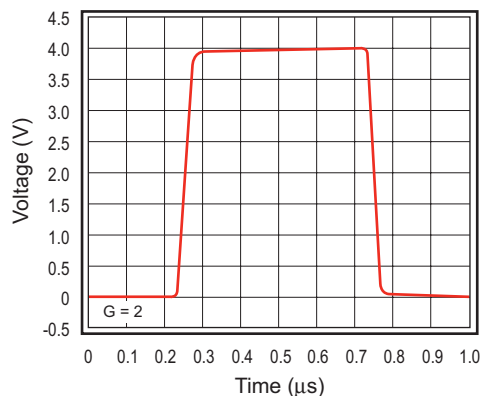
**Figure 21. Pulse Resp. vs. Common Mode Voltage**



**Figure 22. Large Signal Pulse Response (+3V)**



**Figure 23. Large Signal Pulse Response (+5V)**



**Figure 24. Large Signal Pulse Response ( $\pm 5\text{V}$ )**

### Typical Performance Characteristics - Continued

$T_A = 25^\circ\text{C}$ ,  $V_s = 5\text{V}$ ,  $R_L = 2\text{k}\Omega$  to  $V_s/2$  for  $V_s = 5\text{V}$  and  $3\text{V}$ ,  $R_L = 2\text{k}\Omega$  to GND for  $V_s = \pm 5\text{V}$ ,  $G = 2$ ,  $R_f = R_g = 1\text{k}\Omega$ ; unless otherwise noted.

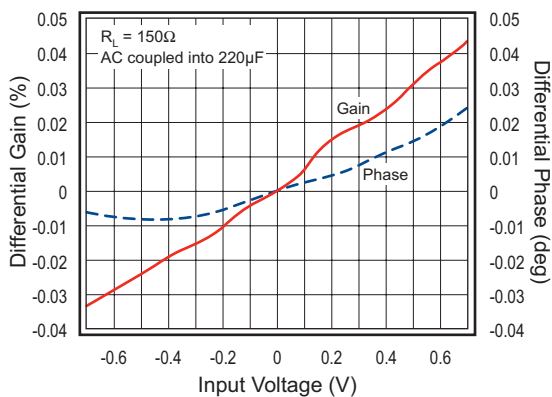


Figure 25. Differential Gain and Phase ( $\pm 2.5$ )

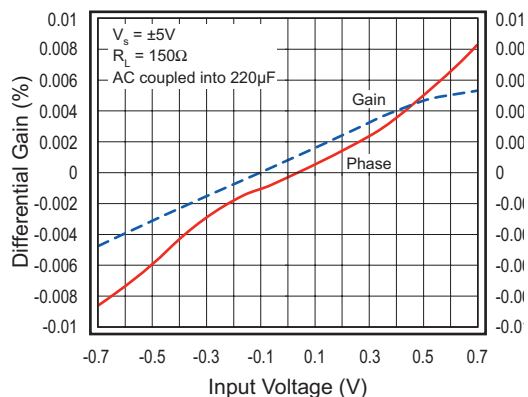
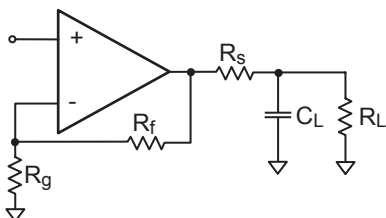


Figure 26. Differential Gain and Phase ( $\pm 5$ )

## Application Information

### Driving Capacitive Loads

The FREQUENCY RESPONSE VS.  $C_L$  plot in Figure 7, illustrates the response of the FHP3230 Family. A small series resistance ( $R_s$ ) at the output of the amplifier, illustrated in Figure 27, improves stability and settling performance.  $R_s$  values in the FREQUENCY RESPONSE VS.  $C_L$  plot were chosen to achieve maximum bandwidth with less than 1dB of peaking. For maximum flatness, use a larger  $R_s$ .



**Figure 27. Typical Topology for Driving Capacitive Loads**

### Power Dissipation

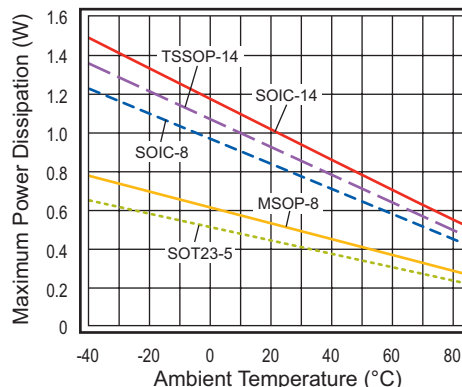
The maximum internal power dissipation allowed is directly related to the maximum junction temperature. If the maximum junction temperature exceeds 150°C for an extended time, device failure may occur.

The FHP3130, FHP3230, and FHP3430 are short-circuit protected; however, this may not guarantee that the maximum junction temperature (+150°C) is not exceeded under all conditions. RMS Power Dissipation can be calculated using the following equation:

$$\text{Power Dissipation} = I_s * (V_{s+} - V_{s-}) + (V_{s+} - V_{o(RMS)}) * I_{OUT(RMS)}$$

where  $I_s$  is the supply current,  $V_{s+}$  is the positive supply pin voltage,  $V_{s-}$  is the negative supply pin voltage,  $V_{o(RMS)}$  is the RMS output voltage, and  $I_{OUT(RMS)}$  is the RMS output current delivered to the load.

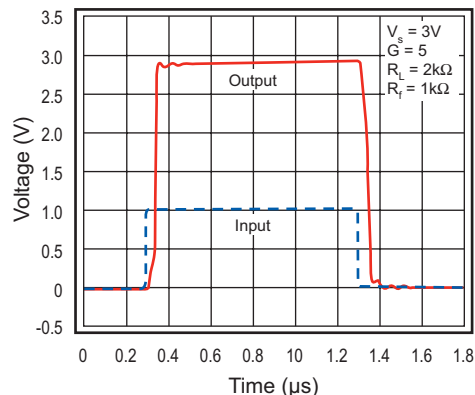
Follow the maximum power derating curves shown in Figure 28 below to ensure proper operation.



**Figure 28. Maximum Power Derating**

### Overdrive Recovery

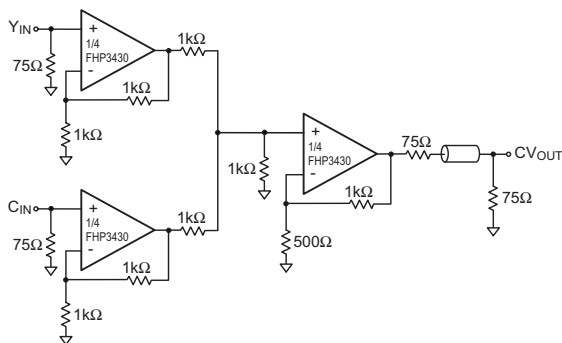
For an amplifier, an overdrive condition occurs when the output and/or input ranges are exceeded. The recovery time varies based on whether the input or output is overdriven and by how much the ranges are exceeded. The FHP3130/3230/3430 typically recovers in less than 50ns from an overdrive condition. Figure 29 shows the FHP3230 in an overdriven condition.



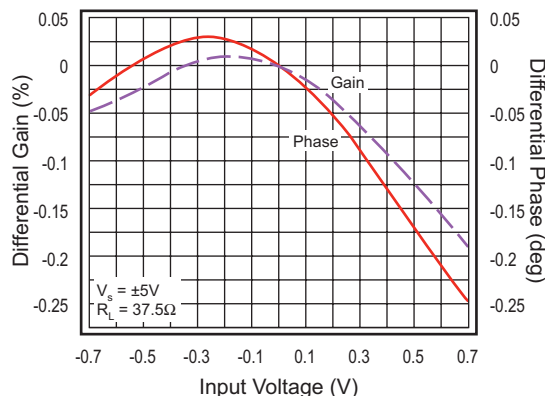
**Figure 29. Overdrive Recovery**

### Composite Video Summer

The bandwidth and differential gain/phase performance of the FHP3130/3230/3430 amplifiers make them well suited for video applications. Figure 30 shows a typical Composite Video Summer. The high output current capability allows for driving multiple video loads. Figure 31 shows the resulting differential gain/phase of this three-amplifier configuration driving four video loads, or 37.5Ω.



**Figure 30. Typical Composite Video Summer**



**Figure 31. DG/DP of CV Summer Driving Four Video Loads**

### Layout Considerations

General layout and supply bypassing play major roles in high-frequency performance. Fairchild has evaluation boards to guide high-frequency layout and aid device testing and characterization. Follow the guidelines below as a basis for high-frequency layout:

- Include 6.8μF and 0.01μF ceramic capacitors.
- Place the 6.8μF capacitor within 0.75 inches of the power pin.
- Place the 0.01μF capacitor within 0.1 inches of the power pin.
- Remove the ground plane under and around the part, especially near the input and output pins, to reduce parasitic capacitance.
- Minimize all trace lengths to reduce series inductances.

Refer to the evaluation board layouts shown below for more information.

### Evaluation Board Information

The following evaluation boards are available to aid testing and layout of these devices:

Evaluation Board	Products
KEB002	FHP3130IS5X
KEB003	FHP3130IM8X
KEB010	FHP3230IMU8X
KEB006	FHP3230IM8X
KEB012	FHP3430IMTC14X
KEB018	FHP3430IM14X

### Evaluation Board Schematics

Evaluation board schematics and layouts are shown in Figures 32 – 46. These evaluation boards are built for dual-supply operation. Follow these steps to use the board in a single-supply application:

1. Short  $-V_s$  to ground.
2. Use C3 and C4 if the  $-V_s$  pin of the amplifier is not directly connected to the ground plane.

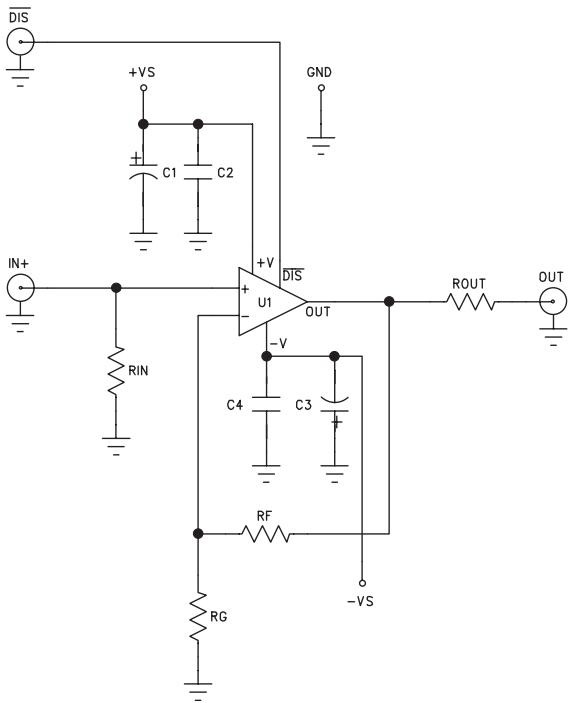


Figure 32. FHP3130 KEB002/KEB003 Schematic

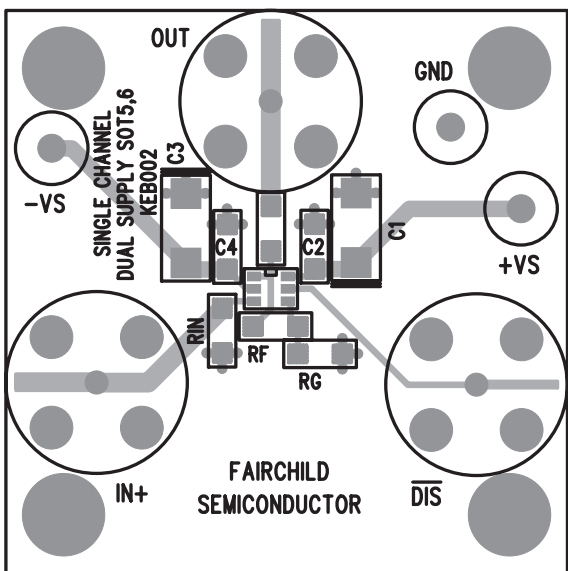


Figure 33. FHP3130 KEB002 (Top-side)

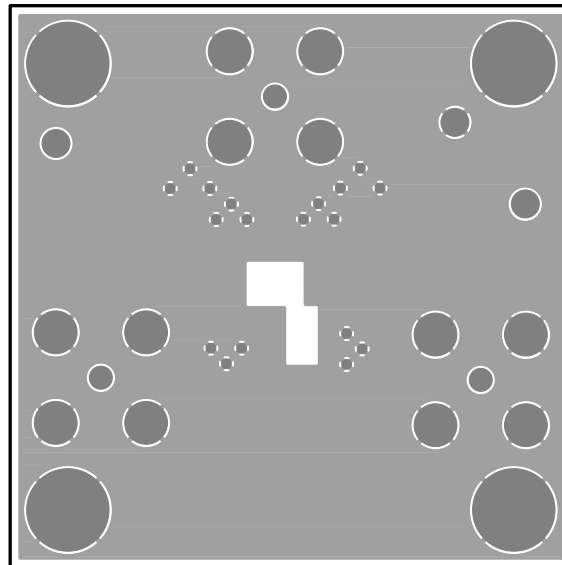


Figure 34. FHP3130 KEB002 (Bottom-side)

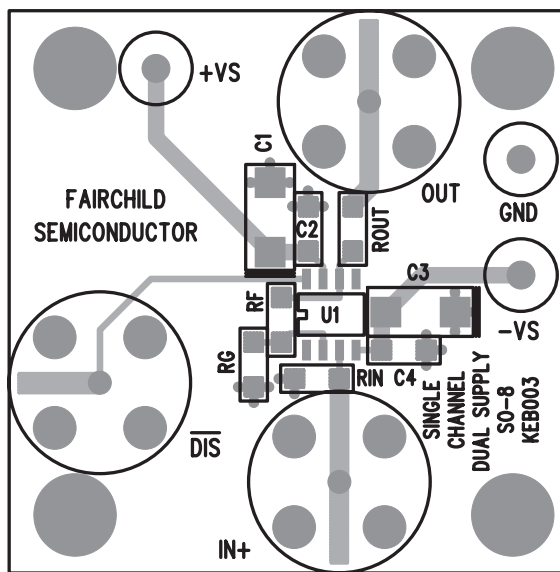


Figure 35. FHP3130 KEB003 (Top-side)

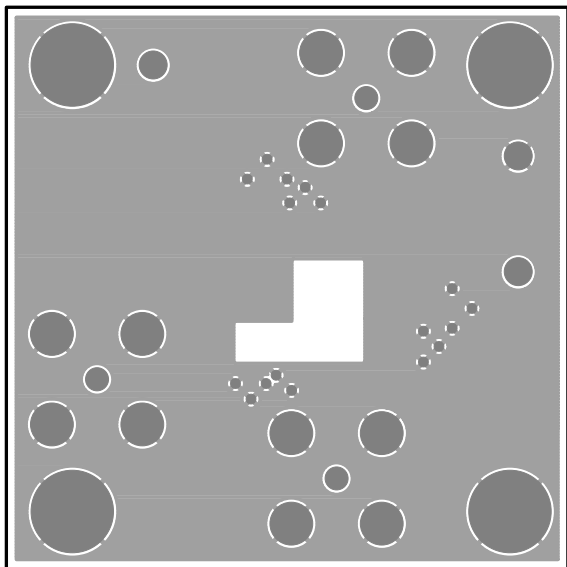


Figure 36. FHP3130 KEB003 (Bottom-side)

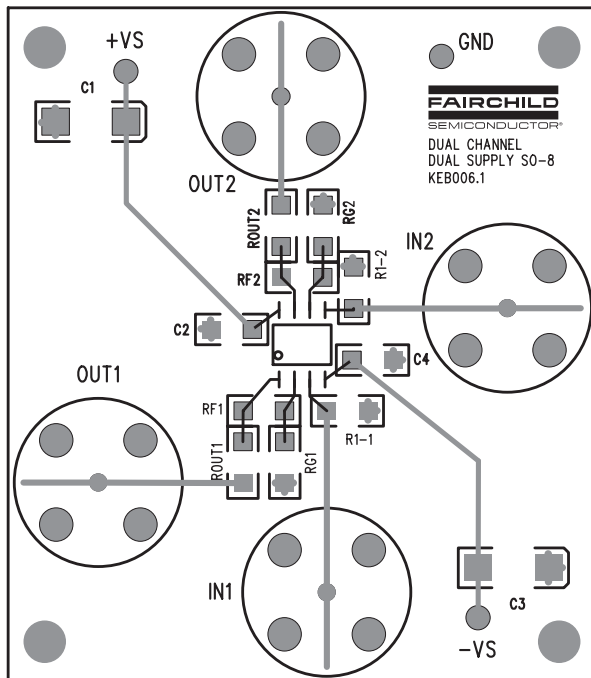


Figure 38. FHP3230 KEB006 (Top-side)

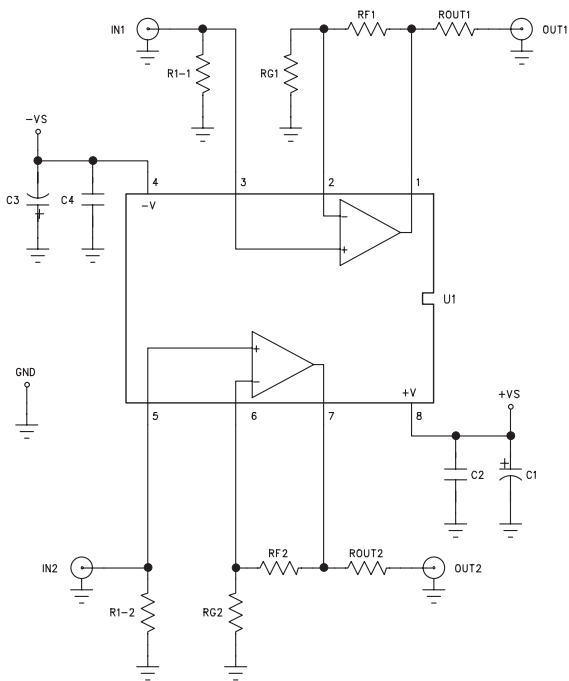


Figure 37. FHP3230 KEB006/KEB010 Schematic

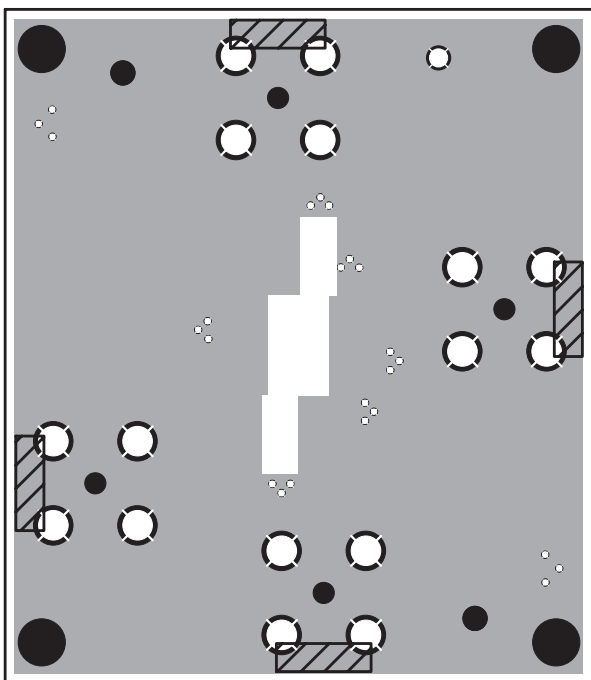


Figure 39. FHP3230 KEB006 (Bottom-side)



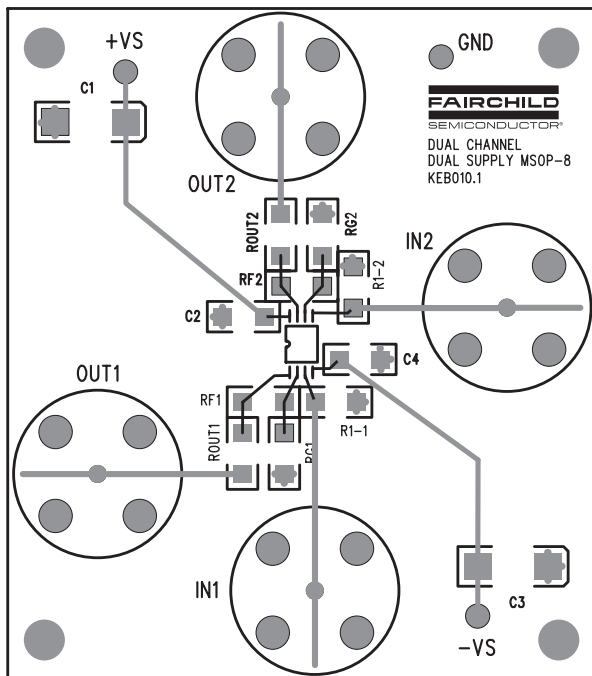


Figure 40. FHP3230 KEB010 (Top-side)

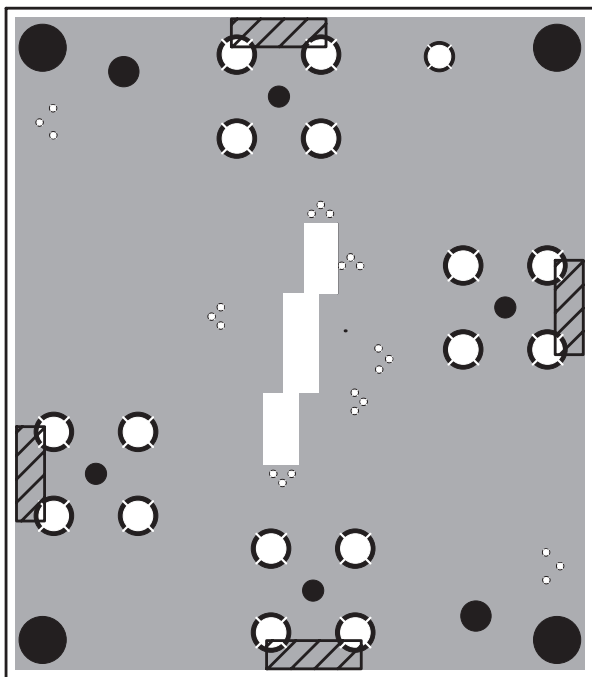


Figure 41. FHP3230 KEB010 (Bottom-side)

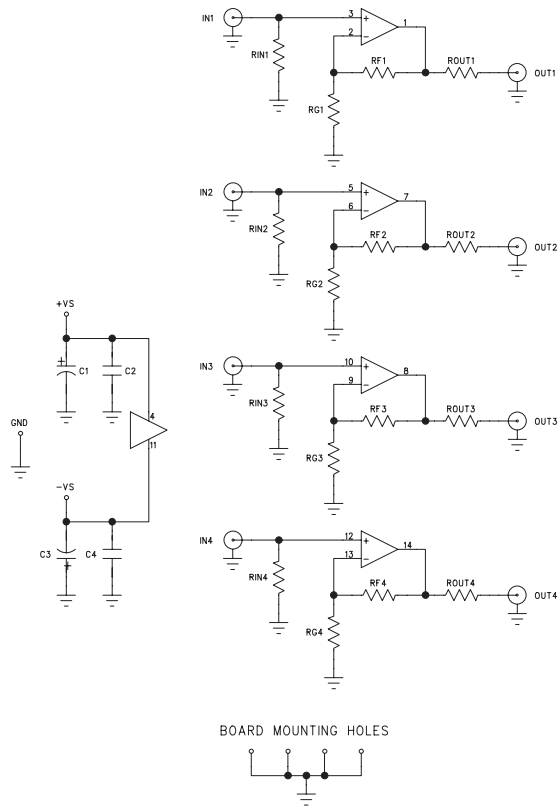


Figure 42. FHP3430 KEB012/KEB018 Schematic

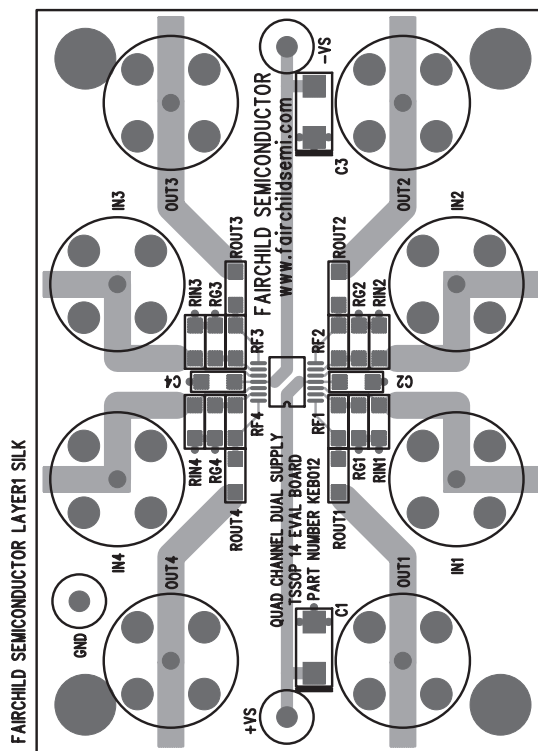


Figure 43. FHP3430 KEB012 (Top-side)

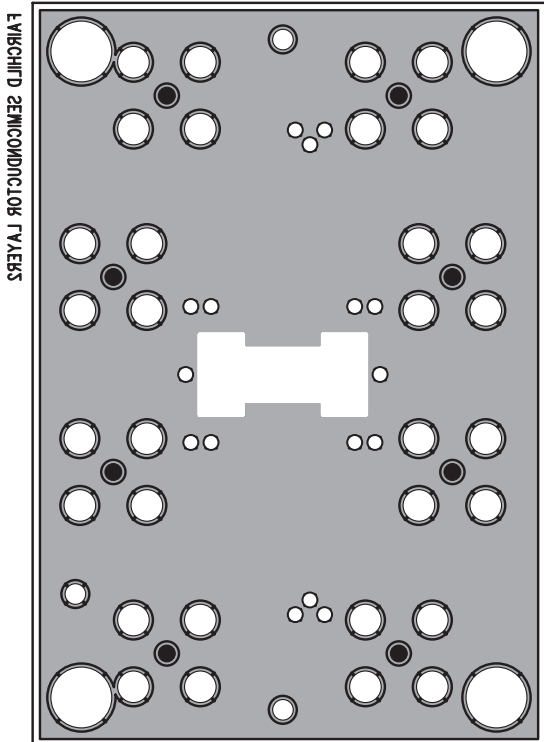


Figure 44. FHP3430 KEB012 (Bottom-side)

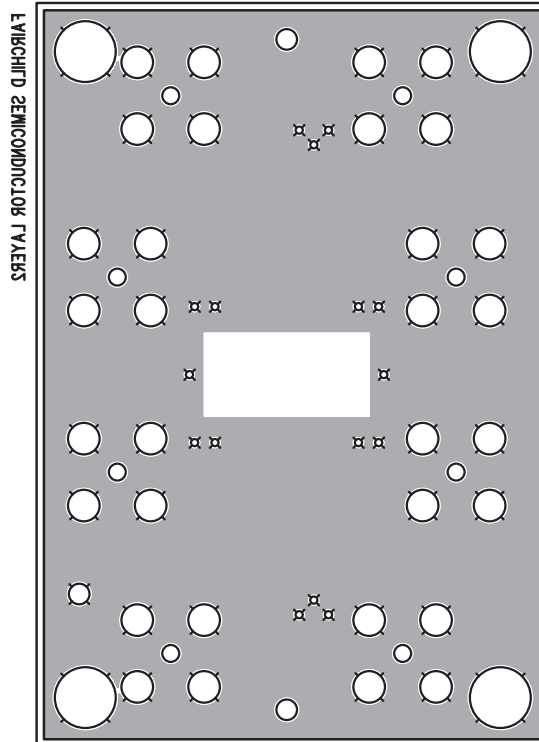


Figure 46. FHP3430 KEB018 (Bottom-side)

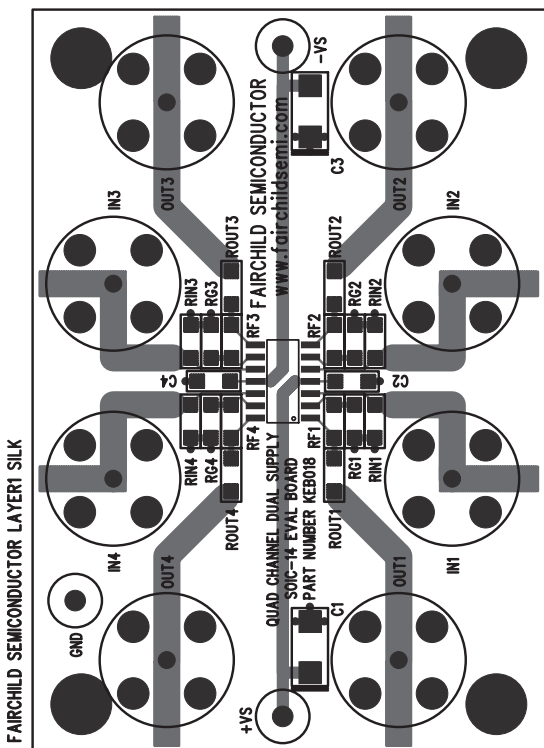
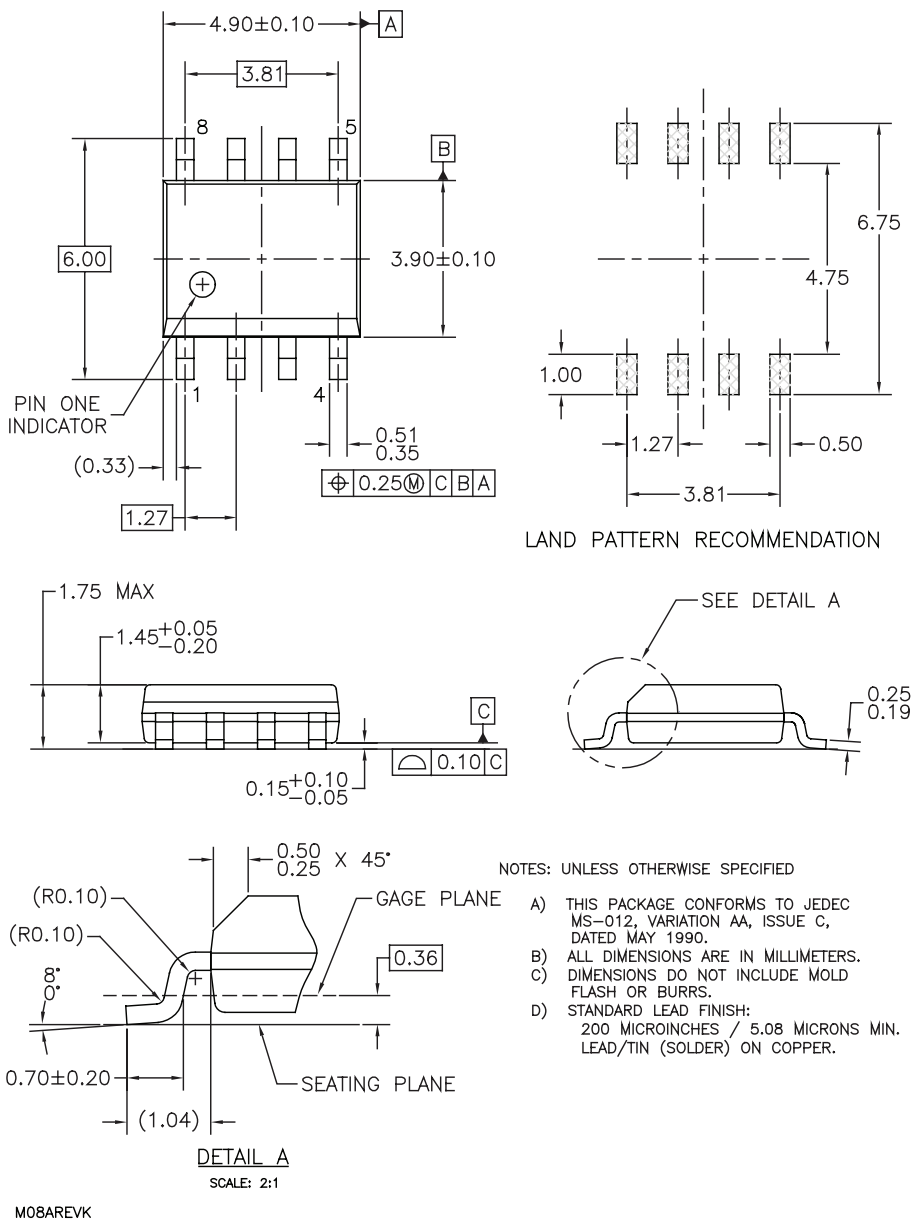


Figure 45. FHP3430 KEB018 (Top-side)

### Mechanical Dimensions



**Figure 47. SOIC-8 Package**

### Mechanical Dimensions

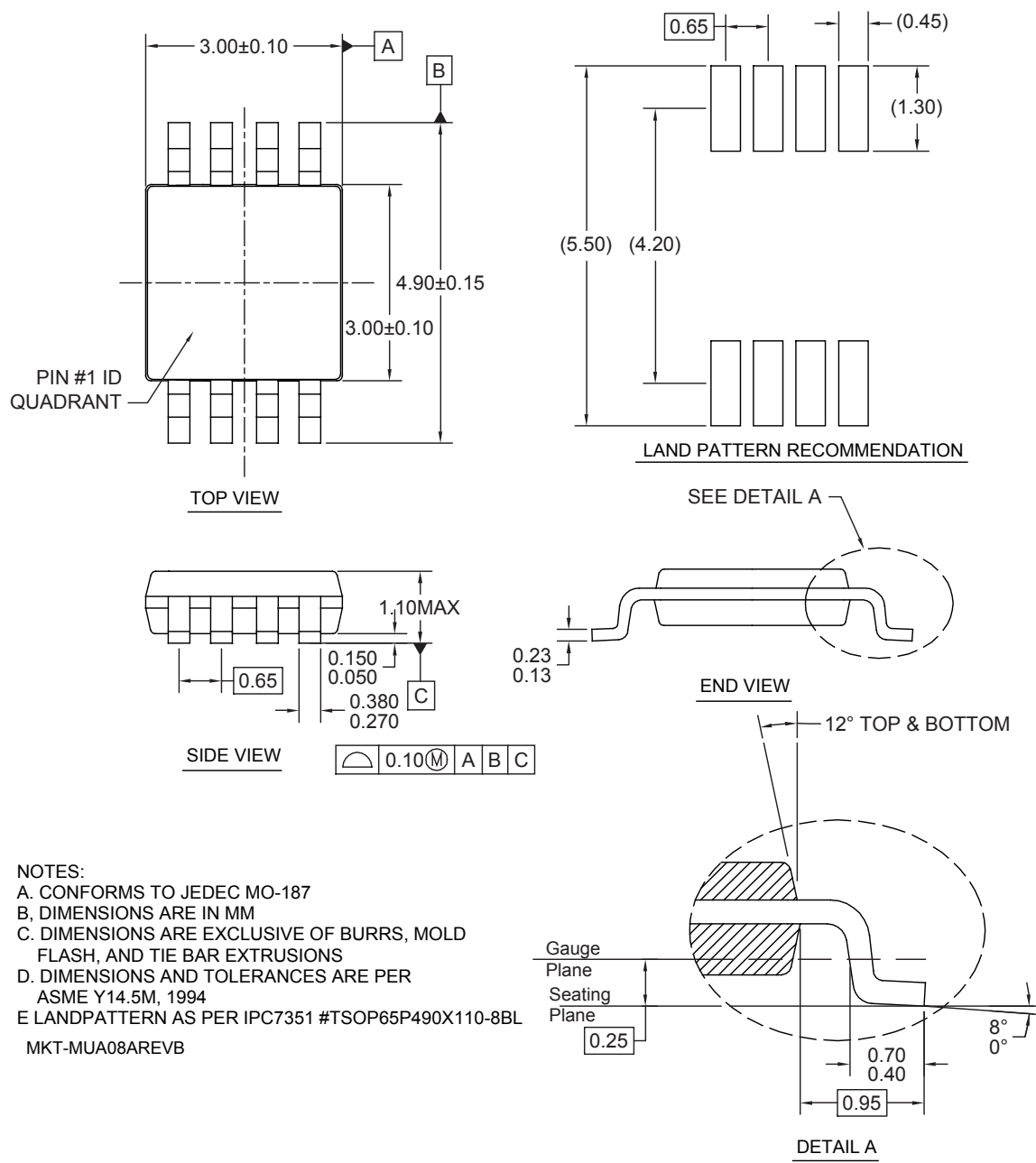
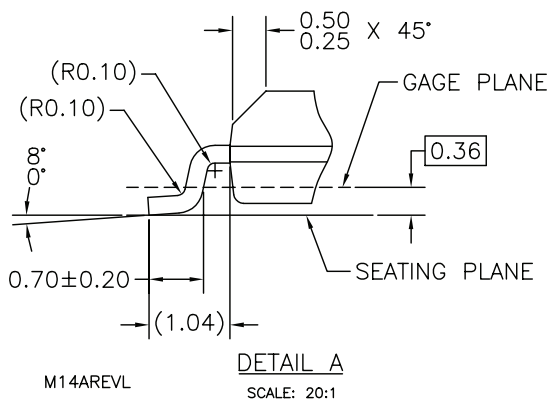
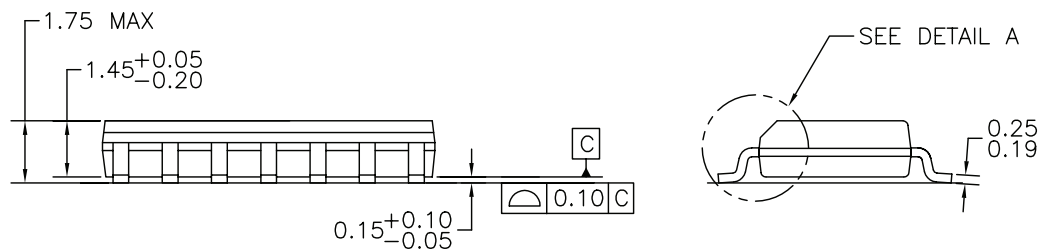
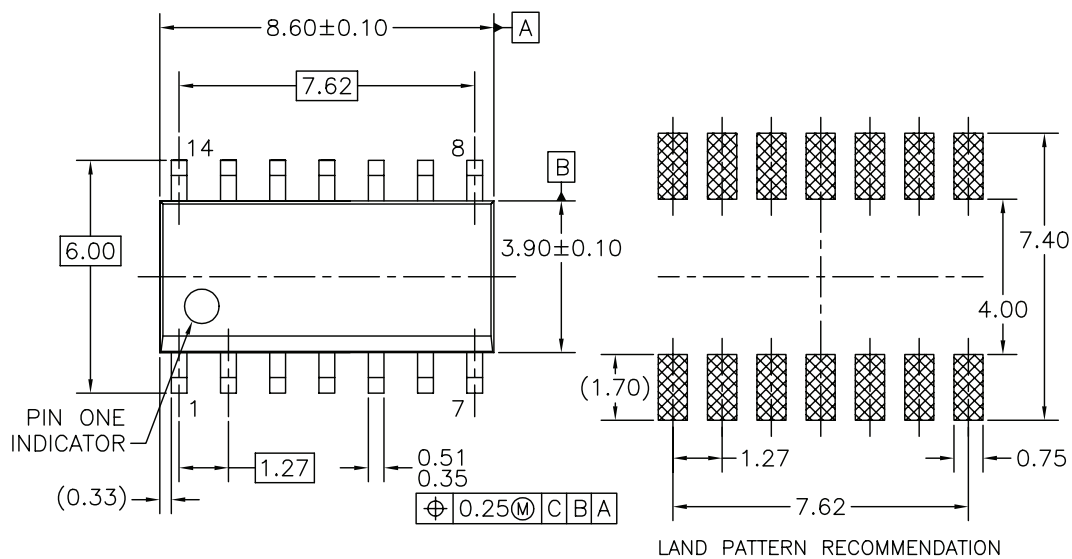


Figure 48. MSOP-8 Package

### Mechanical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AB, ISSUE C, DATED MAY 1990.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.

**Figure 49. SOIC-14 Package**

### Mechanical Dimensions

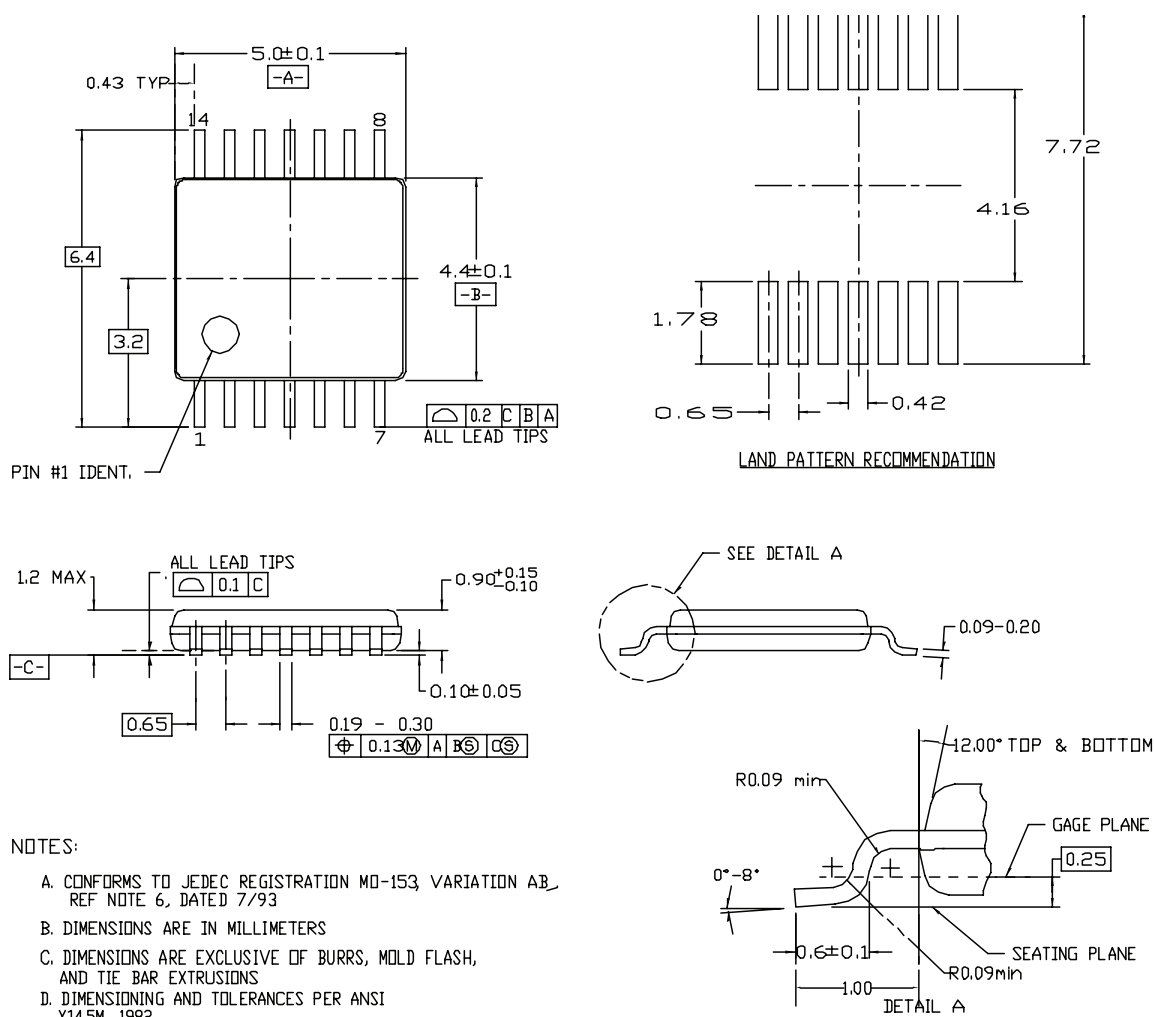
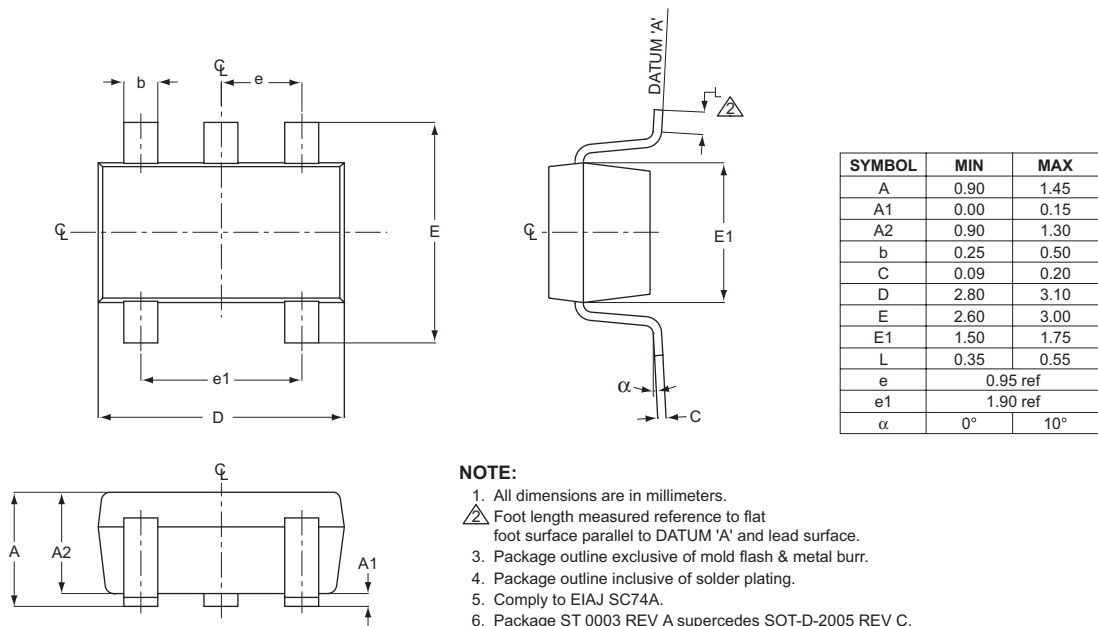


Figure 50. TSSOP-14 Package

### Mechanical Dimensions



**Figure 51. SOT23-5 Package**

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Build it Now™	HiSeC™	OPTOPLANAR™	Stealth™	Wire™
CoolFET™	i <sup>2</sup> C™	PACMAN™	SuperFET™	
CROSSVOL™	i-Lo™	POP™	SuperSOT™_3	
DOME™	ImpliedDisconnect™	Power247™	SuperSOT™_6	
EcoSPARK™	IntelliMAX™	PowerEdge™	SuperSOT™_8	
E <sup>2</sup> CMOS™	ISOPLANAR™	PowerSaver™	SyncFET™	
EnSigna™	LittleFET™	PowerTrench®	TCM™	
FACT™	MICROCOUPLER™	QFET®	TinyBoost™	
FAST®	MicroFET™	QS™	TinyBuck™	
FASTr™	MicroPak™	QT Optoelectronics™	TinyPWM™	
FPS™	MICROWIRE™	Quiet Series™	TinyPower™	
FRFET™	MSX™	RapidConfigure™	TinyLogic®	
	MSXPro™	RapidConnect™	TINYOPTO™	
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	Programmable Active Droop™			

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