imall

Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from, Europe, America and south Asia, supplying obsolete and hard-to-find components to meet their specific needs.

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FJ6K01010L Silicon P-channel MOS FET

For switching

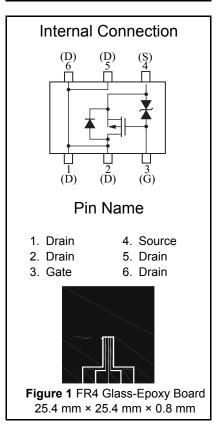
Features

- Low drain-source On-state resistance : RDS (on) typ. = 26 m Ω (VGS = -4.5 V)
- Low drive voltage : 1.8 V drive
- Halogen-free / RoHS compliant
- (EU RoHS / UL-94 V-0 / MSL:Level 1 compliant)
- Marking Symbol : T4

Packaging

Embossed type (Thermo-compression sealing): 3 000 pcs / reel (standard)

	Unit : mm				
1. Drain 2. Drain 3. Gate	 Source Drain Drain 				
Panasonic	WSMini6-F1-B				
JEITA	SC-113DA				
Code	_				



■ Absolute Maximum Ratings Ta = 25 °C Symbol Parameter Rating Unit Drain-source voltage VDS -12 V VGS V Gate-source voltage ±8 Drain current ID -4.0 А Pulse drain current -20 IDp А Total power dissipation PD 700 mW Channel temperature Tch 150 °C Operating ambient temperature Topr -40 to + 85 °C Storage temperature Tstg -55 to +150 °C

Note) *1 Measuring on Glass epoxy board (25.4 x 25.4 x 0.8 mm) (See Figure 1) Absolute maximum rating without heat sink for PD is 150 mW



Electrical Characteristics	Ta = 25 °C ± 3 °C
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Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Drain-source breakdown voltage	VDSS	ID = -1 mA, VGS = 0	-12			V
Drain-source cutoff current	IDSS	VDS = -10 V, VGS = 0			-1.0	μA
Gate-source cutoff current	IGSS	VGS = ±8 V, VDS = 0			±10	μA
Gate threshold voltage	Vth	ID = -1.0 mA, VDS = -6.0 V	-0.3	-0.65	-1.0	V
	RDS(on)1	ID = -1.0 A, VGS = -4.5 V		26	34	
Drain-source ON resistance	RDS(on)2	ID = -0.5 A, VGS = -2.5 V		30	41	mΩ
	RDS(on)3	ID = -0.5 A, VGS = -1.8 V		36	54	
Forward transfer admittance	Yfs	ID = -1.0 A, VDS = -10 V	4.0			S
Input capacitance	Ciss	VDS = -10 V, VGS = 0, f = 1 MHz		1 400		pF
Output capacitance	Coss			190		pF
Reverse transfer capacitance	Crss			210		pF
Turn-on delay time ^{*1}	td(on)	VDD = -6 V, VGS = 0 to -4 V		9		ns
Rise time ^{*1}	tr	ID = -1.0 A		40		ns
Turn-off delay time *1	td(off)	VDD = -6 V, VGS = -4 to 0 V		250		ns
Fall time ^{*1}	tf	ID = -1.0 A		150		ns

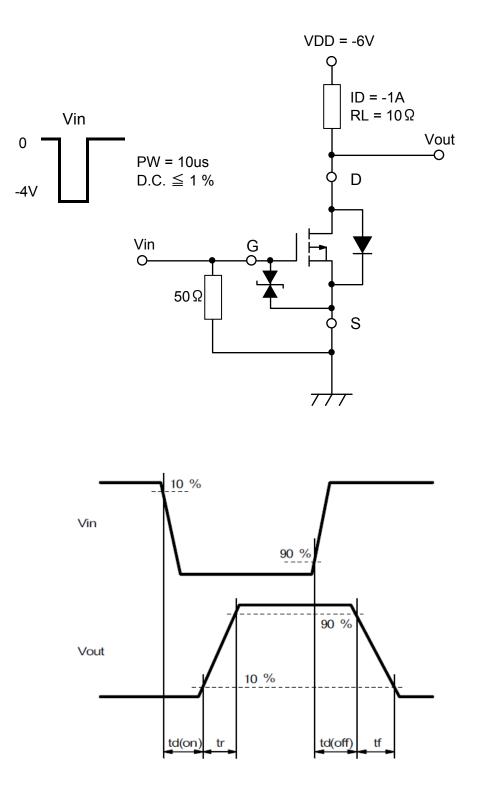
Note) 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

2. *1 Measurement circuit for Turn-on Delay Time/Rise Time/Turn-off Delay Time/Fall Time

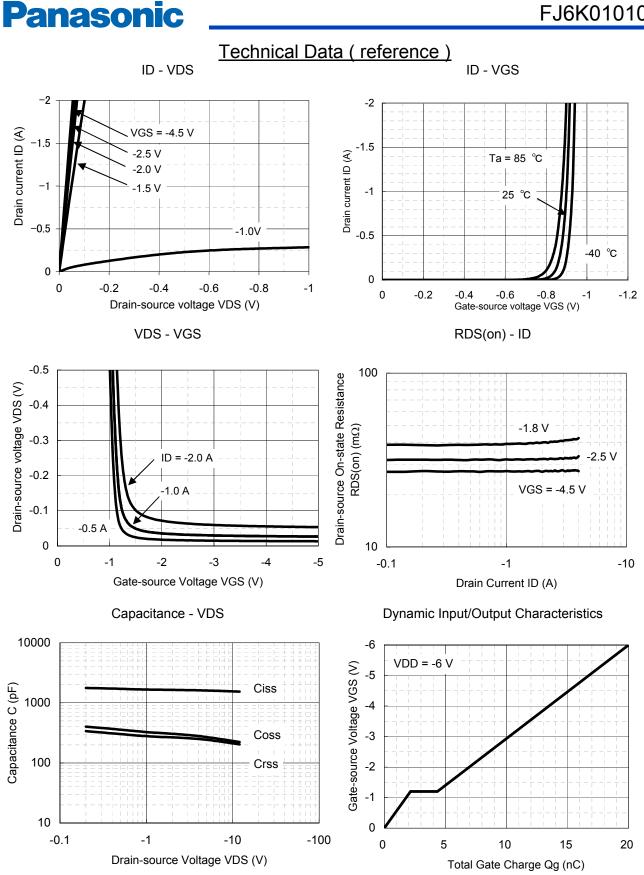
Doc No. TT4-EA-12484 Revision. 2



*1 Measurement circuit for Turn-on Delay Time/Rise Time/Turn-off Delay Time/Fall Time

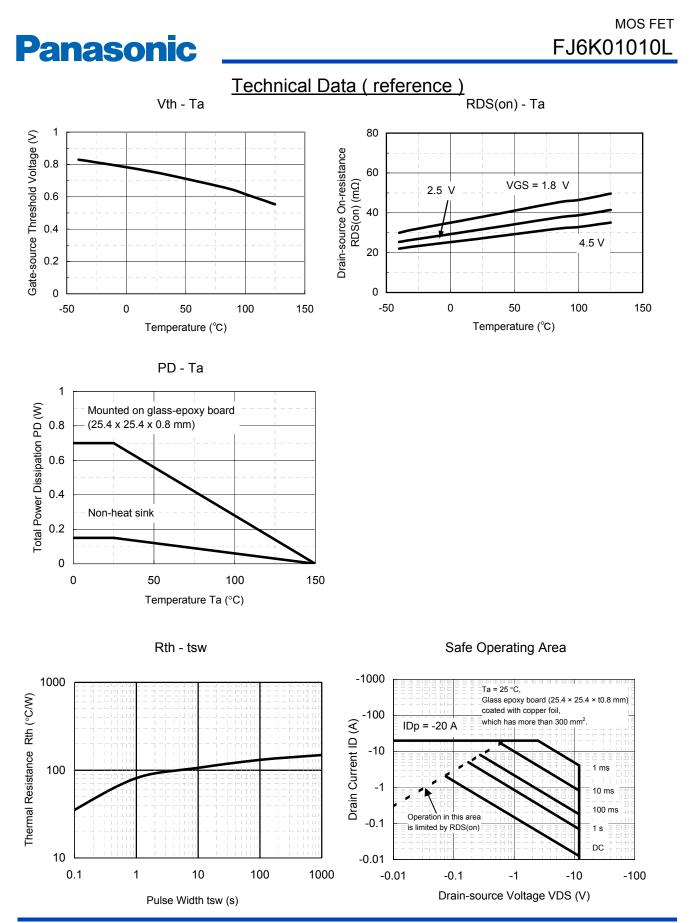


Established : 2010-04-05 Revised : 2013-07-01



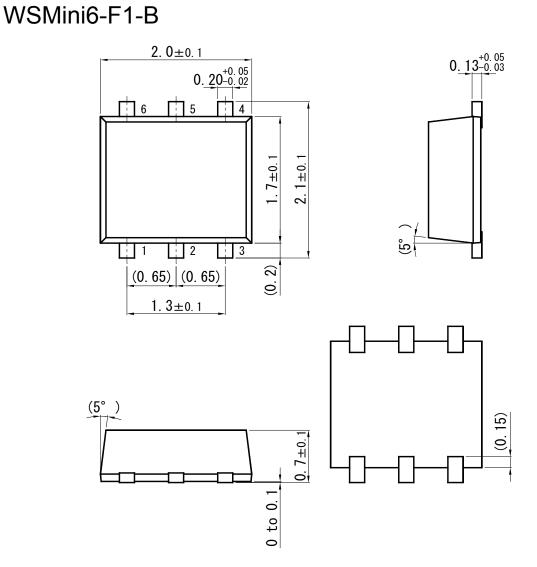
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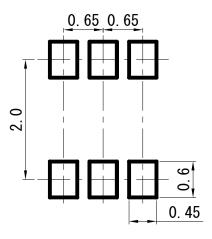


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Land Pattern (Reference) (Unit : mm)



Unit : mm

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