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# FL6L52030L

Silicon P-channel MOSFET(FET)  
Silicon epitaxial planar type(SBD)

For switching  
For DC-DC Converter

■ Features

- Low drain-source ON resistance :  $R_{DS(on)}$  typ. = 300 m $\Omega$  (  $V_{GS} = -4.0$  V )
- Low drive voltage : 2.5 V drive
- Halogen-free / RoHS compliant  
(EU RoHS / UL-94 V-0 / MSL:Level 1 compliant)

■ Marking Symbol Y3

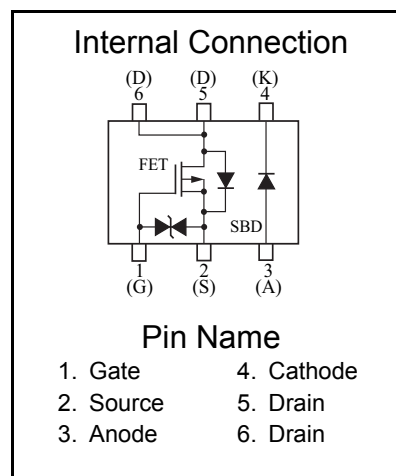
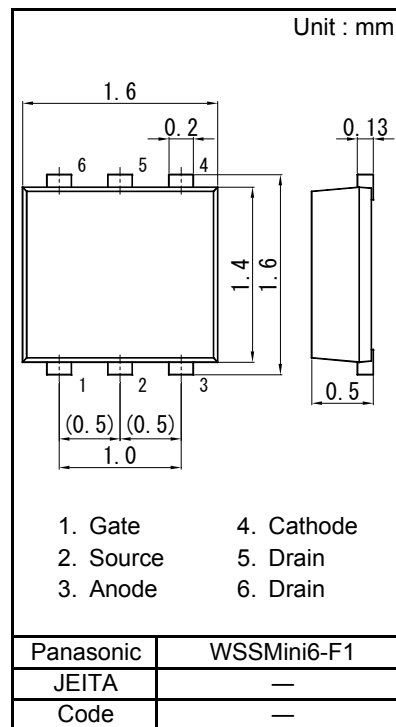
■ Packaging

Embossed type (Thermo-compression sealing) 10 000 pcs / reel (standard)

■ Absolute Maximum Ratings  $T_a = 25$  °C

項目		Symbol	Rating	Unit
FET	Drain to Source Voltage	V <sub>DS</sub>	-20	V
	Gate to Source Voltage	V <sub>GS</sub>	±12	V
	Drain current	I <sub>D</sub>	-1.0	A
	Peak drain current	I <sub>Dp</sub>	-4.0	A
	Channel temperature	T <sub>ch</sub>	150	°C
SBD	Reverse voltage	V <sub>R</sub>	20	V
	Forward current (Average)	I <sub>F(AV)</sub>	800	mA
	Junction temperature	T <sub>j</sub>	125	°C
Overall	Total power dissipation <sup>*1</sup>	PD	540	mW
	Operating ambient temperature	T <sub>opr</sub>	-40 to +85	°C
	Storage temperature	T <sub>stg</sub>	-55 to +125	°C

Note: \*1 Glass epoxy board (25.4 x 25.4 x t0.8 mm) coated with copper foil, which has more than 300mm<sup>2</sup>.  
PD absolute maximum rating without a heat sink: 150 mW



■ Electrical Characteristics Ta = 25 °C ± 3 °C  
FET (P-ch.)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-source surrender voltage	VDSS	ID = -1.0 mA, VGS = 0	-20			V
Drain-source cutoff current	IDSS	VDS = -20 V, VGS = 0			-1.0	μA
Gate-source cutoff current	IGSS	VGS = ±10 V, VDS = 0			±10	μA
Gate threshold voltage	VTH	ID = -1.0 mA, VDS = -10 V	-0.45	-1.0	-1.5	V
Drain-source ON resistance *1	RDS(on)	ID = -0.5 A, VGS = -4.0 V		300	420	mΩ
		ID = -0.5 A, VGS = -2.5 V		420	560	
Forward transfer admittance *1	Yfs	ID = -0.5 A, VDS = -10 V, f = 1 kHz	1.0			S
Short-circuit input capacitance (Common source)	Ciss	VDS = -10 V, VGS = 0 V, f = 1 MHz		80		pF
Short-circuit output capacitance (Common source)	Coss			12		
Reverse transfer capacitance (Common source)	Crss			12		
Turn-on delay time *2	td(on)	VDD = -15 V, VGS = 0 to -4.0 V		12		ns
Rise time *2	tr	ID = -0.5 A		6		
Turn-off delay time *2	td(off)	VDD = -15 V, VGS = -4.0 to 0 V		17		ns
Fall time *2	tf	ID = -0.5 A		10		

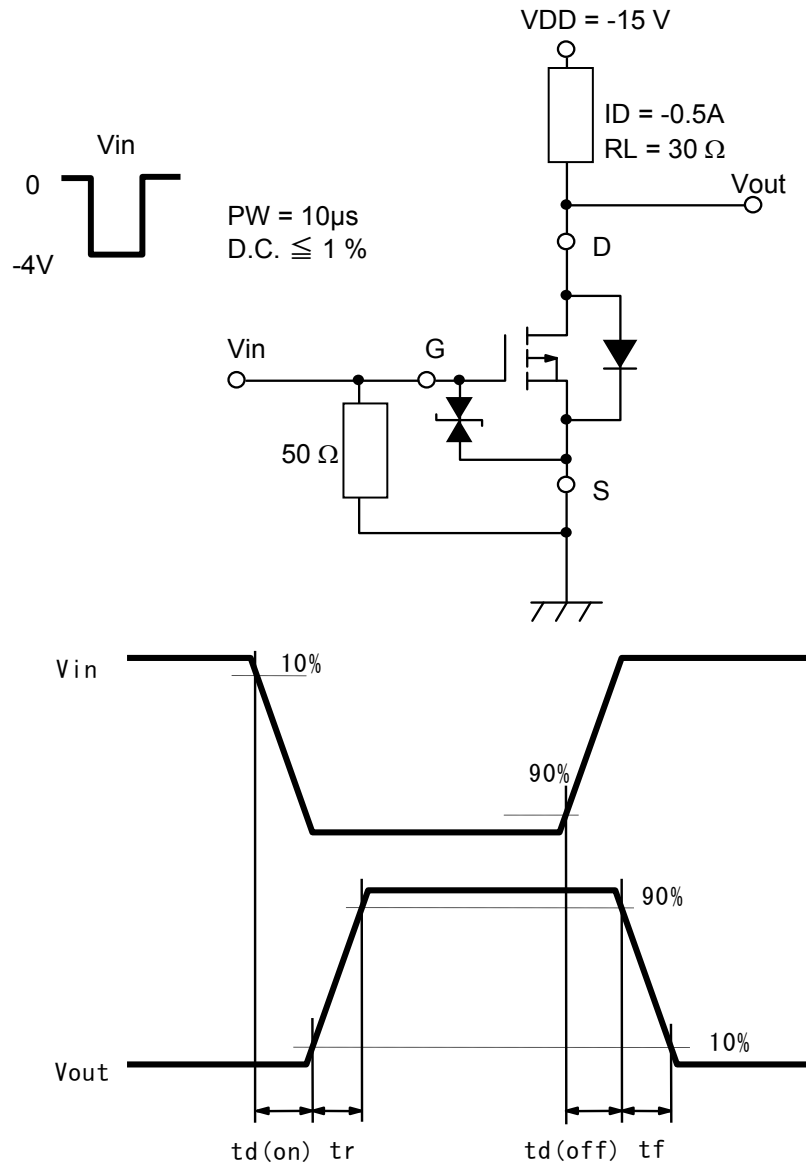
Note: 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.  
2. \*1 Pulse measurement  
\*2 Measurement circuit for Turn-on Delay Time/Rise Time/Turn-off Delay Time/Fall Time

SBD

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Forward voltage	VF	IF = 800 mA			0.47	V
Reverse current	IR	VR = 20 V			80	μA

Note: Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7031 Measuring methods for diodes.

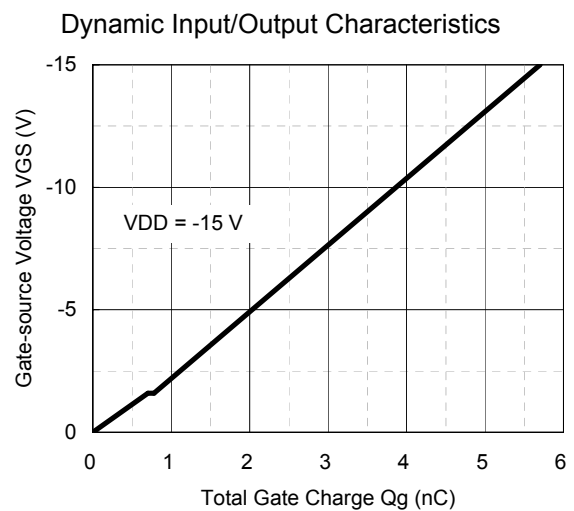
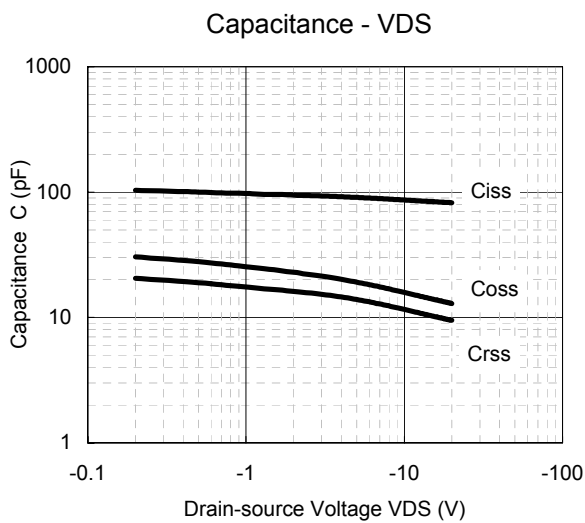
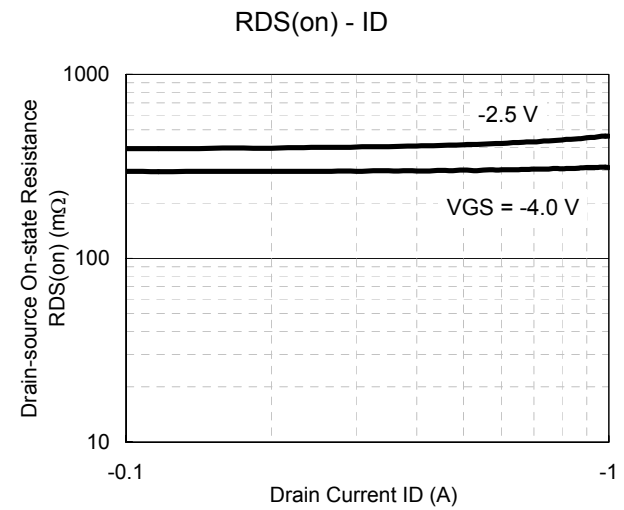
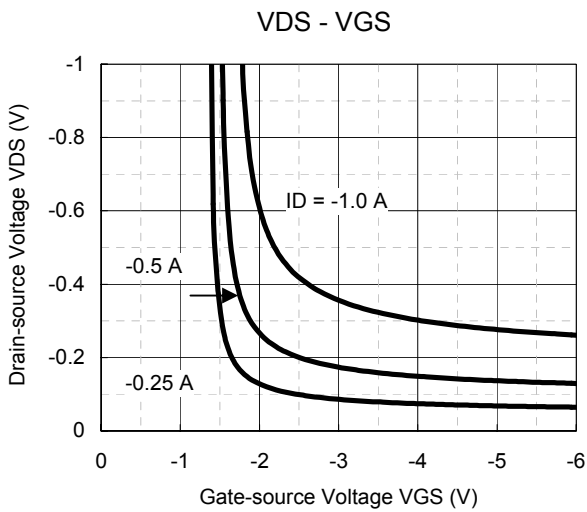
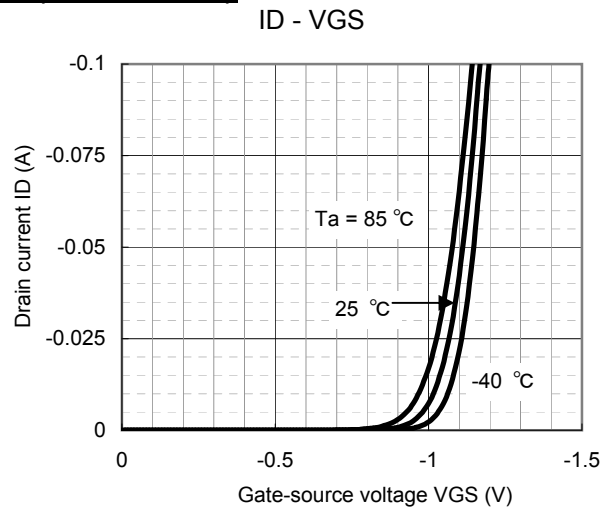
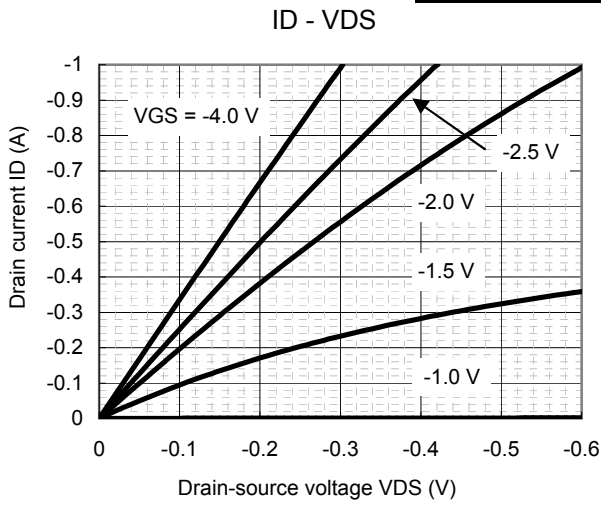
\*2 Measurement circuit for Turn-on Delay Time/Rise Time/Turn-off Delay Time/Fall Time





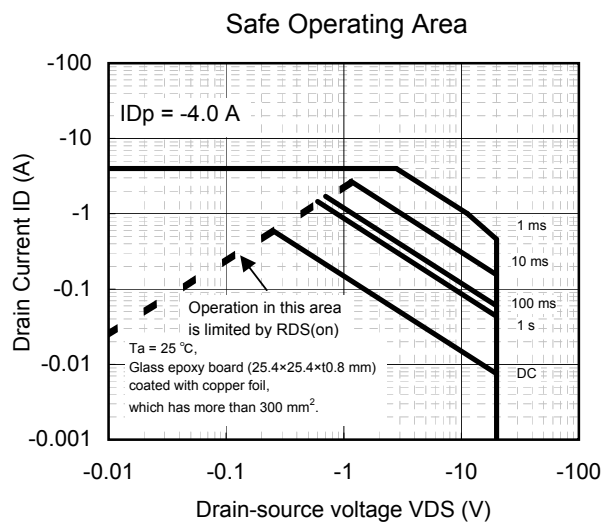
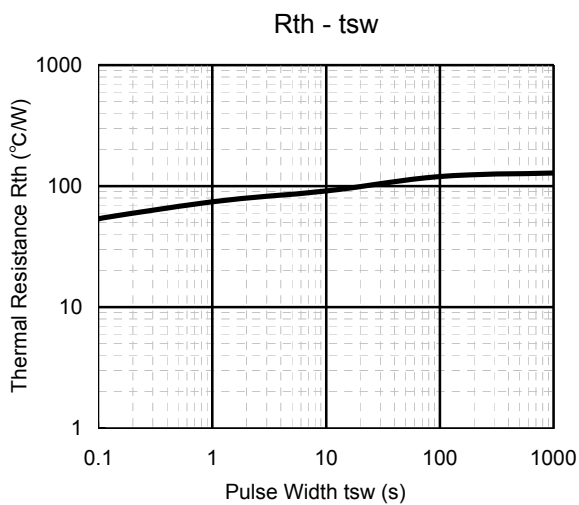
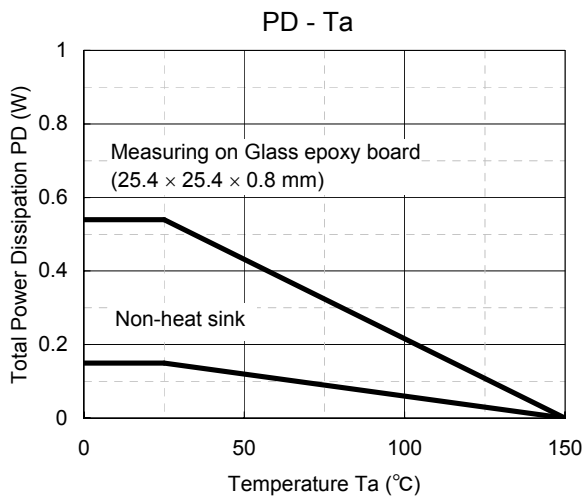
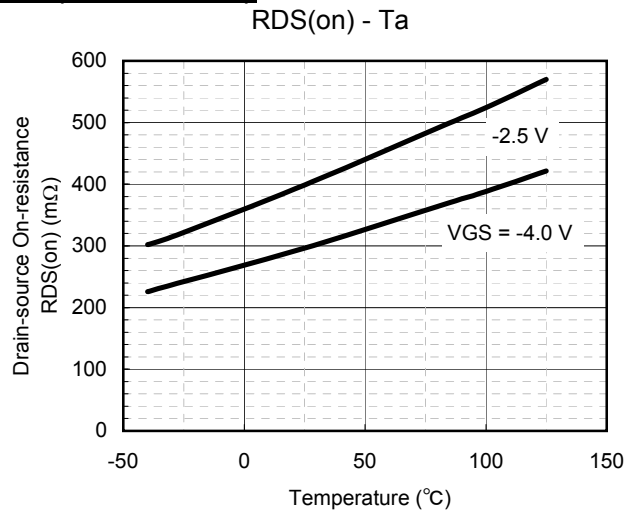
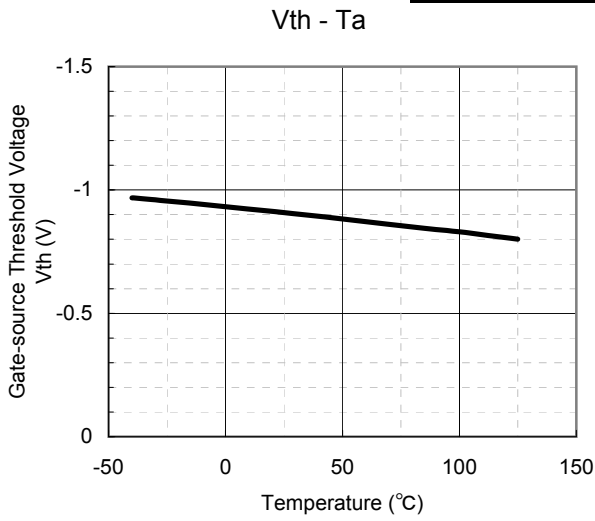


Technical Data ( reference )



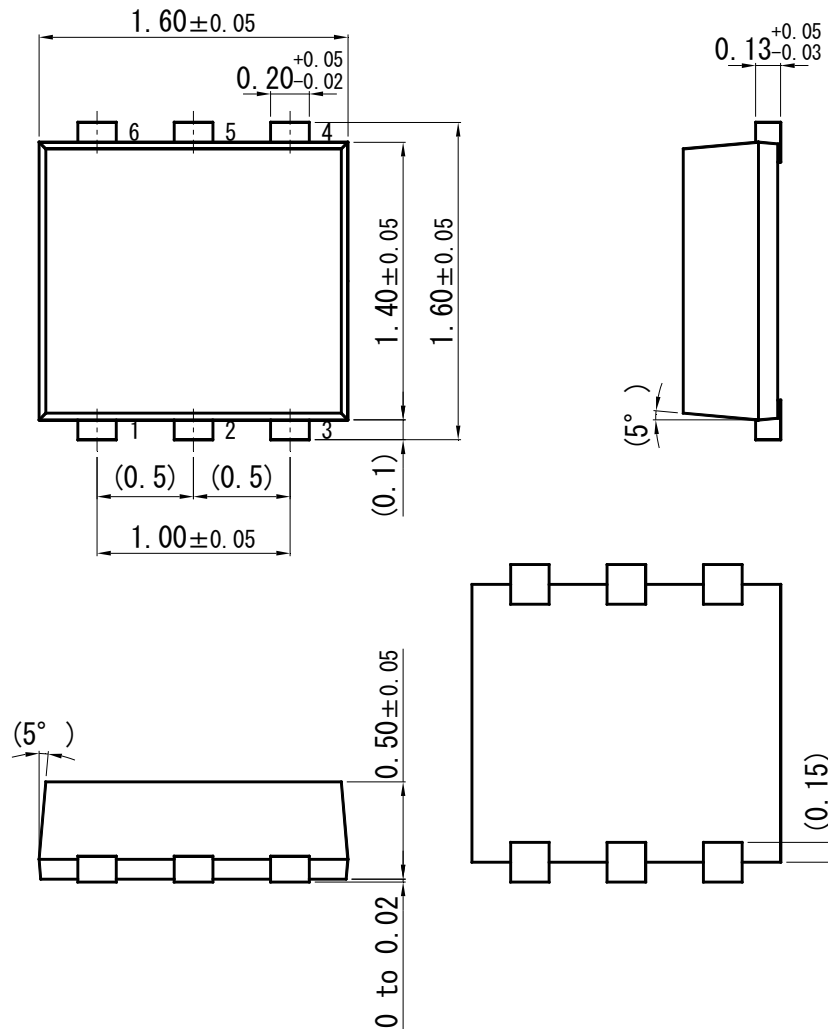


Technical Data ( reference )

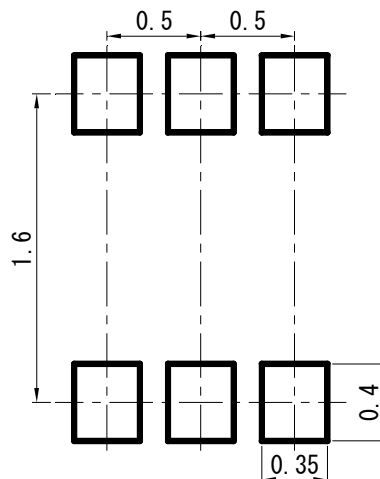


WSSMini6-F1

Unit: mm



■ Land Pattern (Reference) (Unit : mm)



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