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MOS FET

FL6L52060L

### **Panasonic**

### FL6L52060L

Silicon P-channel MOSFET(FET) Silicon epitaxial planar type(SBD)

# For switching For DC-DC Converter

#### ■ Features

• Low drain-source ON resistance : RDS (on) typ. = 80 m $\Omega$  ( VGS = -4.0 V )

• Low drive voltage: 1.8 V drive

 Halogen-free / RoHS compliant (EU RoHS / UL-94 V-0 / MSL:Level 1 compliant)

■ Marking Symbol : Y2

Established: 2011-05-16

: 2013-10-18

Revised

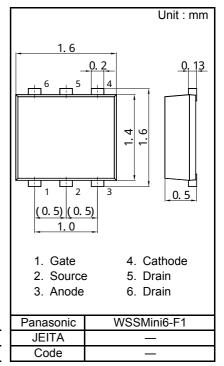
#### Packaging

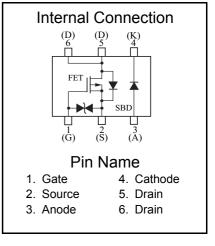
Embossed type (Thermo-compression sealing): 10 000 pcs / reel (standard)

■ Absolute Maximum Ratings Ta = 25 °C

項目		Symbol	Rating	Unit	
FET	Drain to Source Voltage	VDS	-20	V	
	Gate to Source Voltage	VGS	±10	V	
	Drain current	ID	-2.0	Α	
	Peak drain current	IDp	-8.0	Α	
	Channel temperature	Tch	150	°C	
SBD	Reverse voltage	VR	20	V	
	Forward current (Average)	IF(AV)	700	mA	
	Junction temperature	Tj	125	°C	
Overall	Total power dissipation *1	PD	540	mW	
	Operating ambient temperature	Topr	-40 to + 85	°C	
	Storage temperature	Tstg	-55 to +125	°C	

Note: \*1 Measuring on ceramic substrate at 40 mm × 38 mm × 0.2 mm
PD absolute maximum rating without a heat shink: 150 mW





Revision. 2

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■ Electrical Characteristics Ta = 25 °C ± 3 °C FET (P-ch.)

1 = 1 (1 011.)						
Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Drain-source surrender voltage	VDSS	ID = -1.0 mA, VGS = 0 V	-20			V
Drain-source cutoff current	IDSS	VDS = -20 V, VGS = 0 V			-1.0	μΑ
Gate-source cutoff current	IGSS	VGS = ±8 V, VDS = 0 V			±10	μA
Gate threshold voltage	VTH	ID = -1.0 mA, VDS = -10 V	-0.4	-0.75	-1.1	V
	RDS(on)1	ID = -1.0 A, VGS = -4.0 V		80	120	
Drain-source ON resistance *1	RDS(on)2	ID = -1.0 A, VGS = -2.5 V		100	170	$m\Omega$
	RDS(on)3	ID = -0.5 A, VGS = -1.8 V		140	230	
Forward transfer admittance *1	Yfs	ID = -1.0 A, VDS = -10 V, f = 1 kHz	3.0			S
Short-circuit input capacitance (Common source)	Ciss			300		
Short-circuit output capacitance (Common source)	Coss	VDS = -10 V, VGS = 0, f = 1 MHz		30		pF
Reverse transfer capacitance (Common source)	Crss			35		
Turn-on delay time *2	td(on)	VDD = -10 V, VGS = 0 V to - 4.0 V		6		no
Rise time *2	tr	ID = -1.0 A		8		ns
Turn-off delay time *2	td(off)	VDD = -10 V, VGS = -4.0 V to 0 V		57		no
Fall time *2	tf	ID = -1.0 A		55		ns

Note: 1. Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

#### **SBD**

Parameter	Symbol	Conditions	Min	Тур	Max	Unit
Forward voltage	VF1	IF = 10 mA			0.4	V
Forward voitage	VF2	IF = 500 mA			0.55	
Dovorce current	IR1	VR = 5 V			1	
Reverse current	IR2	VR = 10 V			10	μΑ

Note: Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7031 Measuring methods for diodes.

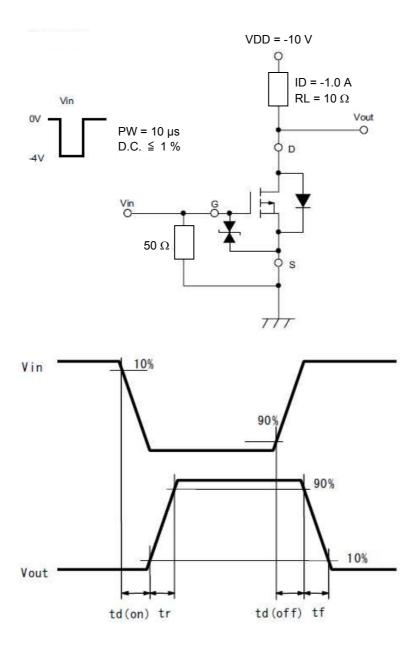
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<sup>2. \*1</sup> Pulse measurement

<sup>\*2</sup> Measurement circuit for Turn-on Delay Time/Rise Time/Turn-off Delay Time/Fall Time

# **Panasonic**

\*2 Measurement circuit for Turn-on Delay Time/Rise Time/Turn-off Delay Time/Fall Time



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MOS FET FL6L52060L

### **Panasonic**

#### Technical Data (reference) ID - VDS ID - VGS -2 -0.1 -4.0 V -2.5 V Drain current ID (A) Drain current ID (A) -1.5 -0.075 -2.0 V Ta = 85 °C -1 -0.05 25 °C -0.5 VGS = -1.0 V -0.025 -40 °C 0 0 0 -0.2 -0.3 -0.4 -0.1 0 -0.2 -0.4 -0.8 Drain-source Voltage VDS (V) Gate-source voltage VGS (V) VDS - VGS RDS(on) - ID 1000 -1.5 Drain-source On-state Resistance Drain-source Voltage VDS (V) $RDS(on) (m\Omega)$ -1.8 V -1 ID = -2.0 mA-2.5 V -0.5 VGS = -4.0 V -0.5 mA 10 0 -0.1 -1 -10 0 -2 -1 -3 Drain current ID (A) Gate-source Voltage VGS (V) Capacitance - VDS **Dynamic Input/Output Characteristics** 1000 Gate-source Voltage VGS (V) -8 Capacitance C (pF) Ciss VDD = -10 V -6 100 -4 Coss -2 Crss

0

-100

Drain-source voltage VDS (V)

2

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8

6

Total Gate Charge Qg (nC)

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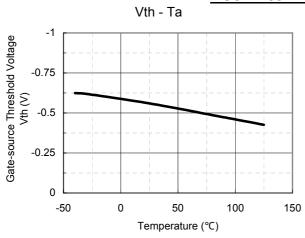
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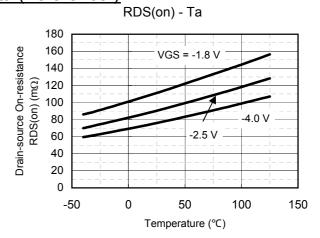
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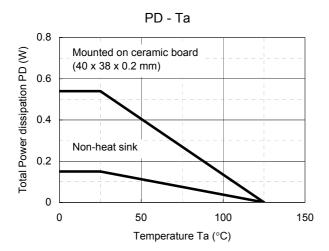
# **Panasonic**

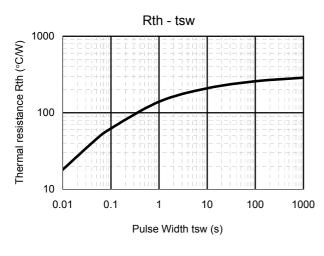
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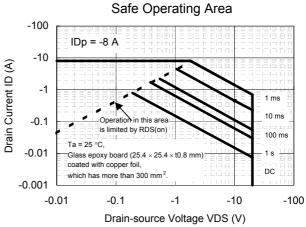
### Technical Data (reference)









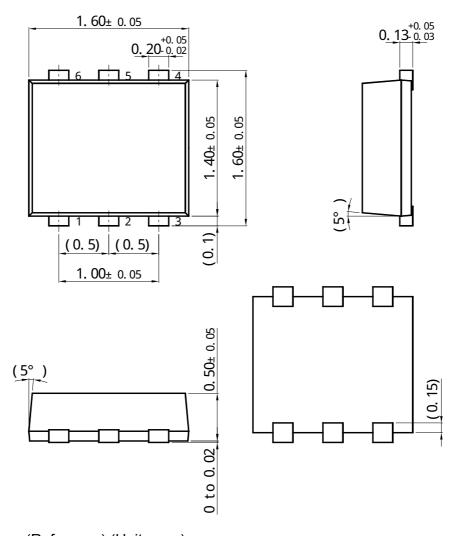


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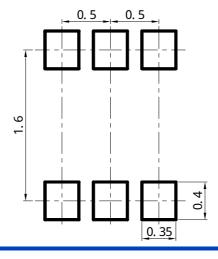
MOS FET FL6L52060L

WSSMini6-F1

Unit: mm



■ Land Pattern (Reference) (Unit : mm)



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