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256Mb Async./Burst/Sync./A/D MUX

1. GENERAL DESCRIPTION

Winbond x16 ADMUX products are high-speed, CMOS pseudo-static random access memory developed for low-power, portable applications. The device has a DRAM core organized. These devices are a variation of the industry-standard Flash control interface, with a multiplexed address/data bus. The multiplexed address and data functionality dramatically reduce the required signal count, and increase READ/WRITE bandwidth.

For seamless operation on a burst Flash bus, Winbond x16 ADMUX products incorporate a transparent self-refresh mechanism. The hidden refresh requires no additional support from the system memory controller and has no significant impact on device READ/WRITE performance.

Two user-accessible control registers define device operation. The bus configuration register (BCR) defines how the Winbond x16 ADMUX device interacts with the system memory bus and is nearly identical to its counterpart on burst mode Flash devices. The refresh configuration register (RCR) is used to control how refresh is performed on the DRAM array. These registers are automatically loaded with default settings during power-up and can be updated anytime during normal operation.

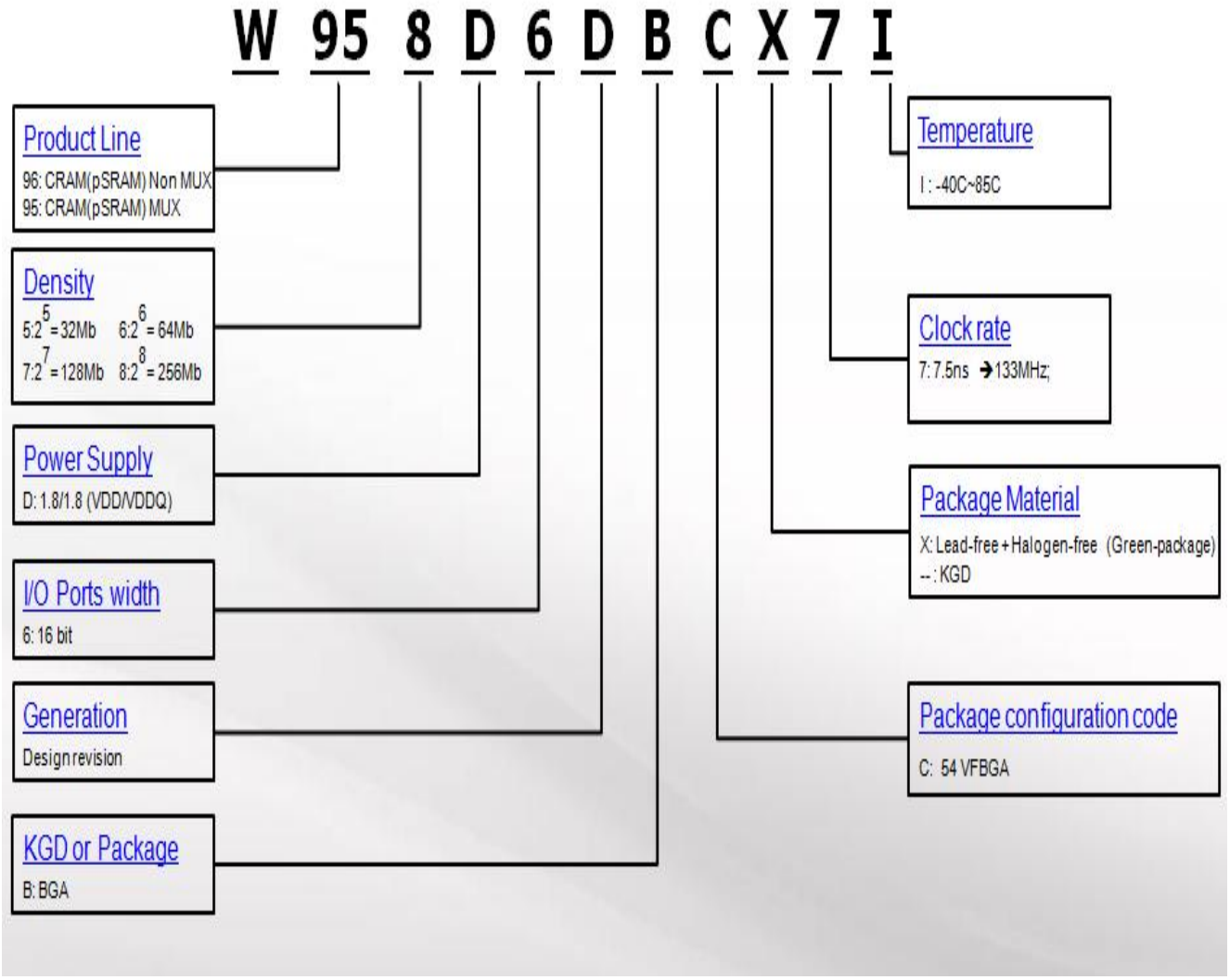
Special attention has been focused on standby current consumption during self refresh. Winbond x16 ADMUX products include two mechanisms to minimize standby current. Partial-array refresh (PAR) enables the system to limit refresh to only that part of the DRAM array that contains essential data. Temperature-compensated refresh (TCR) uses an on-chip sensor to adjust the refresh rate to match the device temperature—the refresh rate decreases at lower temperatures to minimize current consumption during standby. The system-configurable refresh mechanisms are accessed through the RCR.

Winbond x16 ADMUX is compliant with the industry-standard CellularRAM 1.5 x16 A/D MUX.

2. FEATURES

- •Supports asynchronous and burst operations
- • VCC, VCCQ Voltages:
  1.7V–1.95V VCC
  1.7V–1.95V VCCQ
- • Random access time: 70ns
- • Burst mode READ and WRITE access:
  4, 8, 16, or 32 words, or continuous burst
  Burst wrap or sequential
  Max clock rate: 133 MHz (tCLK = 7.5ns)
- • Low power consumption:
  Asynchronous READ: <25 mA
  Continuous burst READ: <35 mA
  Standby current: 400µA
- • Low-power features
  On-chip temperature compensated refresh (TCR)
  Partial array refresh (PAR)
  Deep power-down (DPD) mode
- • Package: 54 Ball VFBGA
- • 16-bit multiplexed address/data bus
- • Operating temperature range : -40°C~85°C

3. ORDERING INFORMATION



Part Number	VDD/VDDQ	I/O Width	Type	Others
W958D6DBCX7I	1.8/1.8	x16	PKG	CRAM A/D MUX,133MHz, -40°C~85°C

TABLE OF CONTENTS

4. PIN CONFIGURATION

4.1 Ball Assignment

	1	2	3	4	5	6
A	LB#	OE#	NC	NC	NC	CRE
B	ADQ8	UB#	NC	NC	CE#	ADQ0
C	ADQ9	ADQ10	NC	NC	ADQ1	ADQ2
D	VSSQ	ADQ11	A17	NC	ADQ3	VCC
E	VCCQ	ADQ12	A21	A16	ADQ4	VSS
F	ADQ14	ADQ13	NC	NC	ADQ5	ADQ6
G	ADQ15	A19	NC	NC	WE#	ADQ7
H	A18	NC	NC	NC	NC	A20
J	WAIT	CLK	ADV#	A22	A23	NC

(Top View) Pin Configuration

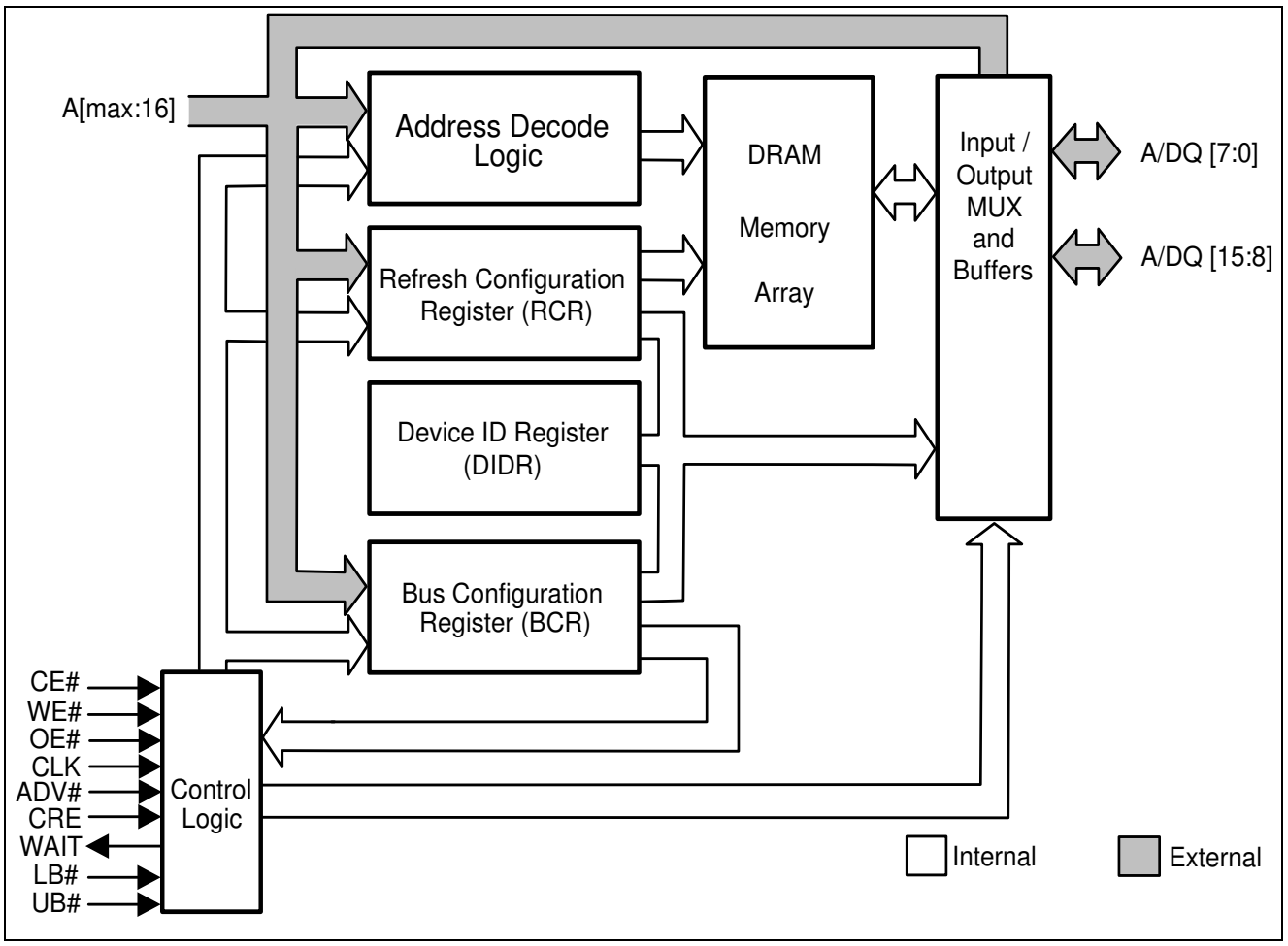
5. PIN DESCRIPTION

5.1 Signal Description

Symbol	Type	Description
A[max:16]	Input	Address inputs: Inputs for addresses during READ and WRITE operations. Addresses are internally latched during READ and WRITE cycles. The address lines are also used to define the value to be loaded into the BCR or the RCR. A[max:16]= A[23:16] (256Mb).
CLK (Note 1)	Input	Clock: Synchronizes the memory to the system operating frequency during synchronous operations. When configured for synchronous operation, the address is latched on the first rising CLK edge when ADV# is active. CLK must be static (HIGH or LOW) during asynchronous access READ and WRITE operations when burst mode is enabled.
ADV# (Note 1)	Input	Address valid: Indicates that a valid address is present on the address inputs. Addresses are latched on the rising edge of ADV# during asynchronous READ and WRITE operations.
CRE	Input	Control register enable: When CRE is HIGH, WRITE operations load the RCR or BCR, and READ operations access the RCR, BCR, or DIDR.
CE#	Input	Chip enable: Activates the device when LOW. When CE# is HIGH, the device is disabled and goes into standby mode.
OE#	Input	Output enable: Enables the output buffers when LOW. When OE# is HIGH, the output buffers are disabled.
WE#	Input	Write enable: Determines if a given cycle is a WRITE cycle. If WE# is LOW, the cycle is a WRITE to either a configuration register or to the memory array.
LB#	Input	Lower byte enable. DQ[7:0].
UB#	Input	Upper byte enable. DQ[15:8].
A/DQ[15:0]	Input/Output	Address/data I/Os: These pins are a multiplexed address/data bus. As inputs for addresses, these pins behave as A[15:0]. A[0] is the LSB of the 16-bit word address within the CellularRAM device. Address, RCR, and BCR values are loaded with ADV# LOW. Data is input or output when ADV# is HIGH.
WAIT (Note 1)	Output	WAIT: Provides data-valid feedback during burst READ and WRITE operations. WAIT is used to arbitrate collisions between refresh and READ/WRITE operations. WAIT is also asserted at the end of a row unless wrapping within the burst length. WAIT should be ignored during asynchronous operations. WAIT is High-Z when CE# is HIGH.
NC	—	Reserved for future use.
VCC	Supply	Device power supply: Power supply for device core operation.
VCCQ	Supply	I/O power supply: Power supply for input/output buffers.
VSS	Supply	VSS must be connected to ground.
VSSQ	Supply	VSSQ must be connected to ground.

Notes: 1. When using asynchronous mode exclusively, CLK can be tied to VSSQ or VCCQ . WAIT should be ignored during asynchronous mode operations.

6. BLOCK DIAGRAM



7. INSTRUCTION SET

7.1 Bus Operation

Asynchronous Mode BCR[15] = 1 (default)	Power	CLK	ADV#	CE#	OE#	WE#	CRE	LB#/ UB#	WAIT*2	A/DQ[15:0]*3	Notes
Read	Active	X	⊓	L	L	H	L	L	Low-Z	Data out	4
Write	Active	X	⊓	L	X	L	L	L	High-Z	Data in	4
Standby	Standby	H or L	X	H	X	X	L	X	High-Z	High-Z	5, 6
No operation	Idle	X	X	L	X	X	L	X	Low-Z	X	4, 6
Configuration register WRITE	Active	X	⊓	L	H	L	H	X	Low-Z	High-Z	
Configuration register READ	Active	X	⊓	L	L	H	H	L	Low-Z	Config. reg. out	
DPD	Deep power-down	X	X	H	X	X	X	X	High-Z	High-Z	10
Burst Mode BCR[15] = 0	**Power**	**CLK*1**	**ADV#**	**CE#**	**OE#**	**WE#**	**CRE**	**LB#/ UB#**	**WAIT*2**	**A/DQ[15:0]*3**	**Notes**
Read	Active	H or L	⊓	L	L	H	L	L	Low-Z	Data out	4, 7
Write	Active	H or L	⊓	L	X	L	L	L	High-Z	Data in	4
Standby	Standby	H or L	X	H	X	X	L	X	High-Z	High-Z	5, 6
No operation	Idle	H or L	X	L	X	X	L	X	Low-Z	X	4, 6
Initial burst READ	Active	⊓	L	L	X	H	L	L	Low-Z	Address	4, 8
Initial burst WRITE	Active	⊓	L	L	H	L	L	X	Low-Z	Address	4, 8
Burst continue	Active	⊓	H	L	X	X	X	L	Low-Z	Data in or Data out	4, 8
Configuration register WRITE	Active	⊓	L	L	H	L	H	X	Low-Z	High-Z	8, 9
Configuration register READ	Active	⊓	L	L	L	H	H	L	Low-Z	Config. reg. out	8, 9
DPD	Deep power-down	L	X	H	X	X	X	X	High-Z	High-Z	10

Notes: 1. With burst mode enabled, CLK must be static (HIGH or LOW) during asynchronous READs and asynchronous WRITEs and to achieve standby power during standby mode.

2. The WAIT polarity is configured through the bus configuration register (BCR[10]).
3. When LB# and UB# are in select mode (LOW), DQ[15:0] are enabled. When only LB# is in select mode, DQ[7:0] are enabled. When only UB# is in the select mode, DQ[15:8] are enabled.
4. The device will consume active power in this mode whenever addresses are changed.
5. When the device is in standby mode, address inputs and data inputs/outputs are internally isolated from any external influence.
6. VIN = VCCQ or 0V; all device balls must be static (unswitched) in order to achieve standby current.
7. When the BCR is configured for synchronous mode, synchronous READ and WRITE and asynchronous WRITE and READ are supported.
8. Burst mode operation is initialized through the bus configuration register (BCR[15]).
9. Initial cycle. Following cycles are the same as BURST CONTINUE. CE# must stay LOW for the equivalent of a single-word burst (as indicated by WAIT).
10. DPD is initiated when CE# transitions from LOW to HIGH after writing RCR[4] to 0. DPD is maintained until CE# transitions from HIGH to LOW.

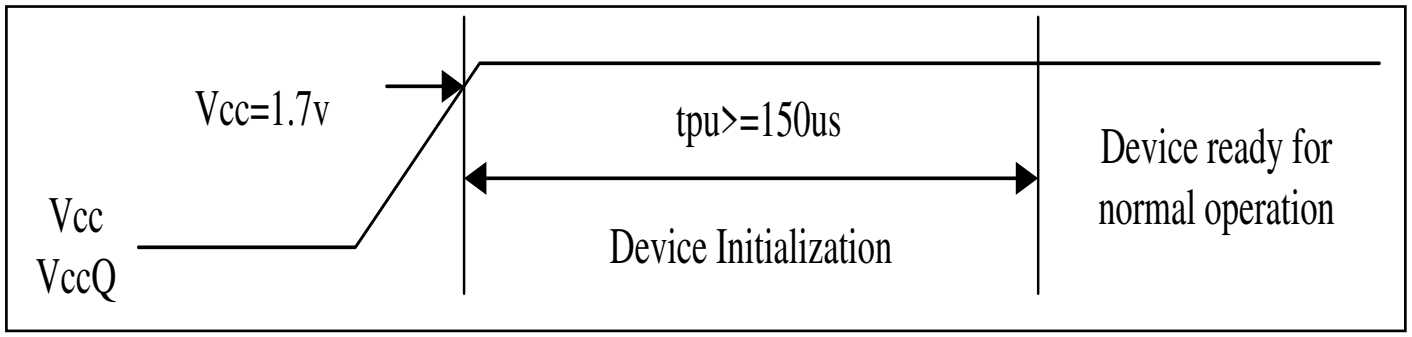
8. FUNCTIONAL DESCRIPTION

In general, ADMUX PSRAM devices are high-density alternatives to SRAM and Pseudo SRAM products, popular in low-power, portable applications. Both devices implement a multiplexed address/data bus. This multiplexed configuration supports greater bandwidth through the x16 data bus, yet still reduces the required signal count. The ADMUX PSRAM bus interface supports both asynchronous and burst mode transfers.

8.1 Power Up Initialization

ADMUX PRAM products include an on-chip voltage sensor used to launch the power-up initialization process. Initialization will configure the BCR and the RCR with their default settings. VCC and VCCQ must be applied simultaneously. When they reach a stable level at or above 1.7V, the device will require 150µs to complete its self-initialization process. During the initialization period, CE# should remain HIGH. When initialization is complete, the device is ready for normal operation.

8.1.1 Power-Up Initialization Timing



8.2 Bus Operating Modes

This asynchronous/burst ADMUX PSRAM products incorporate a burst mode interface found on Flash products targeting low-power, wireless applications. This bus interface supports asynchronous, and burst mode read and write transfers. The specific interface supported is defined by the value loaded into the BCR.

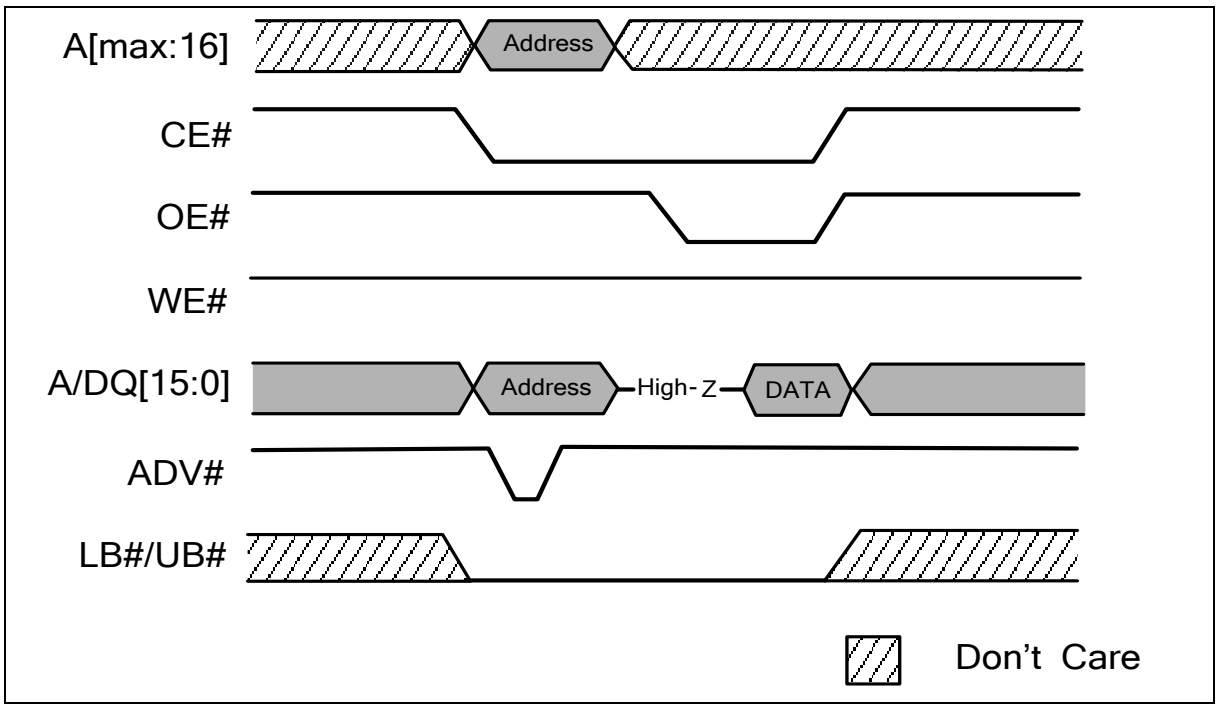
8.2.1 Asynchronous Modes

Using industry-standard SRAM control signals (CE#, ADV#, OE#, WE#, and LB#/UB#). READ operations are initiated by bringing CE#, ADV#, and LB#/UB# LOW while keeping OE# and WE# HIGH, and driving the address onto the A/DQ bus. ADV# is taken HIGH to capture the address, and OE# is taken LOW. Valid data will be driven out of the I/Os after the specified access time has elapsed.

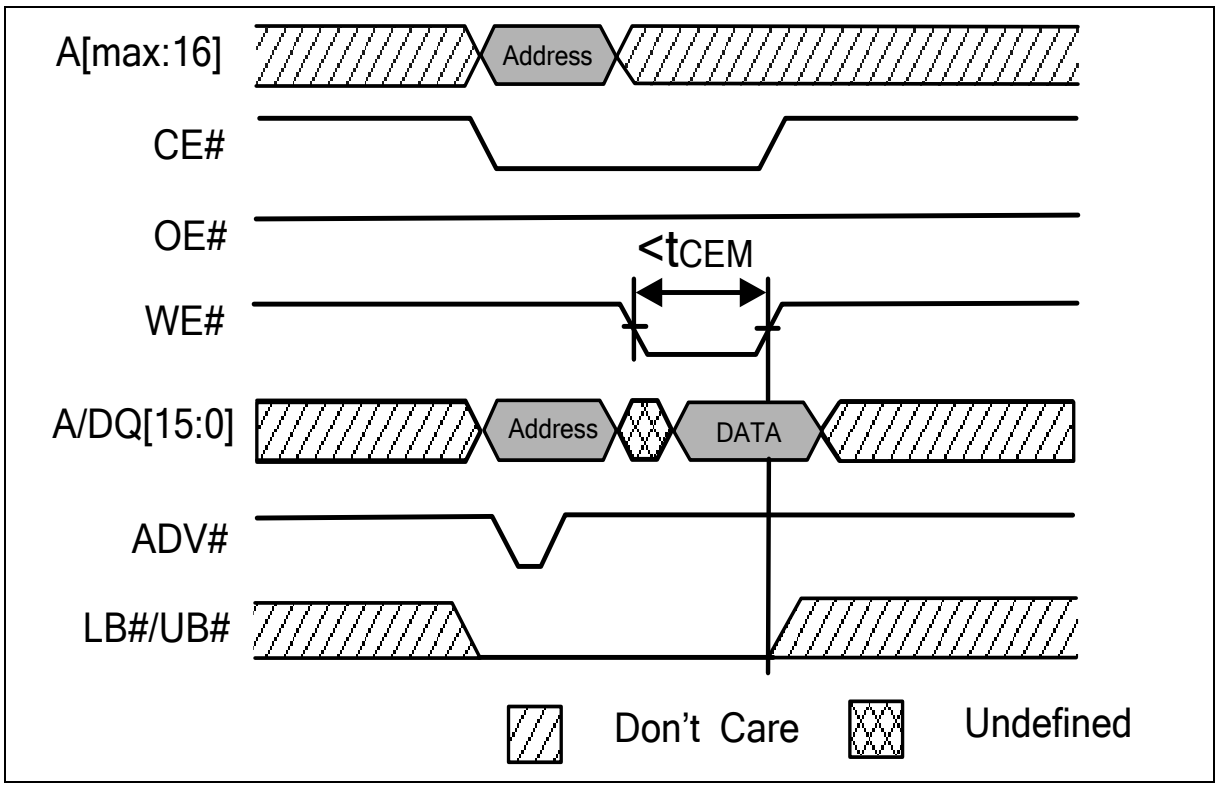
WRITE operations occur when CE#, ADV#, WE#, and LB#/UB# are driven LOW with the address on the A/DQ bus. ADV# is taken HIGH to capture the address, then the WRITE data is driven onto the bus. During asynchronous WRITE operations, the OE# level is a “Don't Care,” and WE# will override OE#; however, OE# must be HIGH while the address is driven onto the A/DQ bus. The data to be written is latched on the rising edge of CE#, WE#, UB#, or LB# (whichever occurs first).

During asynchronous operation with burst mode enabled, the CLK input must be held static (HIGH or LOW). WAIT will be driven during asynchronous READs, and its state should be ignored. WE# LOW time must be limited to tCEM.

8.2.1.1 READ Operation (ADV# LOW)



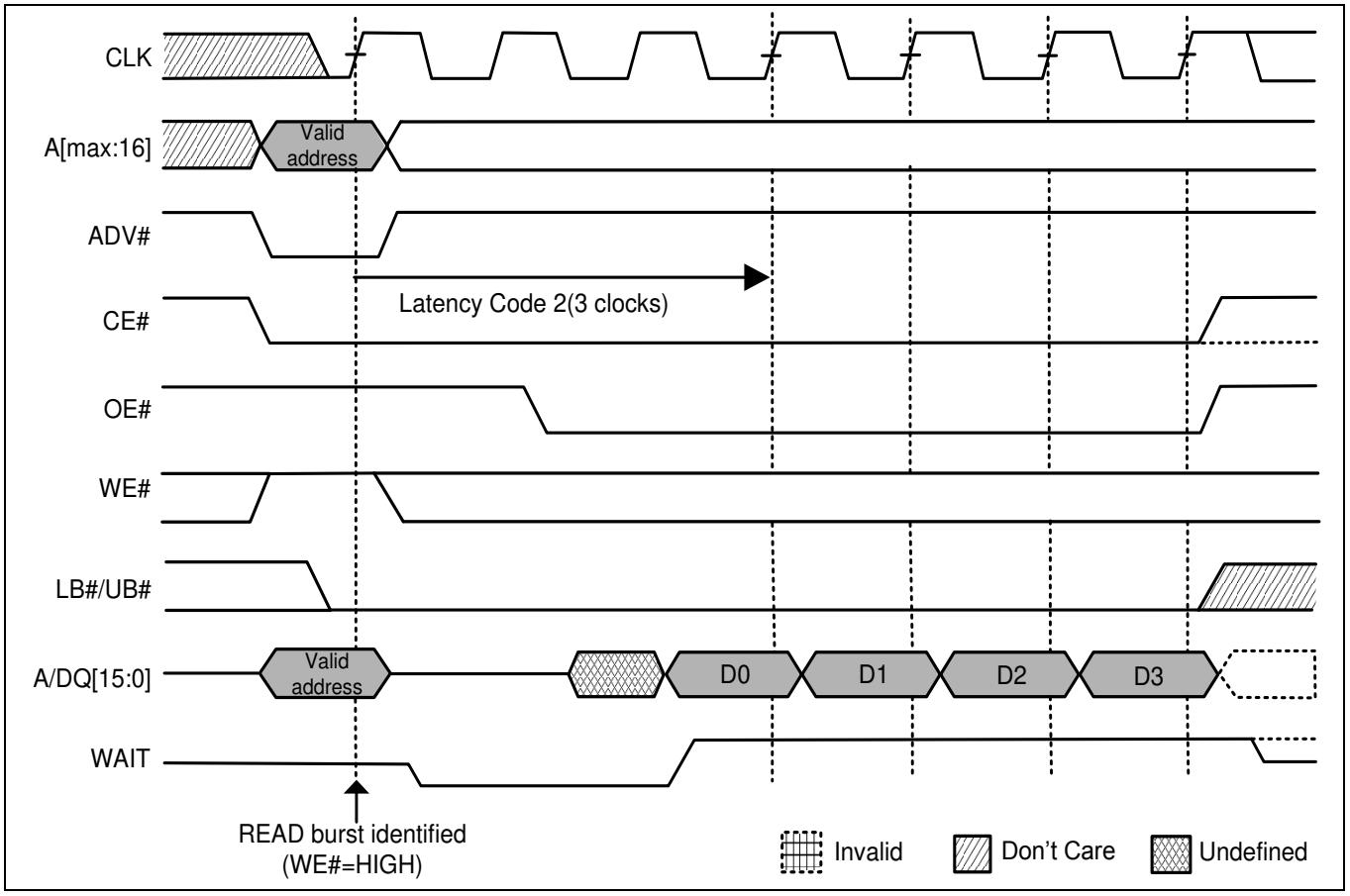
8.2.1.2 WRITE Operation (ADV# LOW)



8.2.2 Burst Mode Operation

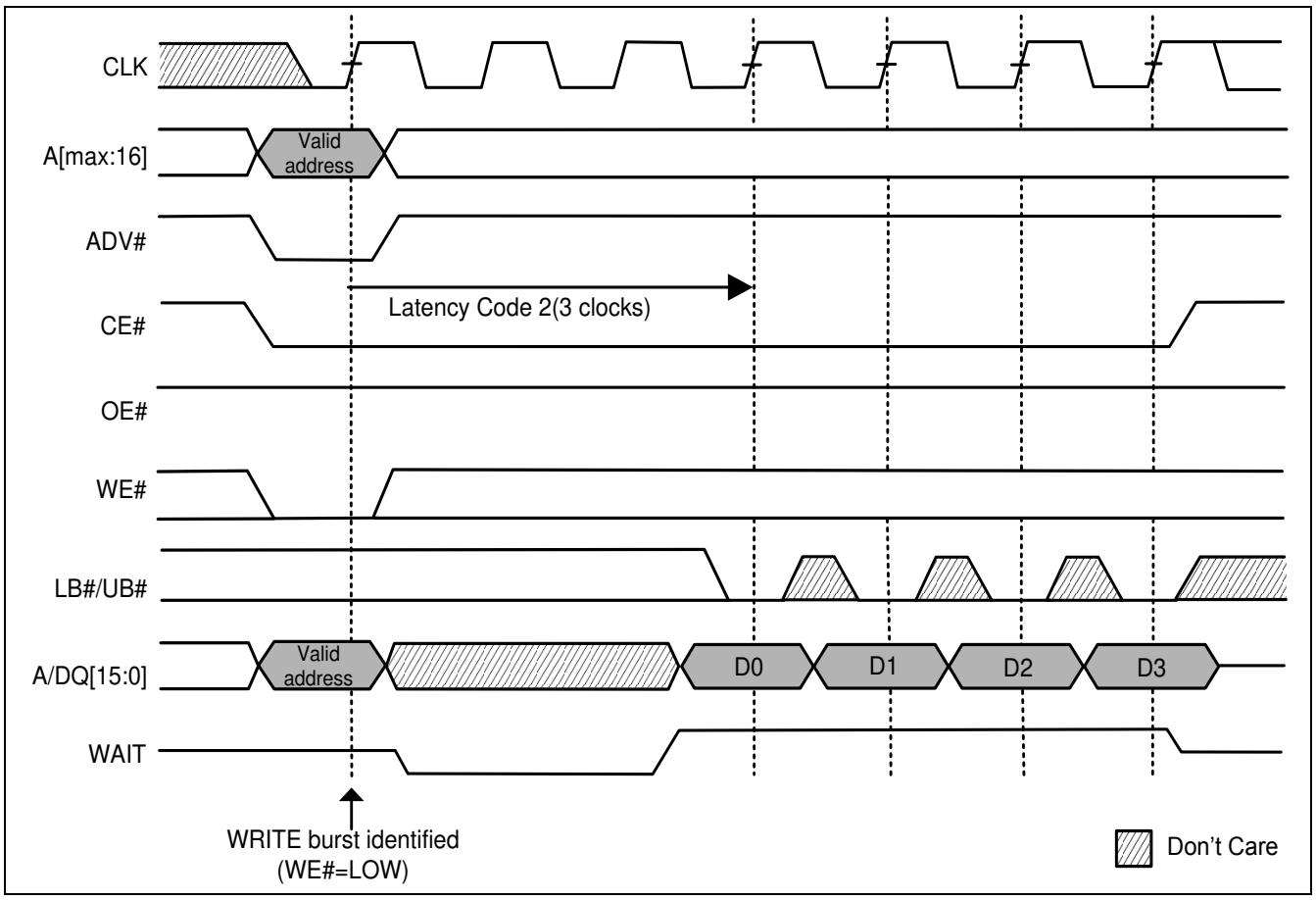
Burst mode operations enable high-speed synchronous READ and WRITE operations. Burst operations consist of a multi-clock sequence that must be performed in an ordered fashion. After CE# goes LOW, the address to access is latched on the first CLK edge after ADV# LOW. During this first clock rising edge, WE# indicates whether the operation is going to be a READ (WE# = HIGH) or WRITE (WE# =LOW).

8.2.2.1 Burst Mode READ (4-word burst)



Note : Non-default BCR settings for burst mode READ (4-word burst): fixed or variable latency, Latency code 2 (3 clocks), WAIT active Low, WAIT asserted during delay. Diagram is representative of variable latency with no refresh collision or fixed-latency access.

8.2.2.2 Burst Mode WRITE (4-word burst)



Note : Non-default BCR settings for burst mode WRITE (4-word burst) : fixed or variable latency , latency code 2(3 clocks) , WAIT active LOW , WAIT asserted during delay.

The size of a burst can be specified in the BCR either as a fixed length or continuous. Fixed-length bursts consist of 4, 8, 16, or 32 words. Continuous bursts have the ability to start at a specified address and burst to the end of the address. It goes back to the first address and continues to burst when continuous bursts meet the end of address.

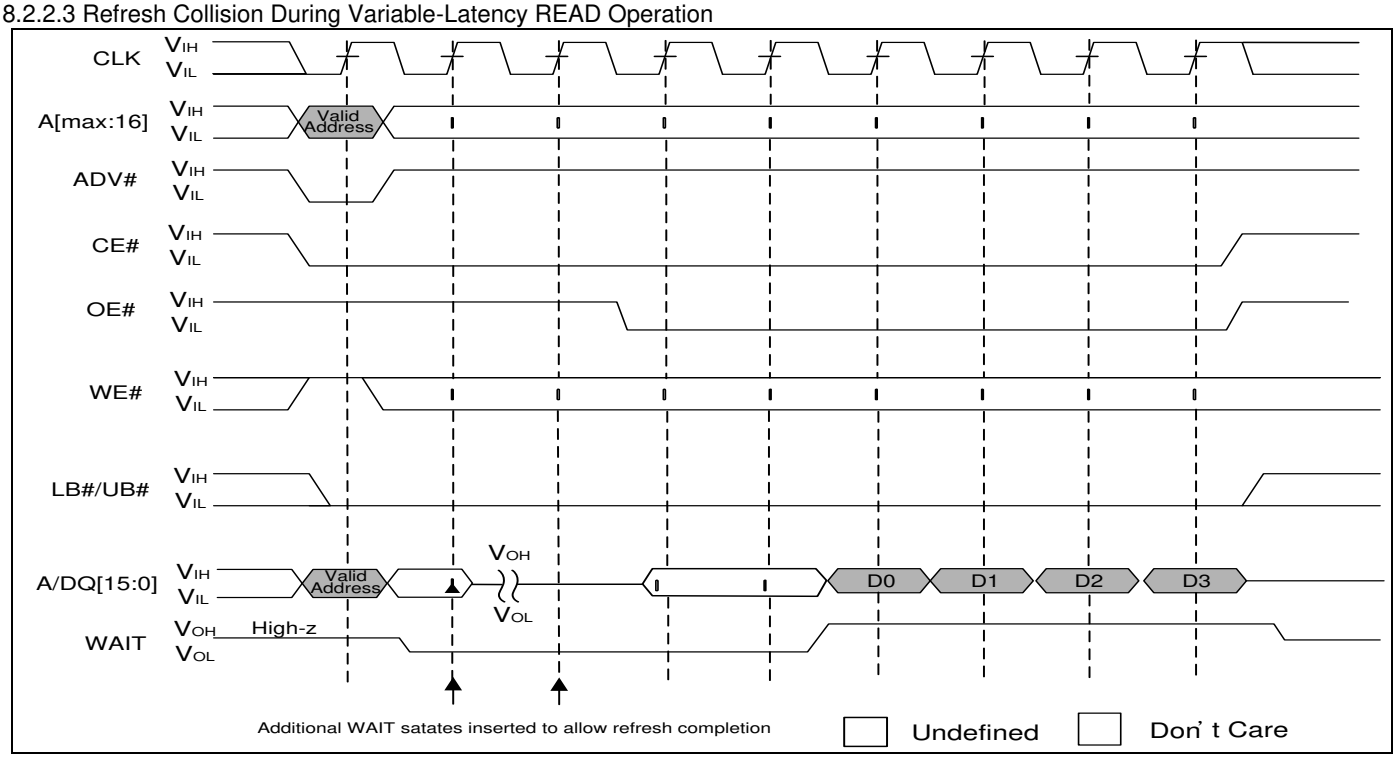
The latency count stored in the BCR defines the number of clock cycles that elapse before the initial data value is transferred between the processor and ADMUX PSRAM device. The initial latency for READ operations can be configured as fixed or variable (WRITE operations always use fixed latency). Variable latency allows the ADMUX PSRAM to be configured for minimum latency at high clock frequencies, but the controller must monitor WAIT to detect any conflict with refresh cycles.

Fixed latency outputs the first data word after the worst-case access delay, including allowance for refresh collisions. The initial latency time and clock speed determine the latency count setting. Fixed latency is used when the controller cannot monitor WAIT. Fixed latency also provides improved performance at lower clock frequencies.

The WAIT output asserts when a burst is initiated, and de-asserts to indicate when data is to be transferred into (or out of) the memory. WAIT will again be asserted at the boundary of the row, unless wrapping within the burst length. With wrap off, the ADMUX PSRAM device will restore the previous row's data and access the next row, WAIT will be de-asserted, and the burst can continue across the row boundary. If the burst is to terminate at the row boundary, CE# must go HIGH within 2 clocks of the last data. CE# must go HIGH before any clock edge following the last word of a defined-length burst WRITE.

The CE# LOW time is limited by refresh considerations. CE# must not stay LOW longer than tCEM. If a burst suspension will cause CE# to remain LOW for longer than tCEM, CE# should be taken HIGH and the burst restarted with a new CE# LOW/ADV# LOW cycle.

8.2.2.3 Refresh Collision During Variable-Latency READ Operation



Note : Non-default BCR settings for refresh collision during variable-latency READ operation : latency code 2(3 clocks) , WAIT active LOW , WAIT asserted during delay.

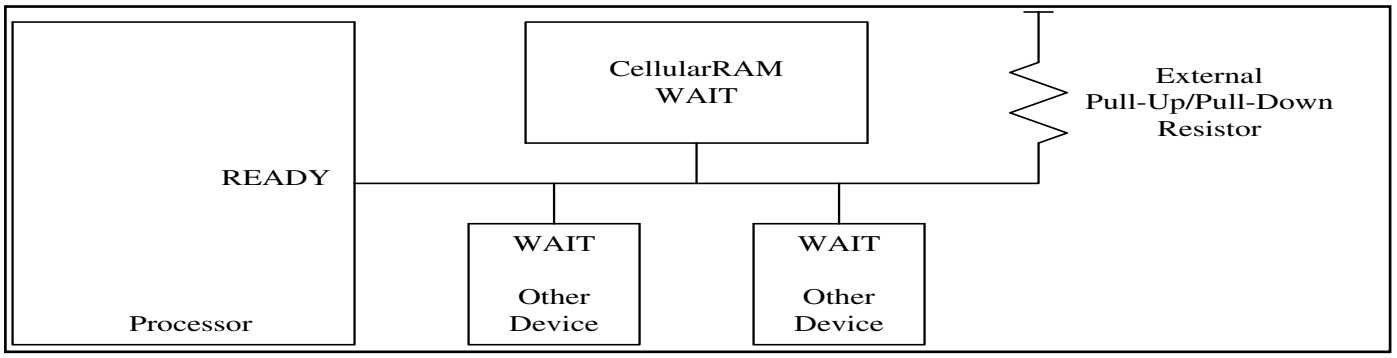
8.2.3 Mixed-Mode Operation

The device supports a combination of synchronous WRITE / READ and asynchronous WRITE / READ operations when the BCR is configured for synchronous operation. The asynchronous WRITE operations require that the clock (CLK) remain static (HIGH or LOW) during the entire sequence. The ADV# signal can be used to latch the target address, or it can remain LOW during the entire WRITE operation. CE# can remain LOW when transitioning between mixed-mode operations with fixed latency enabled; however, the CE# LOW time must not exceed tCEM. Mixed-mode operation facilitates a seamless interface to legacy burst mode Flash memory controllers.

8.2.4 WAIT Operation

The WAIT output on a ADMUX PSRAM device is typically connected to a shared, system level WAIT signal. The shared WAIT signal is used by the processor to coordinate transactions with multiple memories on the synchronous bus.

8.2.4.1 Wired-OR WAIT Configuration



When a burst READ or WRITE operation has been initiated, WAIT goes active to indicate that the ADMUX PSRAM device requires additional time before data can be transferred. For READ operations, WAIT will remain active until valid data is output from the device. For WRITE operations, WAIT will indicate to the memory controller when data will be accepted into the ADMUX PSRAM device. When WAIT transitions to an inactive state, the data burst will progress on successive clock edges.

During a burst cycle, CE# must remain asserted until the first data is valid. Bringing CE# HIGH during this initial latency may cause data corruption.

When using variable initial access latency (BCR[14] = 0), the WAIT output performs an arbitration role for burst READ operations launched while an on-chip refresh is in progress. If a collision occurs, WAIT is asserted for additional clock cycles until the refresh has completed. When the refresh operation has completed, the burst READ operation will continue normally.

WAIT is also asserted when a continuous READ or WRITE burst crosses a row boundary. The WAIT assertion allows time for the new row to be accessed.

WAIT will be asserted after OE# goes LOW during asynchronous READ operations. WAIT will be High-Z during asynchronous WRITE operations. WAIT should be ignored during all asynchronous operations.

By using fixed initial latency (BCR[14] = 1), this ADMUX PSRAM device can be used in burst mode without monitoring the WAIT signal. However, WAIT can still be used to determine when valid data is available at the start of the burst and at the end of the row. If WAIT is not monitored, the controller must stop burst accesses at row boundaries on its own.

8.2.5 LB#/ UB# Operation

The LB# enable and UB# enable signals support byte-wide data WRITEs. During WRITE operations, any disabled bytes will not be transferred to the RAM array and the internal value will remain unchanged. During an asynchronous WRITE cycle, the data to be written is latched on the rising edge of CE#, WE#, LB#, or UB#, whichever occurs first. LB# and UB# must be LOW during READ cycles.

When both the LB# and UB# are disabled (HIGH) during an operation, the device will disable the data bus from receiving or transmitting data. Although the device will seem to be deselected, it remains in an active mode as long as CE# remains LOW.

8.3 Low Power Operation

8.3.1 Standby Mode Operation

During standby, the device current consumption is reduced to the level necessary to perform the DRAM refresh operation. Standby operation occurs when CE# is HIGH. The device will enter a reduced power state upon completion of a READ or WRITE operation, or when the address and control inputs remain static for an extended period of time. This mode will continue until a change occurs to the address or control inputs.

8.3.2 Temperature Compensated Refresh

Temperature-compensated refresh (TCR) allows for adequate refresh at different temperatures. This ADMUX PSRAM device includes an on-chip temperature sensor that automatically adjusts the refresh rate according to the operating temperature. The device continually monitors the temperature to select an appropriate self-refresh rate.

8.3.3 Partial-Array Refresh

Partial-array refresh (PAR) restricts refresh operation to a portion of the total memory array. This feature enables the device to reduce standby current by refreshing only that part of the memory array required by the host system. The refresh options are full array, one-half array, one-quarter array, one-eighth array, or none of the array. The mapping of these partitions can start at either the beginning or the end of the address map . READ and WRITE operations to address ranges receiving refresh will not be affected. Data stored in addresses not receiving refresh will become corrupted. When additional portions of the array need to be re-enabled, the new portions are available immediately after the completion of the WRITE cycle that updates the RCR with the new configuration.

8.3.4 Deep Power-Down Operation

Deep power-down (DPD) operation disables all refresh-related activity. This mode is used if the system does not require the storage provided by the ADMUX PSRAM device. Any stored data will become corrupted when DPD is enabled. When refresh activity has been re-enabled, the ADMUX PSRAM device will require 150µs to perform an initialization procedure before normal operations can resume. During this 150µs period, the current consumption will be higher than the specified standby levels, but considerably lower than the active current specification.

DPD can be enabled by writing to the RCR using CRE or the software access sequence; DPD starts when CE# goes HIGH. DPD is disabled the next time CE# goes LOW and stays LOW for at least 10µs.

8.4 Registers

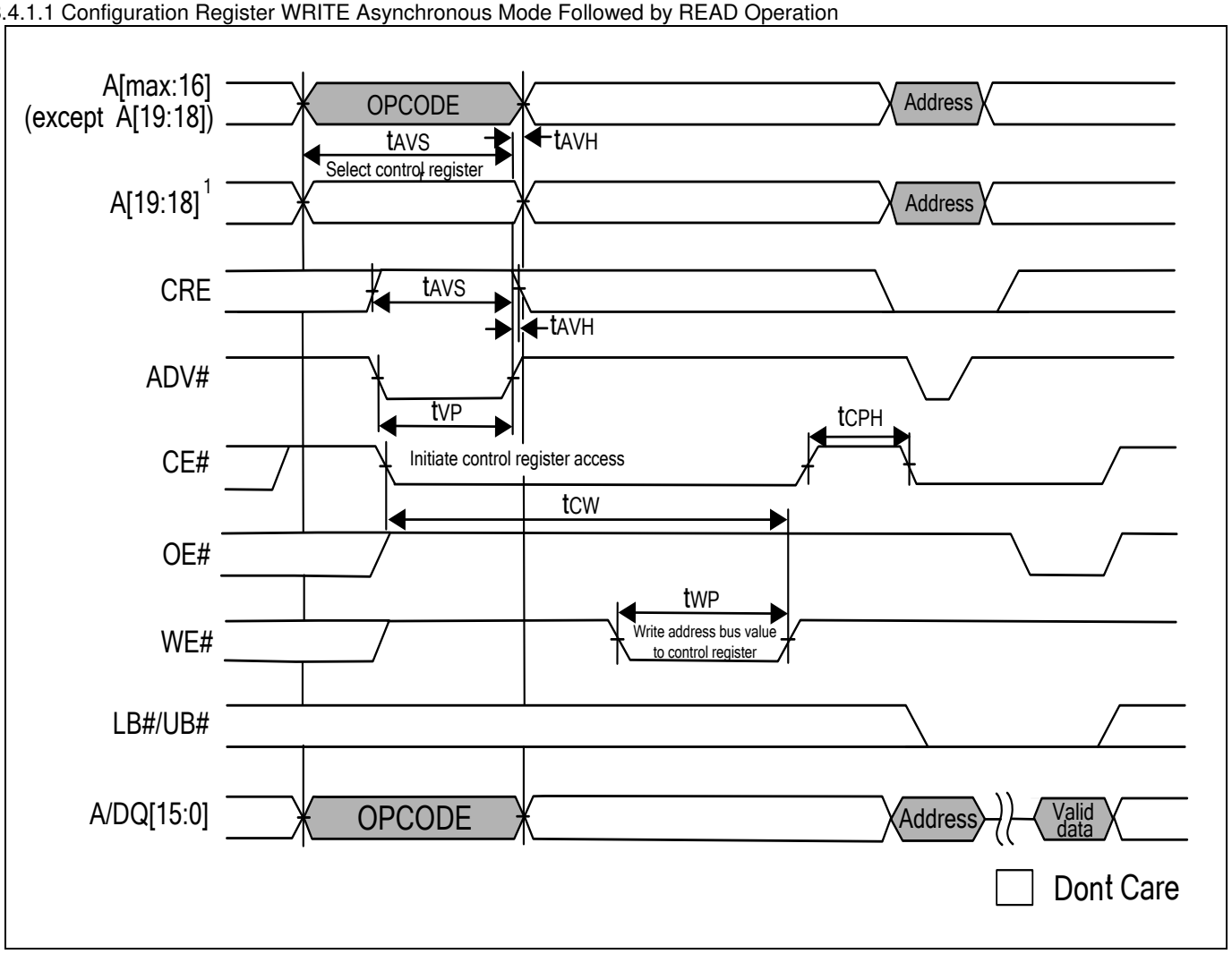
Two user-accessible configuration registers define the device operation. The bus configuration register (BCR) defines how the ADMUX PSRAM interacts with the system memory bus and is nearly identical to its counterpart on burst mode Flash devices. The refresh configuration register (RCR) is used to control how refresh is performed on the DRAM array. These registers are automatically loaded with default settings during power-up, and can be updated any time the devices are operating in a standby state.

A DIDR provides information on the device manufacturer, CellularRAM generation, and the specific device configuration. The DIDR is read-only.

8.4.1 Access Using CRE

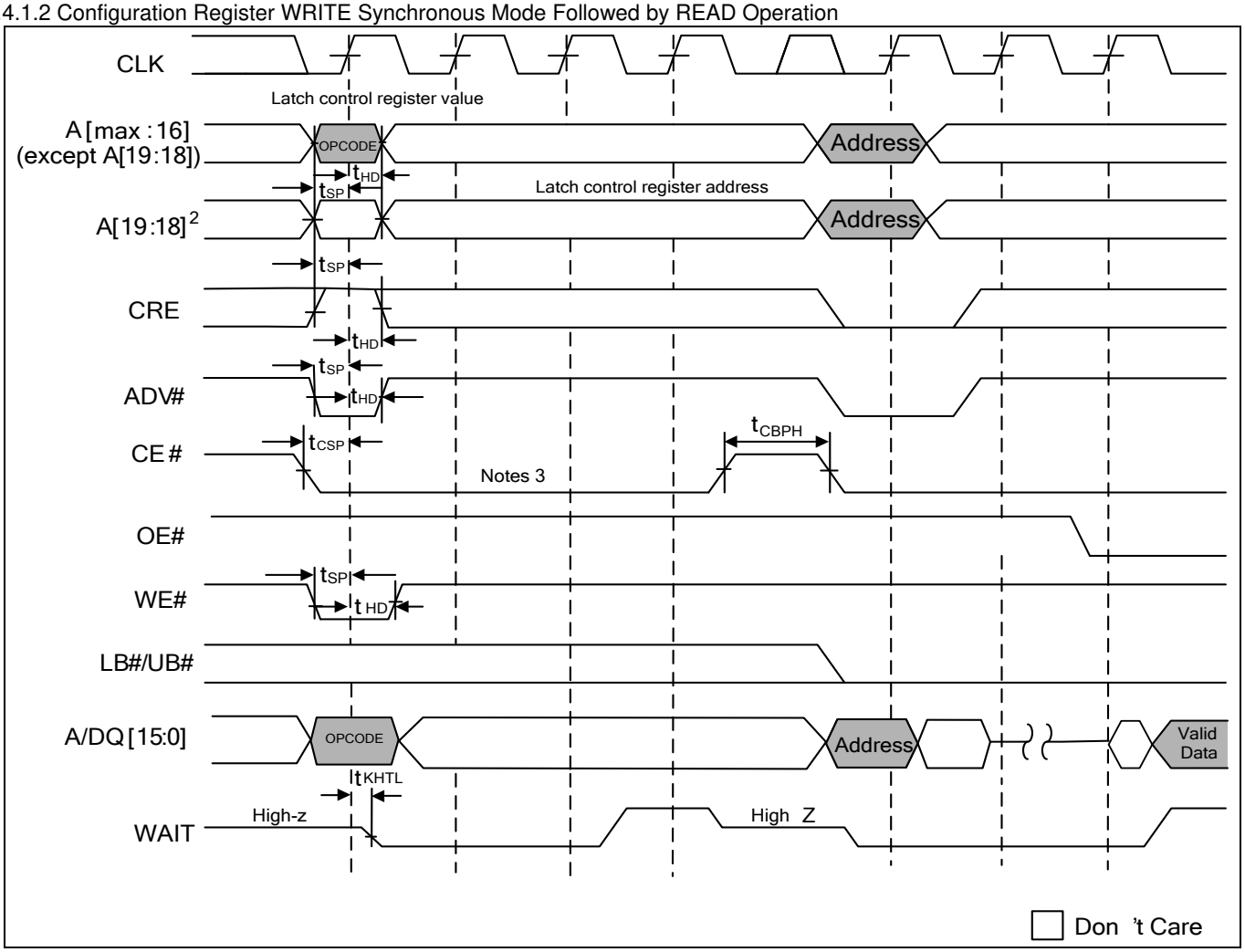
The registers can be accessed using either a synchronous or an asynchronous operation when the control register enable (CRE) input is HIGH. When CRE is LOW, a READ or WRITE operation will access the memory array. The configuration register values are written via addresses A[max:16] and ADQ[15:0]. In an asynchronous WRITE, the values are latched into the configuration register on the rising edge of ADV#, CE#, or WE#, whichever occurs first; LB# and UB# are “Don’t Care.” The BCR is accessed when A[19:18] are 10b; the RCR is accessed when A[19:18] are 00b. The DIDR is read when A[19:18] are 01b. For reads, address inputs other than A[19:18] are “Don’t Care,” and register bits 15:0 are output on DQ[15:0]. Immediately after performing a configuration register READ or WRITE operation, reading the memory array is highly recommended.

8.4.1.1 Configuration Register WRITE Asynchronous Mode Followed by READ Operation



Notes: 1. A[19:18] = 00b to load RCR, and 10b to load BCR.

8.4.1.2 Configuration Register WRITE Synchronous Mode Followed by READ Operation

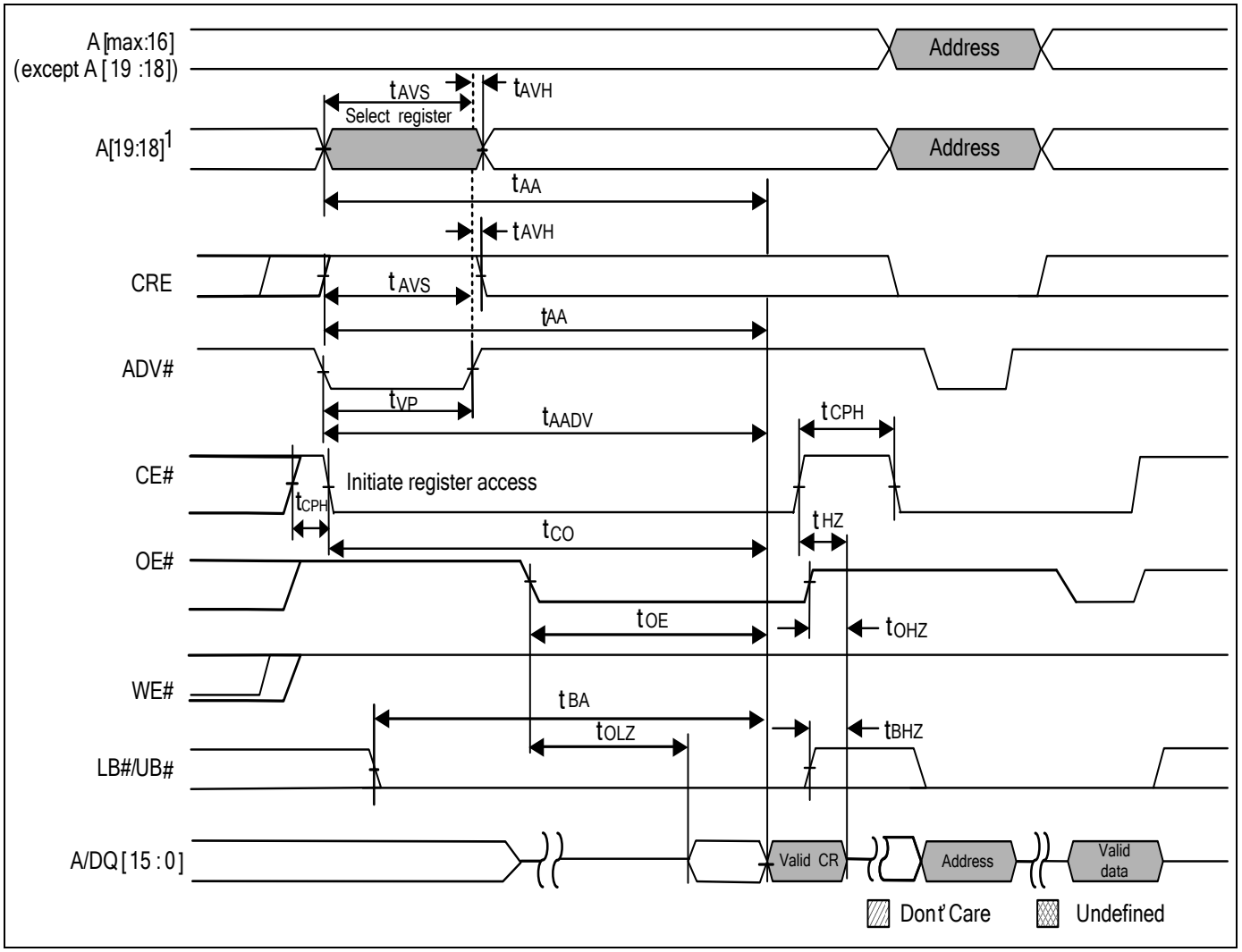


Notes: 1.Non-default BCR settings for synchronous mode configuration register WRITE followed by READ ARRAY operation: latency code 2 (3 clocks), WAIT active LOW, WAIT asserted during delay.

2. A/DQ[19:18] = 00b to load RCR, and 10b to load BCR.

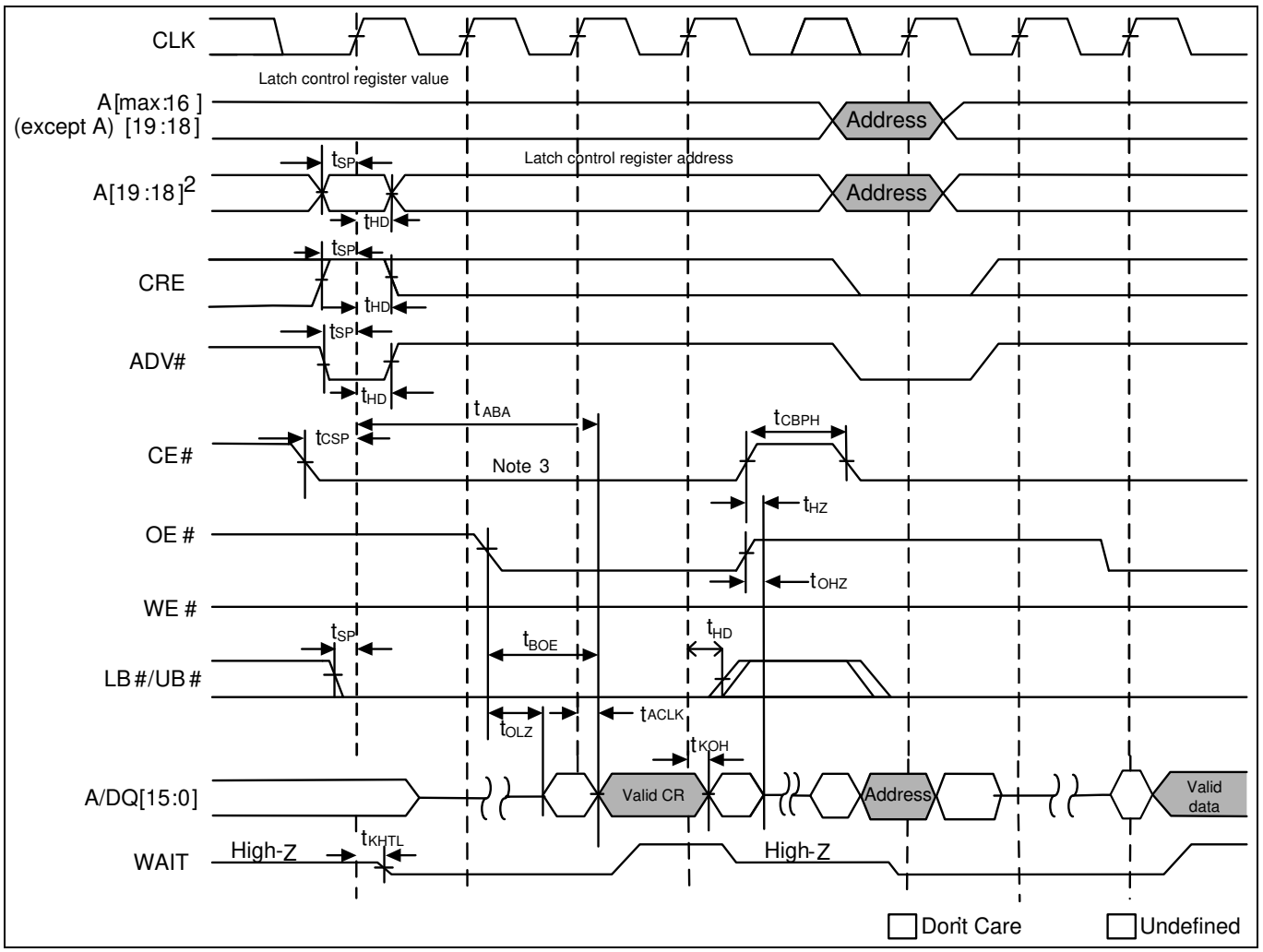
3. CE# must remain LOW to complete a burst-of-one WRITE. WAIT must be monitored—additional WAIT cycles caused by refresh collisions require a corresponding number of additional CE# LOW cycles.

8.4.1.3 Register READ Asynchronous Mode Followed by READ ARRAY Operation



Note : A / DQ [19:18] = 00b to read RCR, 10b to read BCR , and 01b to read DIDR.

8.4.1.4 Register READ Synchronous Mode Followed by READ ARRAY Operation



Notes :1.Non-default BCR settings for synchronous mode register READ followed by READ ARRAY operation : Latency code2(3 clocks) : WAIT active LOW;WAIT asserted during delay.

2.A[19:18]=00b to read RCR,10b to read BCR, and 01b to read DIDR.

3.CE# must remain LOW to complete a burst-of-one READ. WAIT must be monitored—additional WAIT cycles caused by refresh collisions require a corresponding number of additional CE# LOW cycles.

8.4.2 Software Access

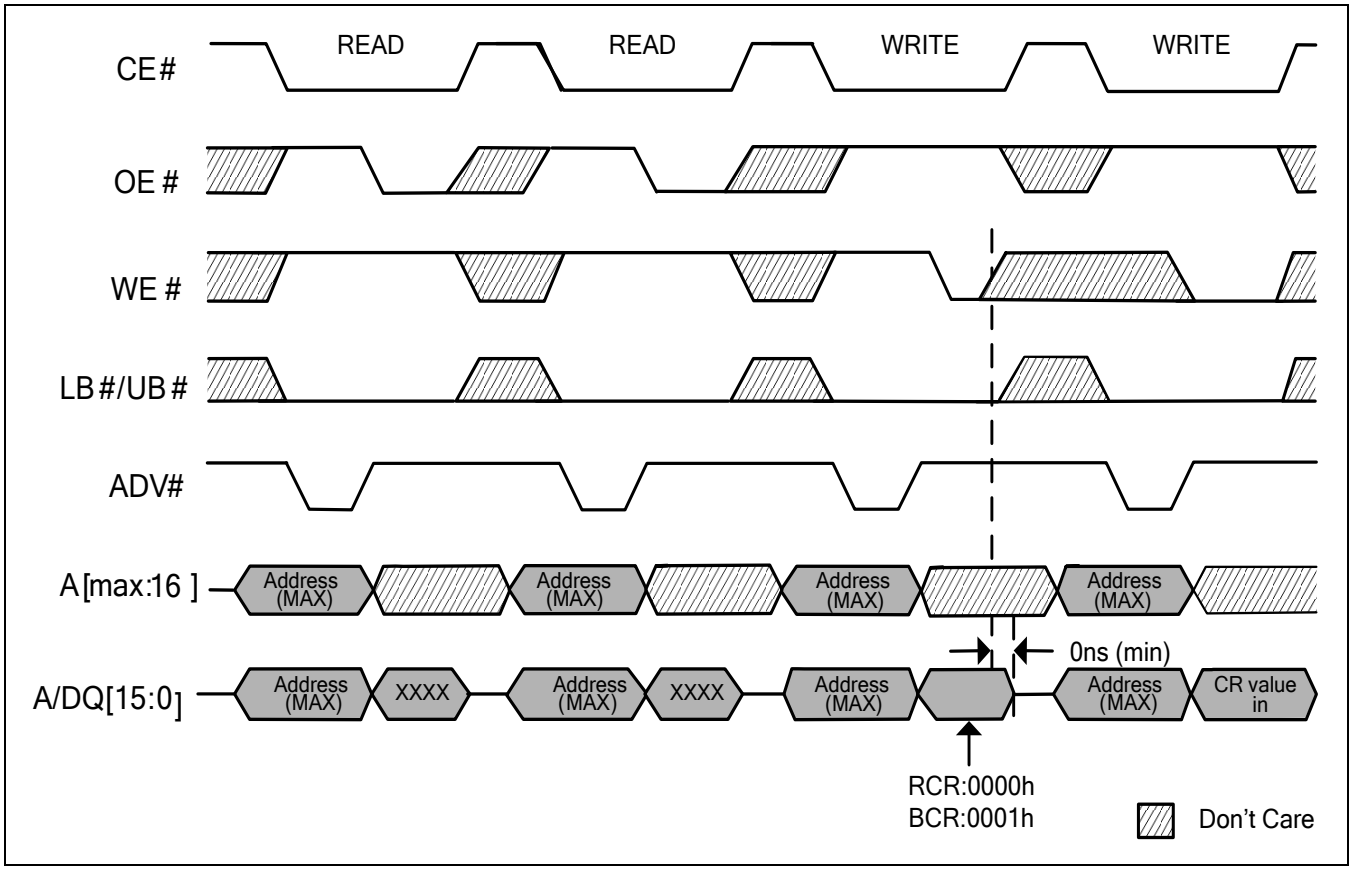
Software access of the registers uses a sequence of asynchronous READ and asynchronous WRITE operations. The contents of the configuration registers can be modified and all registers can be read using the software sequence. The configuration registers are loaded using a four-step sequence consisting of two asynchronous READ operations followed by two asynchronous WRITE operations.

The read sequence is virtually identical except that an asynchronous READ is performed during the fourth operation. The address used during all READ and WRITE operations is the highest address of the ADMUX PSRAM device being accessed; the contents of this address are not changed by using this sequence.

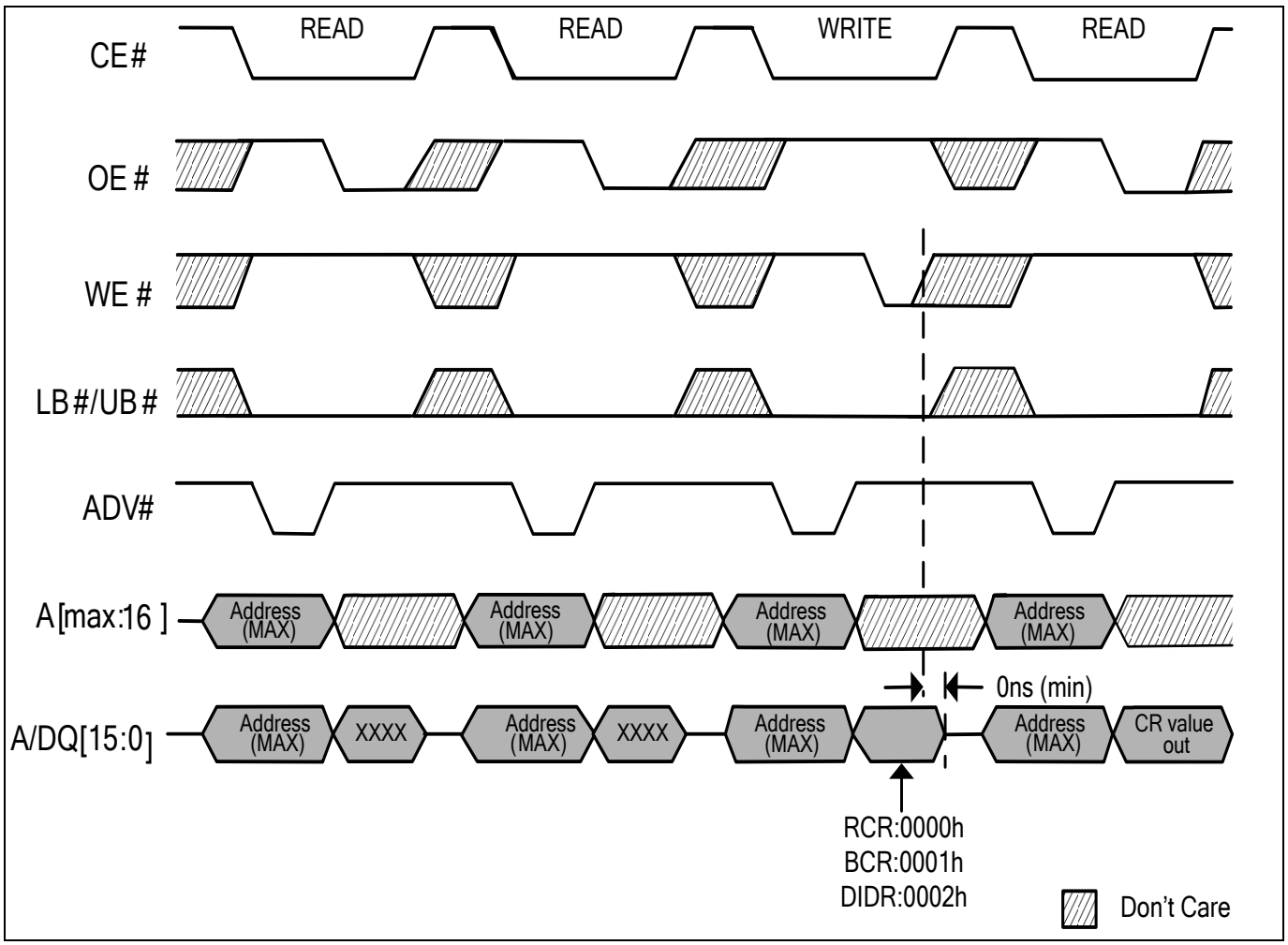
The data value presented during the third operation (WRITE) in the sequence defines whether the BCR, RCR, is to be accessed. If the data is 0000h, the sequence will access the RCR; if the data is 0001h, the sequence will access the BCR. During the fourth operation, ADQ[15:0] transfer data in to or out of bits 15:0 of the registers.

The use of the software sequence does not affect the ability to perform the standard (CRE-controlled) method of loading the configuration registers. However, the software nature of this access mechanism eliminates the need for CRE. If the software mechanism is used, CRE can simply be tied to VSS. The port line often used for CRE control purposes is no longer required.

8.4.2.1 Load Configuration Register



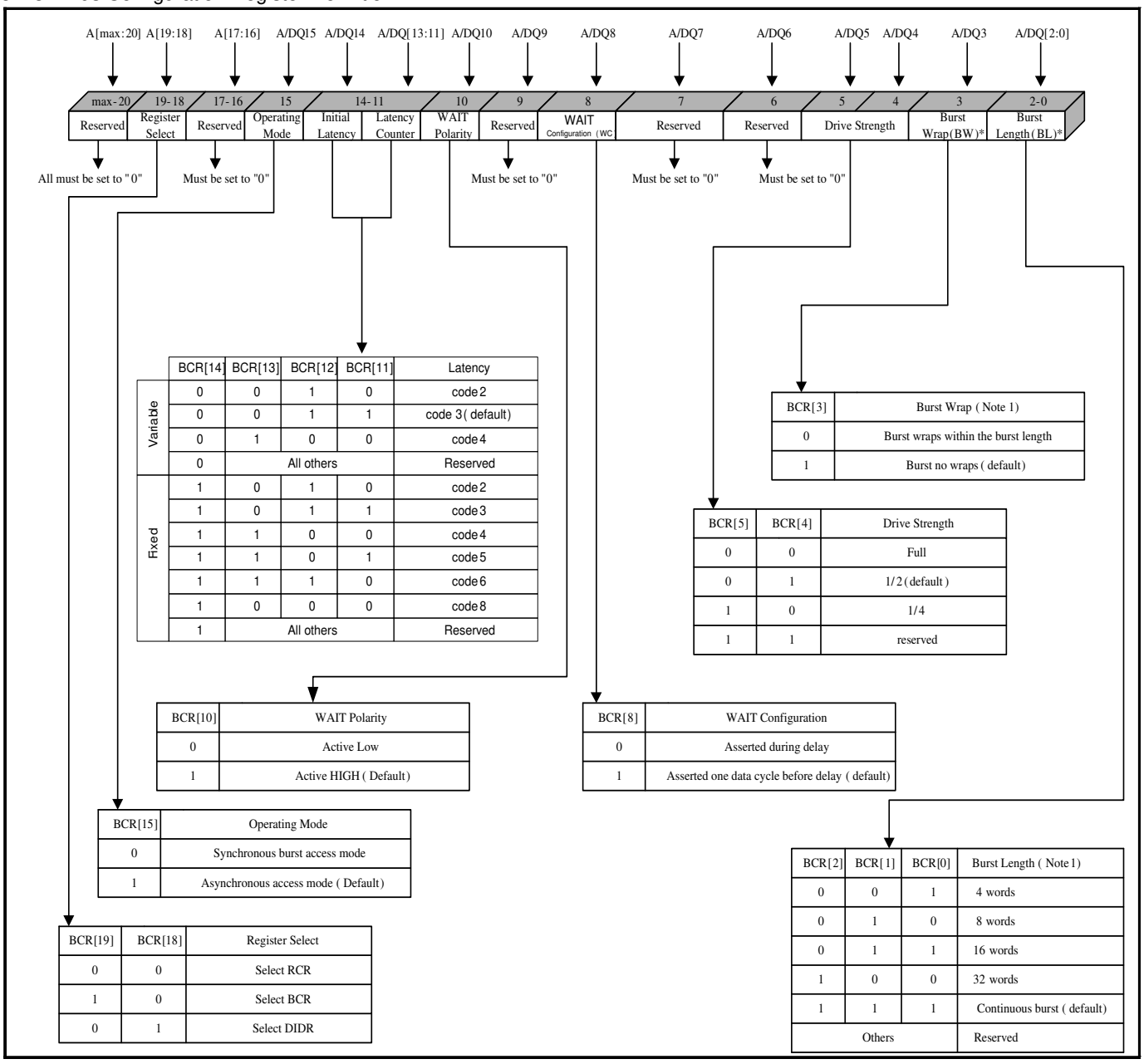
8.4.2.2 Read Configuration Register



8.4.3 Bus Configuration Register

The BCR defines how the ADMUX PSRAM device interacts with the system memory bus. At power-up, the BCR is set to 9D1Fh. The BCR is accessed with CRE HIGH and A[19:18] = 10b, or through the register access software sequence with A/DQ = 0001h on the third cycle.

8.4.3.1 Bus Configuration Register Definition



	BCR[14]	BCR[13]	BCR[12]	BCR[11]	Latency
Variable	0	0	1	0	code 2
	0	0	1	1	code 3 (default)
	0	1	0	0	code 4
	0	All others			Reserved
Fixed	1	0	1	0	code 2
	1	0	1	1	code 3
	1	1	0	0	code 4
	1	1	0	1	code 5
	1	1	1	0	code 6
	1	0	0	0	code 8
	1	All others			Reserved

BCR[3]	Burst Wrap (Note 1)
0	Burst wraps within the burst length
1	Burst no wraps (default)

BCR[5]	BCR[4]	Drive Strength
0	0	Full
0	1	1/2 (default)
1	0	1/4
1	1	reserved

BCR[10]	WAIT Polarity
0	Active Low
1	Active HIGH (Default)

BCR[8]	WAIT Configuration
0	Asserted during delay
1	Asserted one data cycle before delay (default)

BCR[15]	Operating Mode
0	Synchronous burst access mode
1	Asynchronous access mode (Default)

BCR[19]	BCR[18]	Register Select
0	0	Select RCR
1	0	Select BCR
0	1	Select DIDR

BCR[2]	BCR[1]	BCR[0]	Burst Length (Note 1)
0	0	1	4 words
0	1	0	8 words
0	1	1	16 words
1	0	0	32 words
1	1	1	Continuous burst (default)
Others			Reserved

Notes: 1. Burst wrap and length apply to both READ and WRITE operations.
2.Reserved bits must be set to zero. Reserved bits not set to zero will affect device functionality. BCR[15:0] will be read back as written.

8.4.3.2 Burst Length (BCR[2:0]) Default = Continuous Burst

Burst lengths define the number of words the device outputs during burst READ and WRITE operations. The device supports a burst length of 4, 8, 16, or 32 words. The device can also be set in continuous burst mode where data is output sequentially without regard to address boundaries; the internal address wraps to 000000h if the device is read past the last address.

8.4.3.3 Burst Wrap (BCR[3]) Default = No Wrap

The burst-wrap option determines if a 4-, 8-, 16-, or 32-word READ or WRITE burst wraps within the burst length, or steps through sequential addresses. If the wrap option is not enabled, the device accesses data from sequential addresses without regard to address boundaries; the internal address wraps to 000000h if the device is read past the last address.

8.4.3.4 Sequence and Burst Length

Burst Wrap		Start Addr	4-Word Burst Length	8-Word Burst Length	16-Word Burst Length	32-Word Burst Length	Continuous Burst
BCR[3]	Wrap	Deci-mal	Linear	Linear	Linear	Linear	Linear
0	Yes	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0-1-2-...-29-30-31	0-1-2-3-4-5-6-…
		1	1-2-3-0	1-2-3-4-5-6-7-0	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-0	1-2-3-...-30-31-0	1-2-3-4-5-6-7-…
		2	2-3-0-1	2-3-4-5-6-7-0-1	2-3-4-5-6-7-8-9-10-11-12-13-14-15-0-1	2-3-4-...-31-0-1	2-3-4-5-6-7-8-…
		3	3-0-1-2	3-4-5-6-7-0-1-2	3-4-5-6-7-8-9-10-11-12-13-14-15-0-1-2	3-4-5-...-0-1-2	3-4-5-6-7-8-9-…
		4		4-5-6-7-0-1-2-3	4-5-6-7-8-9-10-11-12-13-14-15-0-1-2-3	4-5-6-...-1-2-3	4-5-6-7-8-9-10-…
		5		5-6-7-0-1-2-3-4	5-6-7-8-9-10-11-12-13-14-15-0-1-2-3-4	5-6-7-...-2-3-4	5-6-7-8-9-10-11-…
		6		6-7-0-1-2-3-4-5	6-7-8-9-10-11-12-13-14-15-0-1-2-3-4-5	6-7-8-...-3-4-5	6-7-8-9-10-11-12-
		7		7-0-1-2-3-4-5-6	7-8-9-10-11-12-13-14-15-0-1-2-3-4-5-6	7-8-9-...-4-5-6	7-8-9-10-11-12-13-…
		...			...	...	...
		14			14-15-0-1-2-3-4-5-6-7-8-9-10-11-12-13	14-15-16-...-11-12-13	14-15-16-17-18-19-20-...
		15			15-0-1-2-3-4-5-6-7-8-9-10-11-12-13-14	15-16-17-...-12-13-14	15-16-17-18-19-20-21-...
		...				...	...
		30				30-31-0-...-27-28-29	30-31-32-33-34-...
		31				31-0-1-...-28-29-30	31-32-33-34-35-...
1	No	0	0-1-2-3	0-1-2-3-4-5-6-7	0-1-2-3-4-5-6-7-8-9-10-11-12-13-14-15	0-1-2...--29-30-31	0-1-2-3-4-5-6-…
		1	1-2-3-4	1-2-3-4-5-6-7-8	1-2-3-4-5-6-7-8-9-10-11-12-13-14-15-16	1-2-3-...-30-31-32	1-2-3-4-5-6-7-…
		2	2-3-4-5	2-3-4-5-6-7-8-9	2-3-4-5-6-7-8-9-10-11-12-13-14-15-16-17	2-3-4-...-31-32-33	2-3-4-5-6-7-8-…
		3	3-4-5-6	3-4-5-6-7-8-9-10	3-4-5-6-7-8-9-10-11-12-13-14-15-16-17-18	3-4-5-...-32-33-34	3-4-5-6-7-8-9-…
		4		4-5-6-7-8-9-10-11	4-5-6-7-8-9-10-11-12-13-14-15-16-17-18-19	4-5-6-...-33-34-35	4-5-6-7-8-9-10-…
		5		5-6-7-8-9-10-11-12	5-6-7-8-9-10-11-12-13-...-15-16-17-18-19-20	5-6-7-...-34-35-36	5-6-7-8-9-10-11…
		6		6-7-8-9-10-11-12-13	6-7-8-9-10-11-12-13-14-...-16-17-18-19-20-21	6-7-8-...-35-36-37	6-7-8-9-10-11-12…
		7		7-8-9-10-11-12-13-14	7-8-9-10-11-12-13-14-...-17-18-19-20-21-22	7-8-9-...-36-37-38	7-8-9-10-11-12-13…
		...			...	...	...
		14			14-15-16-17-18-19-...-23-24-25-26-27-28-29	14-15-16-...-43-44-45	14-15-16-17-18-19-20-…
		15			15-16-17-18-19-20-...-24-25-26-27-28-29-30	15-16-17-...-44-45-46	15-16-17-18-19-20-21-…
		...				...	...
		30				30-31-32-...-59-60-61	30-31-32-33-34-35-36-...
		31				31-32-33-...-60-61-62	31-32-33-34-35-36-37-...