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S6E2H Series

32-bit ARM® Cortex®-M4F FM4 Microcontroller

Devices in the S6E2H Series are highly integrated 32-bit microcontrollers with high performance and competitive cost. This series is based on the ARM Cortex-M4F Processor with on-chip Flash memory and SRAM. The series has peripheral functions such as Motor Control Timers, ADCs and Communication Interfaces (CAN, UART, CSIO, I²C, LIN). The products that are described in this data sheet are placed into TYPE6-M4 product categories in the "FM4 Family Peripheral Manual Main Part (002-04856)".

Features

- 32-bit ARM Cortex-M4F Core
  - Up to 160 MHz Frequency Operation
- On-chip Memories
  - MainFlash memory - Up to 512 Kbytes
  - WorkFlash memory - 32 Kbytes
  - SRAM
    - SRAM0: Up to 32 Kbytes
    - SRAM1: Up to 16 Kbytes
    - SRAM2: Up to 16 Kbytes
- External Bus Interface
- CAN Interface (Max 2 channels)
- Multi-function Serial Interface (Max 8 channels)
  - Universal Asynchronous Receiver/Transmitter (UART)
  - Clock Synchronous Serial Interface (CSIO (SPI))
  - Local Interconnect Network (LIN)
  - Inter-integrated Circuit (I²C)
- DMA Controller (8 channels)
- DSTC (Descriptor System data Transfer Controller) (256 channels)
- A/D Converter (Max 24 channels) [12-bit A/D Converter]
- DA Converter (Max 2 channels)
- Base Timer (Max 8 channels)
- Up to 100 high-speed general-purpose I/O ports @ 120 pin Package
- Multi-function Timer (Max 3 units)
- Real-time Clock (RTC)
- Quadrature Position/Revolution Counter (QPRC) (Max 3 channels)
- Dual Timer (32-/16-bit Down Counter)
- Watch Counter
- External Interrupt Controller Unit
- Watchdog Timer (2 channels)
- CRC (Cyclic Redundancy Check) Accelerator
- SD Card Interface
- Five clock sources (2 external oscillators, 2 internal CR oscillator, and Main PLL) that are dynamically selectable.
  - Main clock: 4 MHz to 48 MHz
  - Sub Clock: 32.768 kHz
  - High-speed internal CR Clock: 4 MHz
  - Low-speed internal CR Clock: 100 kHz
  - Main PLL Clock
- Resets
  - Reset requests from INITX pin
  - Power on reset
  - Software reset
  - Watchdog timers reset
  - Low voltage detector reset
  - Clock supervisor reset
- Clock SuperVisor (CSV)
- Low-Voltage Detector (LVD)
- Low-power Consumption Modes
  - Sleep
  - Timer
  - RTC
  - Stop
  - Deep standby RTC (selectable from with/without RAM retention)
  - Deep standby stop (selectable from with/without RAM retention)
- VBAT
- Debug
  - Serial Wire JTAG Debug Port (SWJ-DP)
  - Embedded Trace Macrocells (ETM) provide comprehensive debug and trace facilities.
- Unique value of the device (41-bit) is set.
- Power Supplies
  - Wide range voltage: VCC = 2.7 V to 5.5 V
  - Power supply for VBAT: VBAT = 2.7 V to 5.5 V

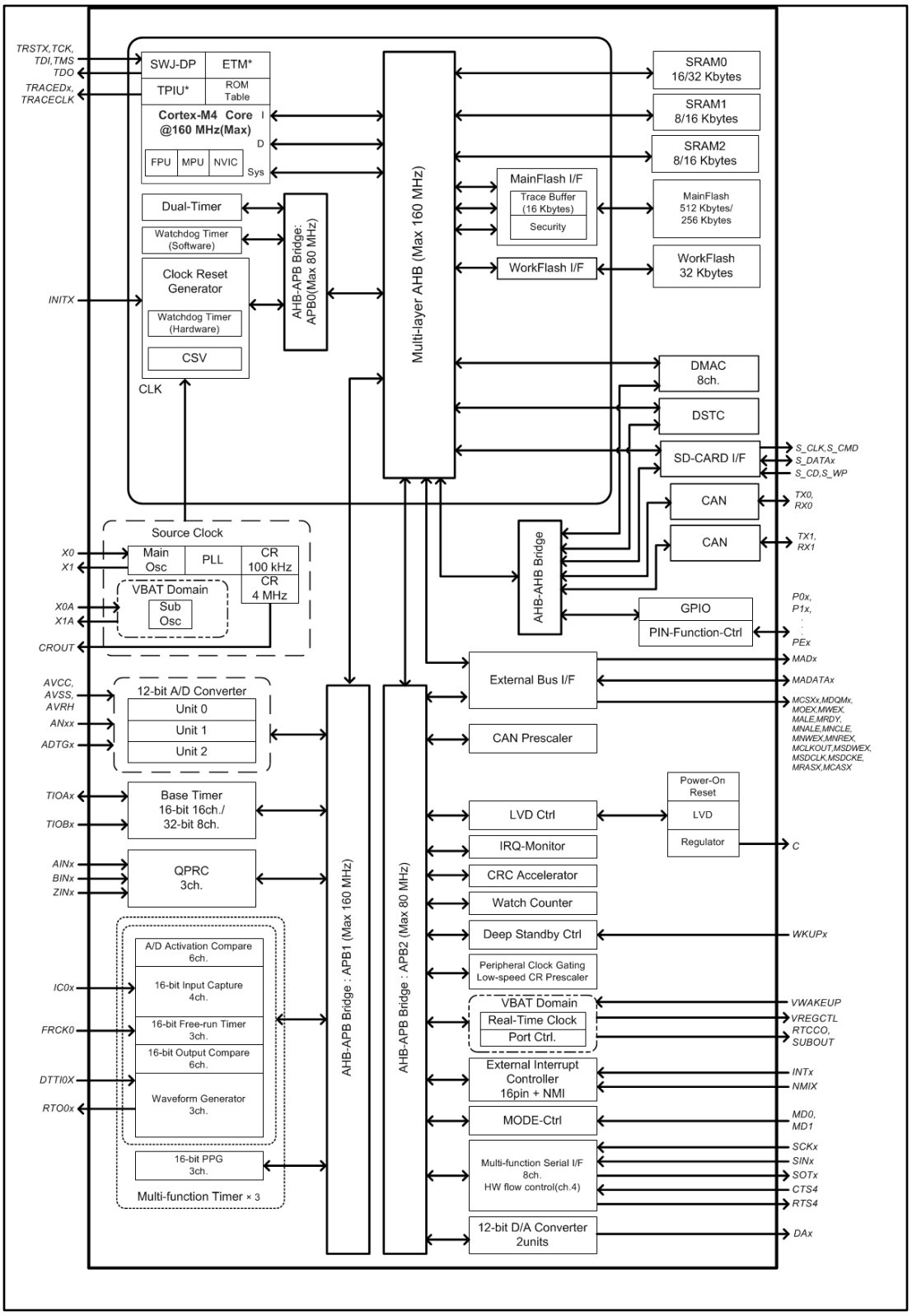
Ecosystem for Cypress FM4 MCUs

Cypress provides a wealth of data at www.cypress.com to help you to select the right MCU for your design, and to help you to quickly and effectively integrate the device into your design. Following is an abbreviated list for FM4 MCUs:

- Overview: Product Portfolio, Product Roadmap
- Product Selectors: FM4 MCUs
- Application notes: Cypress offers a large number of FM4 application notes covering a broad range of topics, from basic to advanced level. Recommended application notes for getting started with FM4 family of MCUs are:
  - AN204468 - FM4 I2S USB MP3 Player Application 32-Bit Microcontroller FM4 Family: This application note describes the general structure of the I²S USB MP3Player software example, its single modules in detail and how it is used.
  - AN204471 - FM4 S6E2CC Series External Memory Programmer: This document describes use of the MCU Universal Programmer as an off-line programmer for Quad SPI flash memory programming on the S6E2CC Series SK.
  - AN203277 - FM 32-Bit Microcontroller Family Hardware Design Considerations: This application note reviews several topics for designing a hardware system around FM0+, FM3, and FM4 family MCUs. Subjects include power system, reset, crystal, and other pin connections, and programming and debugging interfaces.
  - AN202488 - FM4 MB9BF56x and S6E2HG Series MCU - Servo Motor Speed Control: This document covers servo motor speed control solution on FM4 MCU - MB9BF56x and S6E2H.
  - AN99235 - FM4 S6E2HG Series MCU - 16-Bit PWM Using a Base Timer: Cypress FM4 Family of 32-bit ARM® Cortex®-M4 Microcontrollers FM4 S6E2H Series Motor Control ARM® Cortex®-M4 MCU
  - AN202487 - Differences Among FM0+, FM3, and FM4 32-Bit Microcontrollers: Highlights the peripheral differences in Cypress's FM family MCUs. It provides dedicated sections for each peripheral and contains lists, tables, and descriptions of peripheral feature and register differences.
  - AN204438 - How to Setup Flash Security for FM0+, FM3 and FM4 Families: This application note describes how to setup the Flash Security for FM0+, FM**3**, and FM4 devices
- Development kits:
  - FM4-U120-9B560 - ARM® Cortex®-M4 MCU Starter Kit with USB and CMSIS-DAP
  - FM4-216-ETHERNET ARM® Cortex®-M4 MCU Development Kit with Ethernet, CAN and USB Host
  - FM4-176L-S6E2CC-ETH - ARM® Cortex®-M4 MCU Starter Kit with Ethernet and USB Host
  - FM4-176L-S6E2GM - ARM® Cortex®-M4 MCU Pioneer Kit with Ethernet and USB Host
- Peripheral Manuals

Contents

1. S6E2H Series Block Diagram



2. Product Lineup

Memory Size

Product name		S6E2HG4 S6E2HE4 S6E2H44 S6E2H14	S6E2HG6 S6E2HE6 S6E2H46 S6E2H16
MainFlash memory		256 Kbytes	512 Kbytes
WorkFlash memory		32 Kbytes	32 Kbytes
On-chip SRAM		32 Kbytes	64 Kbytes
	SRAM0	16 Kbytes	32 Kbytes
	SRAM1	8 Kbytes	16 Kbytes
	SRAM2	8 Kbytes	16 Kbytes

Function Availability by Part

Description			Product Name			
			S6E2HG6 S6E2HG4	S6E2HE6 S6E2HE4	S6E2H46 S6E2H44	S6E2H16 S6E2H14
CPU			Cortex-M4F, MPU, NVIC 128ch.			
	Freq.		160 MHz			
Power supply voltage range			2.7 V to 5.5 V			
CAN			2ch. (Max)	N/A	2ch. (Max)	N/A
DMAC			8ch.			
DSTC			256ch.			
Multi-function Serial Interface (UART/CSIO/LIN/I²C)			8ch. (Max)			
Base Timer (PWC/Reload timer/PWM/PPG)			8ch. (Max)			
MF Timer	A/D activation compare	6ch.	3 units (Max)			
	Input capture	4ch.				
	Free-run timer	3ch.				
	Output compare	6ch.				
	Waveform generator	3ch.				
	PPG	3ch.				
SD Card Interface			1 unit		N/A	
QPRC			3ch. (Max)			
Dual Timer			1 unit			
Real-Time Clock			1 unit			
Watch Counter			1 unit			

Description		Product Name			
		S6E2HG6 S6E2HG4	S6E2HE6 S6E2HE4	S6E2H46 S6E2H44	S6E2H16 S6E2H14
CRC Accelerator		Yes			
Watchdog Timer		1ch. (SW) + 1ch. (HW)			
External Interrupts		16 pins (Max) + NMI × 1			
12-bit D/A Converter		2 units (Max)			
CSV (Clock Super Visor)		Yes			
LVD (Low-Voltage Detector)		2ch.			
Built-in CR	High-speed	4 MHz (±2%)			
	Low-speed	100 kHz (Typ)			
Debug Function		SWJ-DP/ETM			
Unique ID		Yes			

Notes:

- *Because of package pin limitations, not all functions within the device can be brought out to external pins. You must carefully work out the pin allocation needed for your design.*
  You must use the port relocate function of the I/O port according to your function use.
- *See 13.4.3 Built-in CR Oscillation Characteristics for the accuracy of the built-in CR.*

3. Package-Dependent Features

The S6E2H Series of parts is available in 80-pin, 100-pin, and 120-/121-pin packages.

Description	S6E2H		
	Package Suffix		
	E0A	F0A	G0A
Pins count	80	100	120/121
12-bit A/D Converter	16ch. (3 units)	24ch. (3 units)	
I/O Ports	63 pins (Max)	80 pins (Max)	100 pins (Max)
External Bus Interface	Addr:19-bit (Max), R/W data: 8-bit (Max), CS:5 (Max), SRAM, NOR Flash	Addr:25-bit (Max), R/W data: 8-/16-bit (Max), CS:9 (Max), SRAM, NOR Flash, SDRAM	Addr:25-bit (Max), R/W data: 8-/16-bit (Max), CS:9 (Max), SRAM, NOR Flash, NAND Flash, SDRAM

Notes:

- *For an explicit list of part numbers and the feature differences among them, see 14 Ordering Information.*
- *See 15 Package Dimensions for detailed information on each package.*

4. Detailed Product Features

32-bit ARM Cortex-M4F Core

- Up to 160 MHz Frequency Operation
- FPU built-in
- Support DSP instruction
- Memory Protection Unit (MPU): improves the reliability of an embedded system
- Integrated Nested Vectored Interrupt Controller (NVIC): 1 NMI (non-maskable interrupt) and 128 peripheral interrupts and 16 priority levels
- 24-bit System timer (Sys Tick): System timer for OS task management

On-chip Memories

- Flash memory

These series are based on two independent on-chip Flash memories.

  - MainFlash memory
    - Up to 512 Kbytes
    - Built-in Flash Accelerator System with 16 Kbytes trace buffer memory
    - The read access to Flash memory can be achieved without wait-cycle up to operation frequency of 72 MHz. Even at the operation frequency more than 72 MHz, an equivalent access to Flash memory can be obtained by Flash Accelerator System.
    - Security function for code protection
  - WorkFlash memory
    - 32 Kbytes
    - Read cycle:
    - 6 wait-cycle: the operation frequency more than 120 MHz, and up to 160 MHz
    - 4 wait-cycle: the operation frequency more than 72 MHz, and up to 120 MHz
    - 2 wait-cycle: the operation frequency more than 40 MHz, and up to 72 MHz
    - 0 wait-cycle: the operation frequency up to 40 MHz
    - Security function is shared with code protection

- SRAM

This is composed of three independent SRAMs (SRAM0, SRAM1 and SRAM2). SRAM0 is connected to I-code bus or D-code bus of Cortex-M4F core. SRAM1 and SRAM2 are connected to System bus of Cortex-M4F core.

  - SRAM0: Up to 32 Kbytes
  - SRAM1: Up to 16 Kbytes
  - SRAM2: Up to 16 Kbytes

External Bus Interface

- Supports SRAM, NOR, NAND Flash and SDRAM device
- Up to 9 chip selects CS0 to CS8 (CS8 is only for SDRAM)
- 8-/16-bit Data width
- Up to 25-bit Address bit
- Supports Address/Data multiplex
- Supports external RDY function
- Supports scramble function
  - Possible to set the validity/invalidity of the scramble function for the external areas 0x6000_0000 to 0xDFFF_FFFF in 4 Mbytes units.
  - Possible to set two kinds of the scramble key
  - **Note**: It is necessary to prepare the dedicated software library to use the scramble function.

CAN Interface (Max 2 channels)

- Compatible with CAN Specification 2.0A/B
- Maximum transfer rate: 1 Mbps
- Built-in 32 message buffer

Multi-function Serial Interface (Max 8 channels)

- 64 bytes with FIFO (the FIFO step numbers are variable depending on the settings of the communication mode or bit length.)
- Operation mode is selectable from the followings for each channel.
  - UART
  - CSIO
  - LIN
  - I^2C
- UART
  - Full-duplex double buffer
  - Selection with or without parity supported
  - Built-in dedicated baud rate generator
  - External clock available as a serial clock
  - Hardware Flow control : Automatically control the transmission by CTS/RTS (only ch.4)
  - Various error detect functions available (parity errors, framing errors, and overrun errors)
- CSIO
  - Full-duplex double buffer
  - Built-in dedicated baud rate generator
  - Overrun error detect function available
  - Serial chip select function (ch.6 and ch.7 only)
  - Supports high-speed SPI (ch.4 and ch.6 only)
  - Data length 5 to 16-bit
- LIN
  - LIN protocol Rev.2.1 supported
  - Full-duplex double buffer
  - Master/Slave mode supported
  - LIN break field generation (can change to 13 to 16-bit length)
  - LIN break delimiter generation (can change to 1 to 4-bit length)
  - Various error detect functions available (parity errors, framing errors, and overrun errors)

- I²C
  - Standard mode (Max 100 kbps) / High-speed mode (Max 400 kbps) supported
  - Fast mode Plus (Fm+) (Max 1000 kbps, only for ch.3=ch.A and ch.7=ch.B) supported

DMA Controller (8 channels)

DMA Controller has an independent bus for CPU, so CPU and DMA Controller can process simultaneously.

- 8 independently configured and operated channels
- Transfer can be started by software or request from the built-in peripherals
- Transfer address area: 32-bit (4 Gbytes)
- Transfer mode: Block transfer/Burst transfer/Demand transfer
- Transfer data type: bytes/half-word/word
- Transfer block count: 1 to 16
- Number of transfers: 1 to 65536

DSTC (Descriptor System data Transfer Controller) (256 channels)

The DSTC can transfer data at high-speed without going via the CPU. The DSTC adopts the Descriptor system and, following the specified contents of the Descriptor which has already been constructed on the memory, can access directly the memory /peripheral device and performs the data transfer operation.

It supports the software activation, the hardware activation and the chain activation functions.

A/D Converter (Max 24 channels) [12-bit A/D Converter]

- Successive Approximation type
- Built-in 3 units
- Conversion time: 0.5 µs @ 5 V
- Priority conversion available (priority at 2 levels)
- Scanning conversion mode
- Built-in FIFO for conversion data storage (for SCAN conversion: 16 steps, for Priority conversion: 4 steps)

DA Converter (Max 2 channels)

- R-2R type
- 12-bit resolution

Base Timer (Max 8 channels)

Operation mode is selectable from the followings for each channel.

- 16-bit PWM timer
- 16-bit PPG timer
- 16-/32-bit reload timer
- 16-/32-bit PWC timer
- Event counter mode (external clock mode)

General Purpose I/O Port

This series can use its pins as general purpose I/O ports when they are not used for external bus or peripherals. Moreover, the port relocate function is built in. It can set which I/O port the peripheral function can be allocated.

- Capable of pull-up control per pin
- Capable of reading pin level directly
- Built-in the port relocate function
- Up to 100 high-speed general-purpose I/O ports @ 120 pin Package
- Some pin is 5 V tolerant I/O.

See 6. Pin Description and 7. I/O Circuit Type for the corresponding pins.

Multi-function Timer (Max 3 units)

The Multi-function timer is composed of the following blocks.

Minimum resolution : 6.25 ns

- 16-bit free-run timer × 3 ch./unit
- Input capture × 4 ch./unit
- Output compare × 6 ch./unit
- A/D activation compare × 6 ch./unit
- Waveform generator × 3 ch./unit
- 16-bit PPG timer × 3 ch./unit

The following function can be used to achieve the motor control.

- PWM signal output function
- DC chopper waveform output function
- Dead time function
- Input capture function
- A/D convertor activate function
- DTIF (Motor emergency stop) interrupt function

Real-time Clock (RTC)

The Real-time clock can count Year/Month/Day/Hour/Minute/Second/A day of the week from 00 to 99.

- Interrupt function with specifying date and time (Year/Month/Day/Hour/Minute.) is available. This function is also available by specifying only Year, Month, Day, Hour or Minute.
- Timer interrupt function after set time or each set time.
- Capable of rewriting the time with continuing the time count.
- Leap year automatic count is available.

Quadrature Position/Revolution Counter (QPRC) (Max 3 channels)

The Quadrature Position/Revolution Counter (QPRC) is used to measure the position of the position encoder. Moreover, it is possible to use up/down counter.

- The detection edge of the three external event input pins AIN, BIN and ZIN is configurable.
- 16-bit position counter
- 16-bit revolution counter
- Two 16-bit compare registers

Dual Timer (32-/16-bit Down Counter)

The Dual Timer consists of two programmable 32-/16-bit down counters.
Operation mode is selectable from the followings for each channel.

- Free-running
- Periodic (=Reload)
- One-shot

Watch Counter

The Watch counter is used for wake up from the low-power consumption mode. It is possible to select the main clock, sub clock, built-in high-speed CR clock or built-in low-speed CR clock as the clock source.

Interval timer: up to 64 s (Max) @ Sub Clock : 32.768 kHz

External Interrupt Controller Unit

- External interrupt input pin: Max 16 pins
  - Both edges(Rise edge and Fall edge) detect
- Include one non-maskable interrupt (NMI)

Watchdog Timer (2 channels)

A watchdog timer can generate interrupts or a reset when a time-out value is reached.

This series consists of two different watchdogs, a Hardware watchdog and a Software watchdog.

Hardware watchdog timer is clocked by low-speed internal CR oscillator. Therefore, Hardware watchdog is active in any power saving mode except Stop.

CRC (Cyclic Redundancy Check) Accelerator

The CRC accelerator helps a verify data transmission or storage integrity.

CCITT CRC16 and IEEE-802.3 CRC32 are supported.

- CCITT CRC16 Generator Polynomial: 0x1021
- IEEE-802.3 CRC32 Generator Polynomial: 0x04C11DB7

SD Card Interface

It is possible to use the SD card that conforms to the following standards.

- Part 1 Physical Layer Specification version 3.01
- Part E1 SDIO Specification version 3.00
- Part A2 SD Host Controller Standard Specification version 3.00
- 1-bit or 4-bit data bus

Clock and Reset

[Clocks]

Five clock sources (2 external oscillators, 2 internal CR oscillator, and Main PLL) that are dynamically selectable.

- Main clock: 4 MHz to 48 MHz
- Sub Clock: 32.768 kHz
- High-speed internal CR Clock: 4 MHz
- Low-speed internal CR Clock: 100 kHz
- Main PLL Clock

[Resets]

- Reset requests from INITX pin
- Power on reset
- Software reset
- Watchdog timers reset
- Low voltage detector reset
- Clock supervisor reset

Clock SuperVisor (CSV)

Clocks generated by internal CR oscillators are used to supervise abnormality of the external clocks.

- External OSC clock failure (clock stop) is detected, reset is asserted.
- External OSC frequency anomaly is detected, interrupt or reset is asserted.

Low-Voltage Detector (LVD)

This Series include 2-stage monitoring of voltage on the VCC pins. When the voltage falls below the voltage has been set, Low-Voltage Detector generates an interrupt or reset.

- LVD1: error reporting via interrupt
- LVD2: auto-reset operation

Low-power Consumption Mode

Six low-power consumption modes are supported.

- Sleep
- Timer
- RTC
- Stop
- Deep standby RTC (selectable from with/without RAM retention)
- Deep standby stop (selectable from with/without RAM retention)

VBAT
The consumption power during the RTC operation can be reduced by supplying the power supply independent from the RTC (calendar circuit)/32 kHz oscillation circuit. The following circuits can also be used.

- RTC
- 32 kHz oscillation circuit
- Power-on circuit
- Back up register : 32 bytes
- Port circuit

Debug
- Serial Wire JTAG Debug Port (SWJ-DP)
- Embedded Trace Macrocells (ETM) provide comprehensive debug and trace facilities.

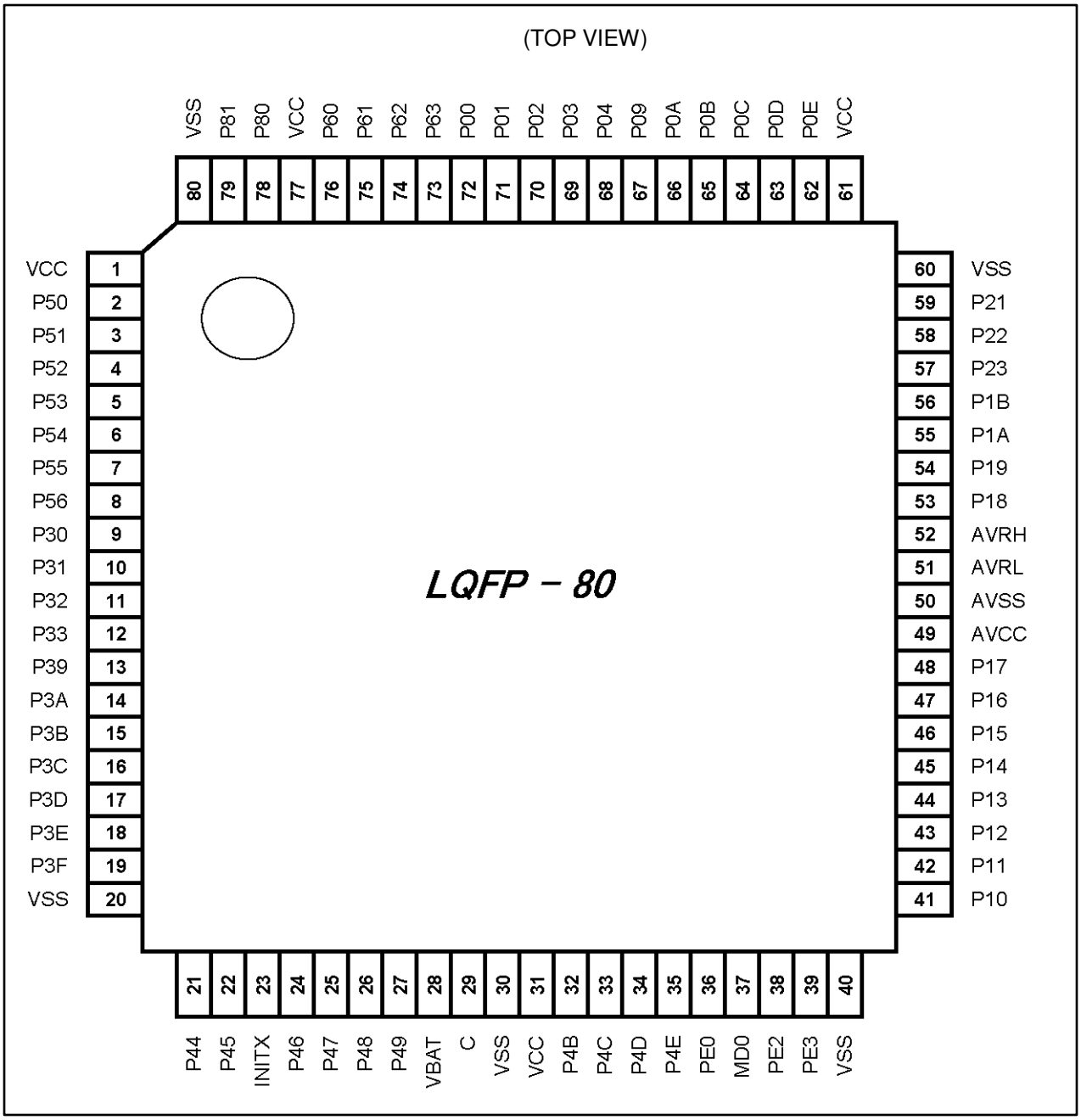
Unique ID
Unique value of the device (41-bit) is set.

Power Supply
Two Power Supplies

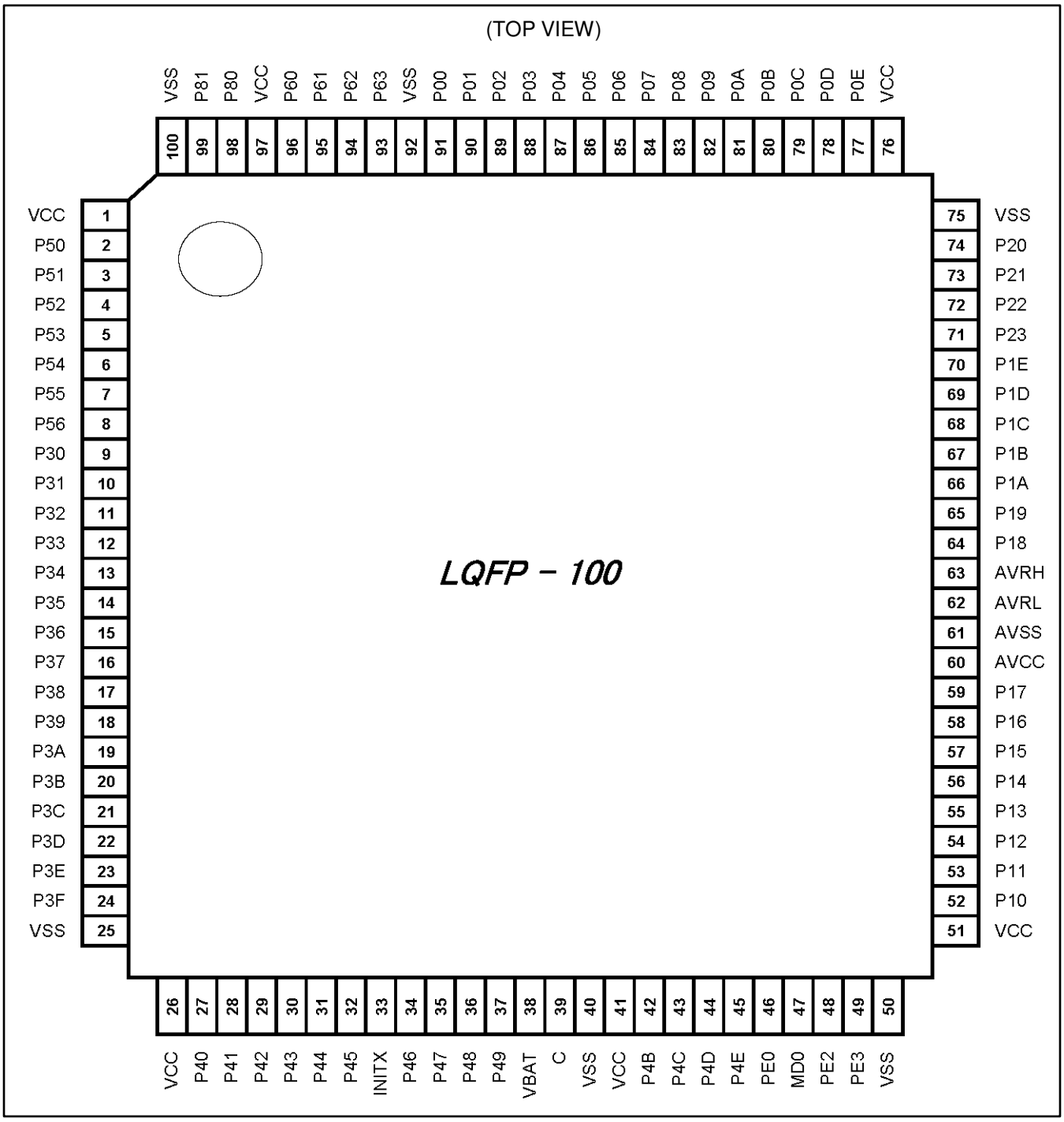
- Wide range voltage: VCC = 2.7 V to 5.5 V
- Power supply for VBAT: VBAT = 2.7 V to 5.5 V

5. Pin Assignment

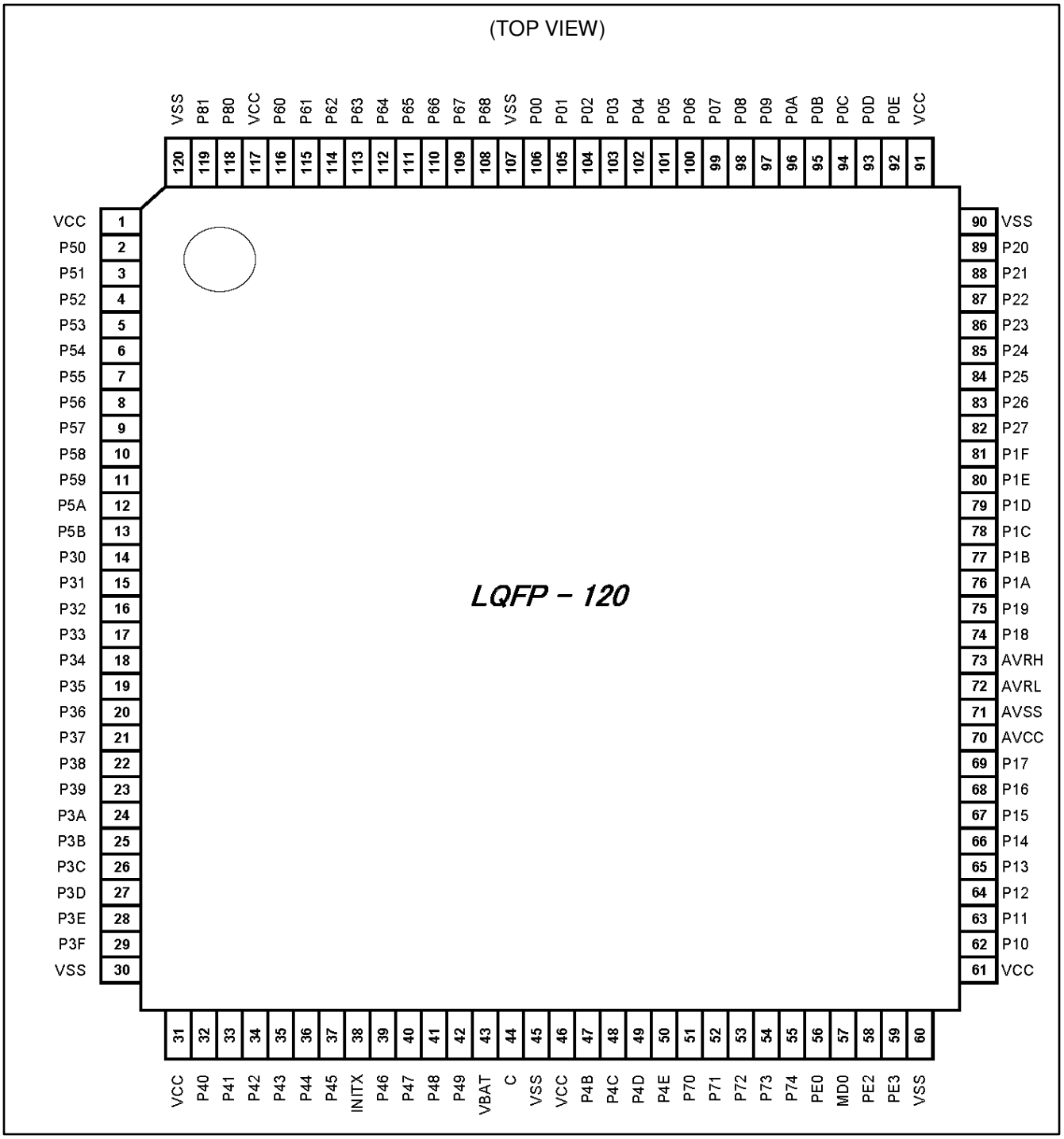
LQH080



LQI100


(TOP VIEW)
LQFP – 100
1 VCC
2 P50
3 P51
4 P52
5 P53
6 P54
7 P55
8 P56
9 P30
10 P31
11 P32
12 P33
13 P34
14 P35
15 P36
16 P37
17 P38
18 P39
19 P3A
20 P3B
21 P3C
22 P3D
23 P3E
24 P3F
25 VSS
26 VCC
27 P40
28 P41
29 P42
30 P43
31 P44
32 P45
33 INITX
34 P46
35 P47
36 P48
37 P49
38 VBAT
39 C
40 VSS
41 VCC
42 P4B
43 P4C
44 P4D
45 P4E
46 PE0
47 MD0
48 PE2
49 PE3
50 VSS
51 VCC
52 P10
53 P11
54 P12
55 P13
56 P14
57 P15
58 P16
59 P17
60 AVCC
61 AVSS
62 AVRL
63 AVRH
64 P18
65 P19
66 P1A
67 P1B
68 P1C
69 P1D
70 P1E
71 P23
72 P22
73 P21
74 P20
75 VSS
76 VCC
77 P0E
78 P0D
79 P0C
80 P0B
81 P0A
82 P09
83 P08
84 P07
85 P06
86 P05
87 P04
88 P03
89 P02
90 P01
91 P00
92 VSS
93 P63
94 P62
95 P61
96 P60
97 VCC
98 P80
99 P81
100 VSS

LQM120


(TOP VIEW)
LQFP – 120
1 VCC
2 P50
3 P51
4 P52
5 P53
6 P54
7 P55
8 P56
9 P57
10 P58
11 P59
12 P5A
13 P5B
14 P30
15 P31
16 P32
17 P33
18 P34
19 P35
20 P36
21 P37
22 P38
23 P39
24 P3A
25 P3B
26 P3C
27 P3D
28 P3E
29 P3F
30 VSS
31 VCC
32 P40
33 P41
34 P42
35 P43
36 P44
37 P45
38 INITX
39 P46
40 P47
41 P48
42 P49
43 VBAT
44 C
45 VSS
46 VCC
47 P4B
48 P4C
49 P4D
50 P4E
51 P70
52 P71
53 P72
54 P73
55 P74
56 PE0
57 MD0
58 PE2
59 PE3
60 VSS
61 VCC
62 P10
63 P11
64 P12
65 P13
66 P14
67 P15
68 P16
69 P17
70 AVCC
71 AVSS
72 AVRL
73 AVRH
74 P18
75 P19
76 P1A
77 P1B
78 P1C
79 P1D
80 P1E
81 P1F
82 P27
83 P26
84 P25
85 P24
86 P23
87 P22
88 P21
89 P20
90 VSS
91 VCC
92 P0E
93 P0D
94 P0C
95 P0B
96 P0A
97 P09
98 P08
99 P07
100 P06
101 P05
102 P04
103 P03
104 P02
105 P01
106 P00
107 VSS
108 P68
109 P67
110 P66
111 P65
112 P64
113 P63
114 P62
115 P61
116 P60
117 VCC
118 P80
119 P81
120 VSS

FDI121

(TOP VIEW)

	1	2	3	4	5	6	7	8	9	10	11
A	VSS	P81	P80	VCC	TRSTX	VSS	P06	P0A	P0D	VCC	VSS
B	VCC	P60	P61	P63	TCK	TDO	P07	P0B	P0E	P24	P20
C	P50	P51	P62	P64	TDI	TMS	P08	P0C	P25	P22	P21
D	P52	P53	P54	P65	P66	P05	P09	P26	P1E	P1D	P23
E	P30	P55	P56	P57	P67	P68	P27	P1C	P1B	P1A	P19
F	P34	P33	P32	P31	P58	P59	P1F	P18	P17	P16	AVRH
G	P35	P36	P37	P38	P5A	P5B	P72	P15	P14	P13	AVRL
H	P39	P3A	P3B	P3C	P43	P70	P71	P73	P12	P11	AVSS
J	P3D	P3E	P41	P45	P42	P4B	P4C	P4D	P74	P10	AVCC
K	VCC	P3F	P44	X1A	P48	P49	VCC	P4E	MD0	VSS	VCC
L	VSS	P40	INITX	X0A	VBAT	C	VSS	MD1	X0	X1	VSS

PFBGA-121

6. Pin Description

6.1 List of Pin Numbers

The number after the underscore ("_") in pin names such as XXX_1 and XXX_2 indicates the relocated port number. For these pins, there are multiple pins that provide the same function for the same channel. Use the extended port function register (EPFR) to select the pin.

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
1	1	1	B1	VCC	-	-
2	2	2	C1	P50	E	K
				CTS4_0		
				AIN0_2		
				RTO10_0 (PPG10_0)		
				INT00_0		
				MADATA00_0		
3	3	3	C2	P51	E	K
				RTS4_0		
				BIN0_2		
				RTO11_0 (PPG10_0)		
				INT01_0		
				MADATA01_0		
4	4	4	D1	P52	E	I
				SCK4_0 (SCL4_0)		
				ZIN0_2		
				RTO12_0 (PPG12_0)		
				MADATA02_0		
5	5	5	D2	P53	E	I
				TIOA1_2		
				SOT4_0 (SDA4_0)		
				RTO13_0 (PPG12_0)		
				MADATA03_0		
6	6	6	D3	P54	E	K
				TIOB1_2		
				SIN4_0		
				RTO14_0 (PPG14_0)		
				INT02_0		
				MADATA04_0		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
7	7	7	E2	P55 ADTG_1 SIN6_0 RTO15_0 (PPG14_0) INT07_2 MADATA05_0	E	K
8	8	8	E3	P56 SOT6_0 (SDA6_0) DTTI1X_0 INT08_2 MADATA06_0	E	K
9	-	-	E4	P57 SCK6_0 (SCL6_0) MADATA07_0 RTO20_1	E	I
10	-	-	F5	P58 SIN4_2 AIN1_0 INT04_2 MADATA08_0 RTO21_1	E	K
11	-	-	F6	P59 SOT4_2 (SDA4_2) BIN1_0 INT07_1 MADATA09_0 RTO22_1 RX1_1	E	K
12	-	-	G5	P5A SCK4_2 (SCL4_2) ZIN1_0 MADATA10_0 RTO23_1 TX1_1	E	I
13	-	-	G6	P5B CTS4_2 MADATA11_0 RTO24_1	E	I

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
14	9	9	E1	P30	E	Q
				TIOB0_1		
				RTS4_2		
				INT15_2		
				WKUP1		
-			-	MADATA07_0		
14	-	-	E1	MADATA12_0		
	9	9		RTO25_1		
15	10	10	F4	P31	I	K
				TIOB1_1		
				SIN3_1		
				INT09_2		
-			-	MADATA08_0		
15	-	-	F4	MADATA13_0		
	10	10		DTTI2X_1		
16	11	11	F3	P32	N	K
				TIOB2_1		
				SOT3_1 (SDA3_1)		
				INT10_1		
-			-	MADATA09_0		
16	-	-	F3	MADATA14_0		
17	12	12	F2	P33	N	K
				ADTG_6		
				TIOB3_1		
				SCK3_1 (SCL3_1)		
				INT04_0		
-			-	MADATA10_0		
17	-	-	F2	MADATA15_0		
18	13	-	F1	P34	E	I
				TIOB4_1		
				FRCK0_0		
				TX0_1		
-			-	MADATA11_0		
18	-	-	F1	MNALE_0		
19	14	-	G1	P35	E	K
				TIOB5_1		
				IC03_0		
				INT08_1		
				RX0_1		
-			-	MADATA12_0		
19	-	-	G1	MNCLE_0		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
20	15	-	G2	P36	E	K
				SIN5_2		
				IC02_0		
				INT09_1		
-			-	MADATA13_0		
20	-	-	G2	MNWEX_0		
21	16	-	G3	P37	E	K
				SOT5_2 (SDA5_2)		
				IC01_0		
				INT05_2		
-			-	MADATA14_0		
21	-	-	G3	MNREX_0		
22	17	-	G4	P38	E	K
				SCK5_2 (SCL5_2)		
				IC00_0		
				INT06_2		
-			-	MADATA15_0		
23	18	13	H1	P39	L	I
				ADTG_2		
				DTTI0X_0		
				RTCCO_2		
				SUBOUT_2		
		-		MSDCLK_0		
24	19	14	H2	P3A	G	I
				TIOA0_1		
				AIN0_0		
				RTO00_0 (PPG00_0)		
		-		MSDCKE_0		
25	20	15	H3	P3B	G	I
				TIOA1_1		
				BIN0_0		
				RTO01_0 (PPG00_0)		
		-		MRASX_0		
26	21	16	H4	P3C	G	I
				TIOA2_1		
				ZIN0_0		
				RTO02_0 (PPG02_0)		
		-		MCASX_0		
27	22	17	J1	P3D	G	I
				TIOA3_1		
				RTO03_0 (PPG02_0)		
				MAD00_0		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
28	23	18	J2	P3E TIOA4_1 RTO04_0 (PPG04_0) MAD01_0	G	I
29	24	19	K2	P3F TIOA5_1 RTO05_0 (PPG04_0) MAD02_0	G	I
30	25	20	L1	VSS	-	-
31	26	-	K1	VCC	-	-
32	27	-	L2	P40 TIOA0_0 RTO10_1 (PPG10_1) INT12_1	G	K
33	28	-	J3	P41 TIOA1_0 RTO11_1 (PPG10_1) INT13_1 AIN2_0	G	K
34	29	-	J5	P42 TIOA2_0 RTO12_1 (PPG12_1) MSDWEX_0 BIN2_0	G	I
35	30	-	H5	P43 ADTG_7 TIOA3_0 RTO13_1 (PPG12_1) MCSX8_0 ZIN2_0	G	I
36	31	21	K3	P44 TIOA4_0 RTO14_1 (PPG14_1) DA0	R	J
37	32	22	J4	P45 TIOB0_0 RTO15_1 (PPG14_1) DA1	R	J
38	33	23	L3	INITX	B	C

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
39	34	24	L4	P46	P	S
				X0A		
40	35	25	K4	P47	Q	T
				X1A		
41	36	26	K5	P48	O	U
				VREGCTL		
42	37	27	K6	P49	O	U
				VWAKEUP		
43	38	28	L5	VBAT	-	-
44	39	29	L6	C	-	-
45	40	30	L7	VSS	-	-
46	41	31	K7	VCC	-	-
47	42	32	J6	P4B	E	I
				TIOB1_0		
				SCS7_1		
				MAD03_0		
48	43	33	J7	P4C	N	I
				TIOB2_0		
				SCK7_1 (SCL7_1)		
				AIN1_2		
				MAD04_0		
49	44	34	J8	P4D	N	K
				TIOB3_0		
				SOT7_1 (SDA7_1)		
				BIN1_2		
				INT13_2		
				MAD05_0		
50	45	35	K8	P4E	I	Q
				TIOB4_0		
				SIN7_1		
				ZIN1_2		
				FRCK1_1		
				INT11_1		
				WKUP2		
				MAD06_0		
51	-	-	H6	P70	E	I
				TIOA4_2		
				AIN0_1		
				IC13_1		
				TX0_0		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
52	-	-	H7	P71 TIOB4_2 BIN0_1 IC12_1 INT15_1 RX0_0	E	K
53	-	-	G7	P72 TIOA6_0 SIN2_0 ZIN0_1 IC11_1 INT14_2	E	K
54	-	-	H8	P73 TIOB6_0 SOT2_0 (SDA2_0) IC10_1 INT03_2	E	K
55	-	-	J9	P74 SCK2_0 (SCL2_0) DTTI1X_1	E	I
56	46	36	L8	PE0 MD1	C	E
57	47	37	K9	MD0	J	D
58	48	38	L9	PE2 X0	A	A
59	49	39	L10	PE3 X1	A	B
60	50	40	L11	VSS	-	-
61	51	-	K11	VCC	-	-
62	52	41	J10	P10 AN00 SIN1_1 FRCK0_2 INT02_1 MAD07_0 RX1_2	F	M
63	53	42	H10	P11 AN01 SOT1_1 (SDA1_1) IC00_2 MAD08_0 TX1_2	F	L

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
64	54	43	H9	P12 AN02 SCK1_1 (SCL1_1) IC01_2 RTCCO_1 SUBOUT_1 MAD09_0	F	L
65	55	44	G10	P13 AN03 SIN0_1 IC02_2 INT03_1 MAD10_0	F	M
66	56	45	G9	P14 AN04 SOT0_1 (SDA0_1) IC03_2 MAD11_0	F	L
67	57	46	G8	P15 AN05 SCK0_1 (SCL0_1) MAD12_0 ZIN2_2 RTO22_0	F	L
68	58	47	F10	P16 AN06 SIN2_2 INT14_1 MAD13_0 BIN2_2 RTO21_0	F	M
69	59	48	F9	P17 AN07 SOT2_2 (SDA2_2) WKUP3 MAD14_0 AIN2_2 RTO20_0	F	P
70	60	49	J11	AVCC	-	-
71	61	50	H11	AVSS	-	-
72	62	51	G11	AVRL	-	-
73	63	52	F11	AVRH	-	-

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
74	64	53	F8	P18	F	L
				AN08		
				SCK2_2 (SCL2_2)		
				MAD15_0		
				DTTI2X_0		
75	65	54	E11	P19	F	M
				AN09		
				SIN4_1		
				IC00_1		
				INT05_1		
				MAD16_0		
76	66	55	E10	P1A	M	L
				AN10		
				SOT4_1 (SDA4_1)		
				IC01_1		
				MAD17_0		
77	67	56	E9	P1B	M	L
				AN11		
				SCK4_1 (SCL4_1)		
				IC02_1		
				MAD18_0		
78	68	-	E8	P1C	F	L
				AN12		
				CTS4_1		
				IC03_1		
				MAD19_0		
79	69	-	D10	P1D	F	L
				AN13		
				RTS4_1		
				DTTI0X_1		
				MAD20_0		
80	70	-	D9	P1E	F	L
				AN14		
				ADTG_5		
				FRCK0_1		
				MAD21_0		
81	-	-	F7	P1F	E	I
				ADTG_4		
				TIOB6_2		
				RTO05_1 (PPG04_1)		

Pin Number				Pin Name	I/O Circuit Type	Pin State Type
LQFP120	LQFP100	LQFP80	FBGA121			
82	-	-	E7	P27	E	K
				TIOA6_2		
				RTO04_1 (PPG04_1)		
				INT02_2		
83	-	-	D8	P26	E	I
				TIOB5_0		
				SCK2_1 (SCL2_1)		
				RTO03_1 (PPG02_1)		
84	-	-	C9	P25	E	I
				TIOA5_0		
				SOT2_1 (SDA2_1)		
				RTO02_1 (PPG02_1)		
				TX1_0		
85	-	-	B10	P24	E	K
				SIN2_1		
				RTO01_1 (PPG00_1)		
				INT01_2		
				RX1_0		
86	71	57	D11	P23	F	L
				AN15		
				TIOA7_1		
				SCK0_0 (SCL0_0)		
				RTO00_1 (PPG00_1)		
		-		MAD22_0		
87	72	58	C10	P22	F	L
				CROUT_0		
				AN16		
				TIOB7_1		
				SOT0_0 (SDA0_0)		
		-		ZIN1_1		
		58		RTO23_0		
88	73	59	C11	P21	F	M
				AN17		
				SIN0_0		
		-		BIN1_1		
		59		INT06_1		
		-		MAD23_0		
		59		RTO24_0		