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# FNB50560TD1

## Motion SPM® 55 Series

### Features

- UL Certified No. E209204 (UL1557)
- 600 V - 5 A 3-Phase IGBT Inverter Including Control IC for Gate Drive and Protections
- Low-Loss, Short-Circuit Rated IGBTs
- Built-In Bootstrap Diodes in HVIC
- Separate Open-Emitter Pins from Low-Side IGBTs for Three-Phase Current Sensing
- Active-HIGH interface, works with 3.3 / 5 V Logic, Schmitt-trigger Input
- HVIC for Gate Driving, Under-Voltage and Short-Circuit Current Protection
- Fault Output for Under-Voltage and Short-Circuit Current Protection
- Inter-Lock Function to Prevent Short-Circuit
- Shut-Down Input
- HVIC Temperature-Sensing Built-In for Temperature Monitoring
- Optimized for 15 - 20 kHz Switching Frequency
- Isolation Rating: 1500 V<sub>rms</sub> / min.

### Applications

- Motion Control - Home Appliance / Industrial Motor

### Related Resources

- [AN-9096 - Smart Power Module, Motion SPM® 55 Series User's Guide](#)
- [AN-9097 - SPM® 55 Packing Mounting Guidance](#)

### General Description

FNB50560TD1 is a Motion SPM 55 module providing a fully-featured, high-performance inverter output stage for AC Induction, BLDC, and PMSM motors. These modules integrate optimized gate drive of the built-in IGBTs to minimize EMI and losses, while also providing multiple on-module protection features including under-voltage lockouts, inter-lock function, over-current shutdown, thermal monitoring of drive IC, and fault reporting. The built-in, high-speed HVIC requires only a single supply voltage and translates the incoming logic-level gate inputs to the high-voltage, high-current drive signals required to properly drive the module's robust short-circuit-rated IGBTs. Separate negative IGBT terminals are available for each phase to support the widest variety of control algorithms.



**Figure 1. 3D Package Drawing**  
(Click to Activate 3D Content)

### Package Marking and Ordering Information

Device	Device Marking	Package	Packing Type	Quantity
FNB50560TD1	FNB50560TD1	SPMFA-A20	RAIL	13

## Integrated Power Functions

- 600 V - 5 A IGBT inverter for three phase DC / AC power conversion (Please refer to Figure 3)

## Integrated Drive, Protection and System Control Functions

- For inverter high-side IGBTs: gate drive circuit, high-voltage isolated high-speed level shifting control circuit Under-Voltage Lock-Out (UVLO) protection
- For inverter low-side IGBTs: gate drive circuit, Short-Circuit Protection (SCP) control supply circuit Under-Voltage Lock-Out (UVLO) protection
- Fault signaling: corresponding to UVLO (low-side supply) and SC faults
- Input interface: High-active interface, works with 3.3 / 5 V logic, Schmitt trigger input
- Built in Bootstrap circuitry in HVIC

## Pin Configuration

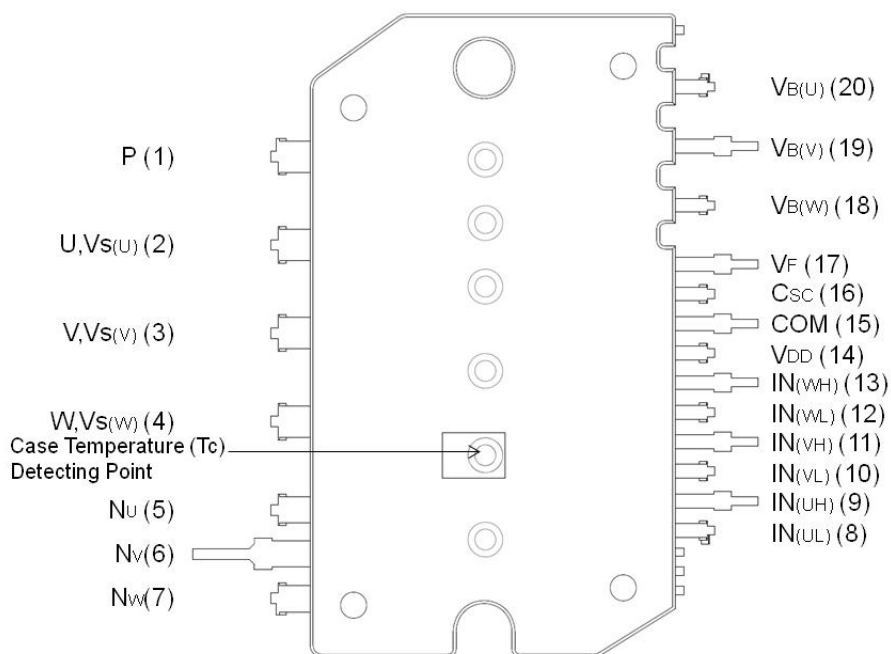


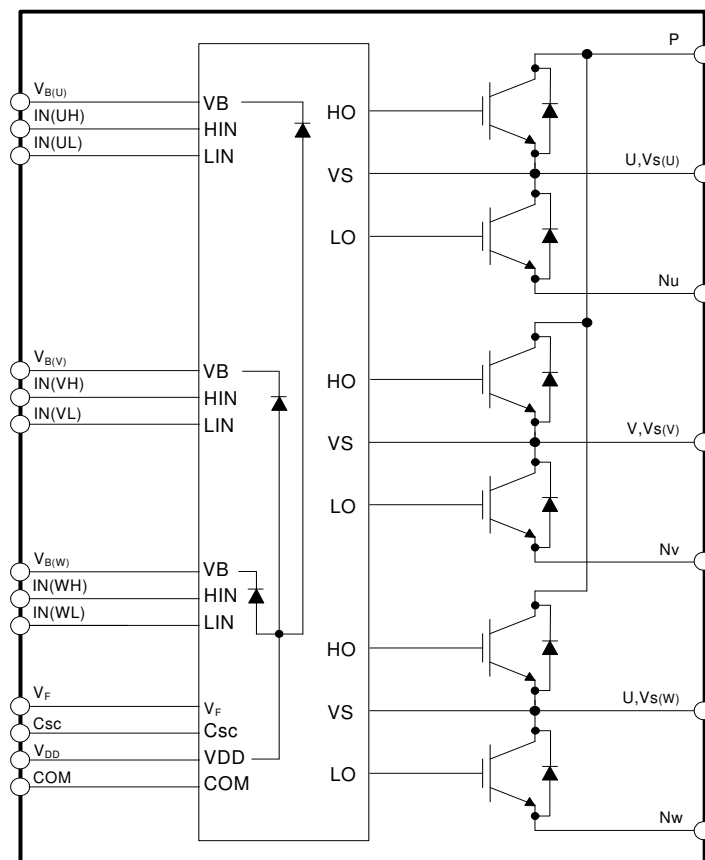
Figure 2. Top View



## Pin Descriptions

Pin Number	Pin Name	Pin Description
1	P	Positive DC-Link Input
2	U, V <sub>S</sub> (U)	Output for U Phase
3	V, V <sub>S</sub> (V)	Output for V Phase
4	W, V <sub>S</sub> (W)	Output for W Phase
5	N <sub>U</sub>	Negative DC-Link Input for U Phase
6	N <sub>V</sub>	Negative DC-Link Input for V Phase
7	N <sub>W</sub>	Negative DC-Link Input for W Phase
8	IN <sub>(UL)</sub>	Signal Input for Low-Side U Phase
9	IN <sub>(UH)</sub>	Signal Input for High-Side U Phase
10	IN <sub>(VL)</sub>	Signal Input for Low-Side V Phase
11	IN <sub>(VH)</sub>	Signal Input for High-Side V Phase
12	IN <sub>(WL)</sub>	Signal Input for Low-Side W Phase
13	IN <sub>(WH)</sub>	Signal Input for High-Side W Phase
14	V <sub>DD</sub>	Common Bias Voltage for IC and IGBTs Driving
15	COM	Common Supply Ground
16	C <sub>SC</sub>	Capacitor (Low-Pass Filter) for Short-circuit Current Detection Input
17	V <sub>F</sub>	Fault Output, Shut-Down Input, Temperature Output of Drive IC
18	V <sub>B(W)</sub>	High-Side Bias Voltage for W-Phase IGBT Driving
19	V <sub>B(V)</sub>	High-Side Bias Voltage for V-Phase IGBT Driving
20	V <sub>B(U)</sub>	High-Side Bias Voltage for U-Phase IGBT Driving

## Internal Equivalent Circuit and Input/Output Pins



**Figure 3. Internal Block Diagram**

**Note:**

1. Inverter high-side is composed of three IGBTs, freewheeling diodes, and one control IC for each IGBT.
2. Inverter low-side is composed of three IGBTs, freewheeling diodes, and one control IC for each IGBT. It has gate drive and protection functions.
3. Single drive IC has gate driver for six IGBTs and protection functions.
4. Inverter power side is composed of four inverter DC-link input terminals and three inverter output terminals.

**Absolute Maximum Ratings** ( $T_J = 25^\circ\text{C}$ , unless otherwise specified.)**Inverter Part**

Symbol	Parameter	Conditions	Rating	Unit
$V_{PN}$	Supply Voltage	Applied between P - $N_U$ , $N_V$ , $N_W$	450	V
$V_{PN(\text{Surge})}$	Supply Voltage (Surge)	Applied between P - $N_U$ , $N_V$ , $N_W$	500	V
$V_{CES}$	Collector - Emitter Voltage		600	V
* $\pm I_C$	Each IGBT Collector Current	$T_C = 25^\circ\text{C}$ , $T_J < 150^\circ\text{C}$	5	A
* $\pm I_{CP}$	Each IGBT Collector Current (Peak)	$T_C = 25^\circ\text{C}$ , $T_J < 150^\circ\text{C}$ , Under 1 ms Pulse Width	10	A
* $P_C$	Collector Dissipation	$T_C = 25^\circ\text{C}$ per Chip	19	W
$T_J$	Operating Junction Temperature	(Note 5)	-40 ~ 150	$^\circ\text{C}$

**Note:**

5. The maximum junction temperature rating of the power chips integrated within the Motion SPM® 55 product is  $150^\circ\text{C}$ .

**Control Part**

Symbol	Parameter	Conditions	Rating	Unit
$V_{DD}$	Control Supply Voltage	Applied between $V_{DD}$ - COM	20	V
$V_{BS}$	High-Side Control Bias Voltage	Applied between $V_{B(U)}$ - $V_{S(U)}$ , $V_{B(V)}$ - $V_{S(V)}$ , $V_{B(W)}$ - $V_{S(W)}$	20	V
$V_{IN}$	Input Signal Voltage	Applied between $IN_{(UH)}$ , $IN_{(VH)}$ , $IN_{(WH)}$ , $IN_{(UL)}$ , $IN_{(VL)}$ , $IN_{(WL)}$ - COM	-0.3 ~ $V_{DD} + 0.3$	V
$V_F$	Fault Supply Voltage	Applied between $V_F$ - COM	-0.3 ~ $V_{DD} + 0.3$	V
* $I_F$	Fault Current	Sink Current at $V_F$ pin	5	mA
$V_{SC}$	Current Sensing Input Voltage	Applied between $C_{SC}$ - COM	-0.3 ~ $V_{DD} + 0.3$	V

**Total System**

Symbol	Parameter	Conditions	Rating	Unit
$V_{PN(\text{PROT})}$	Self Protection Supply Voltage Limit (Short Circuit Protection Capability)	$V_{DD} = V_{BS} = 13.5 \sim 16.5 \text{ V}$ $T_J = 150^\circ\text{C}$ , Non-Repetitive, $< 2 \mu\text{s}$	400	V
$T_{STG}$	Storage Temperature		-40 ~ 125	$^\circ\text{C}$
$V_{ISO}$	Isolation Voltage Connect Pins to Heat Sink Plate	AC 60 Hz, Sinusoidal, 1 Minute	1500	$V_{\text{rms}}$

**Thermal Resistance**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$R_{th(j-c)Q}$	Junction to Case Thermal Resistance (Note 7)	Inverter IGBT part (per 1 / 6 module)	-	-	6.5	$^\circ\text{C} / \text{W}$
$R_{th(j-c)F}$		Inverter FWD part (per 1 / 6 module)	-	-	8.9	$^\circ\text{C} / \text{W}$

**Note:**

6. For Marking " \* ", These Value had been made an acquisition by the calculation considered to design factor.

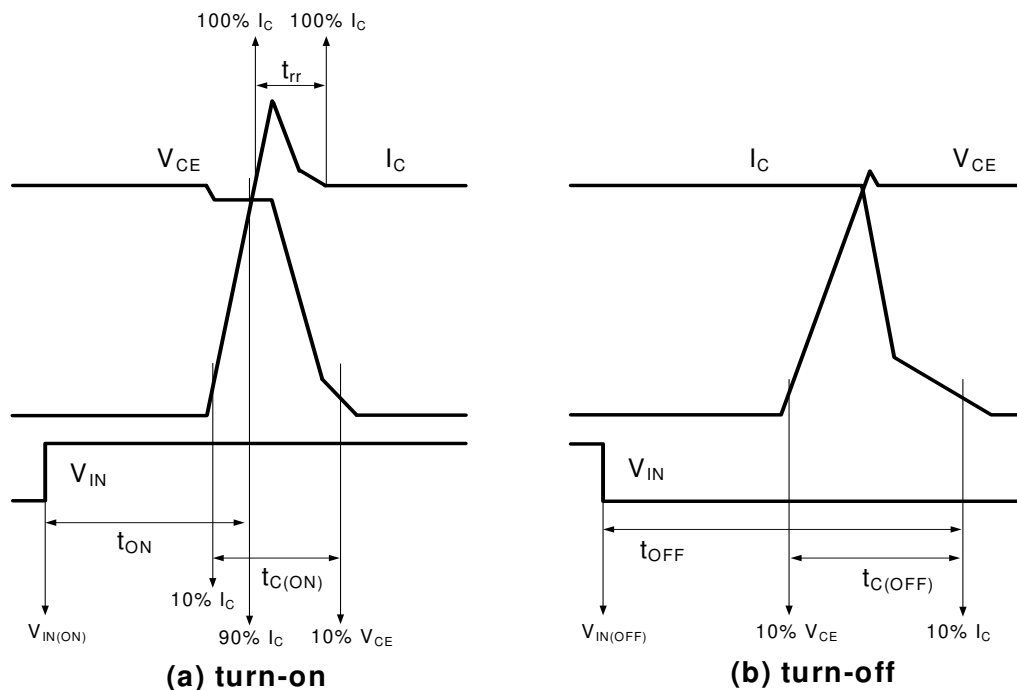
7. For the measurement point of case temperature ( $T_C$ ), please refer to Figure 2.

**Electrical Characteristics** ( $T_J = 25^\circ\text{C}$ , unless otherwise specified.)**Inverter Part**

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{CE(SAT)}$	Collector - Emitter Saturation Voltage	$V_{DD} = V_{BS} = 15\text{ V}$ $V_{IN} = 5\text{ V}$ $I_C = 4\text{ A}$ $T_J = 25^\circ\text{C}$	-	1.9	2.25	V
		$T_J = 150^\circ\text{C}$	-	2.4	-	V
$V_F$	FWDi Forward Voltage	$V_{IN} = 0\text{ V}$ $I_F = 4\text{ A}$ $T_J = 25^\circ\text{C}$	-	2.2	2.55	V
		$T_J = 150^\circ\text{C}$	-	2.0	-	V
HS	$t_{ON}$	$V_{PN} = 400\text{ V}$ , $V_{DD} = V_{BS} = 15\text{ V}$ , $I_C = 5\text{ A}$ $T_J = 25^\circ\text{C}$ $V_{IN} = 0\text{ V} \leftrightarrow 5\text{ V}$ , Inductive load (Note 8)	0.30	0.60	0.90	us
	$t_{C(ON)}$		-	0.15	0.35	us
	$t_{OFF}$		-	0.30	0.50	us
	$t_{C(OFF)}$		-	0.08	0.20	us
	$t_{rr}$		-	0.08	-	us
LS	$t_{ON}$	$V_{PN} = 400\text{ V}$ , $V_{DD} = V_{BS} = 15\text{ V}$ , $I_C = 5\text{ A}$ $T_J = 25^\circ\text{C}$ $V_{IN} = 0\text{ V} \leftrightarrow 5\text{ V}$ , Inductive load (Note 8)	0.30	0.60	0.90	us
	$t_{C(ON)}$		-	0.15	0.35	us
	$t_{OFF}$		-	0.30	0.50	us
	$t_{C(OFF)}$		-	0.08	0.20	us
	$t_{rr}$		-	0.08	-	us
$I_{CES}$	Collector - Emitter Leakage Current	$V_{CE} = V_{CES}$	-	-	1	mA

**Note:**

8.  $t_{ON}$  and  $t_{OFF}$  include the propagation delay of the internal drive IC.  $t_{C(ON)}$  and  $t_{C(OFF)}$  are the switching time of IGBT itself under the given gate driving condition internally. For the detailed information, please see Figure 4.

**Figure 4. Switching Time Definition**



## Control Part

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
I <sub>QDD</sub>	Quiescent V <sub>DD</sub> Supply Current	V <sub>DD</sub> = 15 V, IN <sub>(UH,VH,WH,UL,VL,WL)</sub> = 0 V	V <sub>DD</sub> - COM	-	1.5	2.0	mA
I <sub>PDD</sub>	Operating V <sub>DD</sub> Supply Current	V <sub>DD</sub> = 15 V, f <sub>PWM</sub> = 20 kHz, duty = 50%, applied to one PWM signal input	V <sub>DD</sub> - COM	-	2.0	2.5	mA
I <sub>QBS</sub>	Quiescent V <sub>BS</sub> Supply Current	V <sub>BS</sub> = 15 V, IN <sub>(UH, VH, WH)</sub> = 0 V	V <sub>B(U)</sub> - V <sub>S(U)</sub> , V <sub>B(V)</sub> - V <sub>S(V)</sub> , V <sub>B(W)</sub> - V <sub>S(W)</sub>	-	30	60	μA
I <sub>PBS</sub>	Operating V <sub>BS</sub> Supply Current	V <sub>DD</sub> = V <sub>BS</sub> = 15 V, f <sub>PWM</sub> = 20 kHz, duty = 50%, applied to one PWM signal input for high - side	V <sub>B(U)</sub> - V <sub>S(U)</sub> , V <sub>B(V)</sub> - V <sub>S(V)</sub> , V <sub>B(W)</sub> - V <sub>S(W)</sub>	-	500	650	μA
V <sub>FH</sub>	Fault Output Voltage	V <sub>SC</sub> = 0 V, V <sub>F</sub> Circuit: 10 kΩ to 5 V Pull-up		4.5	-	-	V
V <sub>FL</sub>		V <sub>SC</sub> = 1 V, V <sub>F</sub> Circuit: 10 kΩ to 5 V Pull-up		-	-	0.5	V
V <sub>SC(ref)</sub>	Short-Circuit Trip Level	V <sub>DD</sub> = 15 V (Note 4)		0.45	0.5	0.55	V
UV <sub>DDD</sub>	Supply Circuit Under-Voltage Protection	Detection level		10.7	11.4	12.1	V
UV <sub>DDR</sub>		Reset level		11.2	12.3	13.0	V
UV <sub>BSD</sub>		Detection level		10.1	10.8	11.5	V
UV <sub>BSR</sub>		Reset level		10.7	11.4	12.1	V
I <sub>FT</sub>	HVIC Temperature Sensing Current	V <sub>DD</sub> = V <sub>BS</sub> = 15 V, T <sub>HVIC</sub> = 25°C		68	81	95	μA
V <sub>FT</sub>	HVIC Temperature Sensing Voltage	V <sub>DD</sub> = V <sub>BS</sub> = 15 V, T <sub>HVIC</sub> = 25°C, 10 kΩ to 5 V Pull-up (Figure. 5)		4.05	4.19	4.32	V
t <sub>FOD</sub>	Fault-Out Pulse Width			40	120	-	μs
V <sub>FSDR</sub>	Shut-down Reset level	Applied between V <sub>F</sub> - COM		-	-	2.4	V
V <sub>FSDS</sub>	Shut-down Set level			0.8	-	-	V
V <sub>IN(ON)</sub>	ON Threshold Voltage	Applied between IN <sub>(UH)</sub> , IN <sub>(VH)</sub> , IN <sub>(WH)</sub> , IN <sub>(UL)</sub> , IN <sub>(VL)</sub> , IN <sub>(WL)</sub> - COM		-	-	2.4	V
V <sub>IN(OFF)</sub>	OFF Threshold Voltage			0.8	-	-	V

## Note:

9. Short-circuit protection is functioning for all six IGBTs.

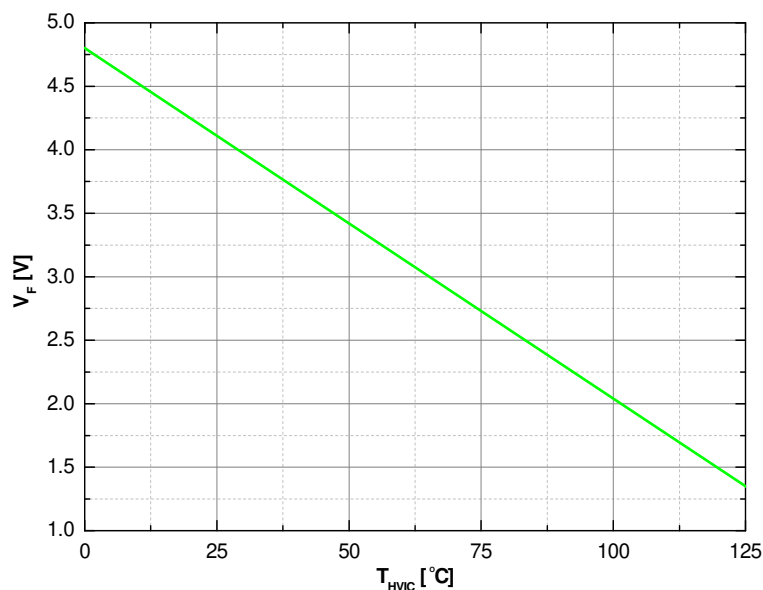


Figure. 5. V-T Curve of Temperature Output of IC (5V pull-up with 10kohm)

## Bootstrap Diode Part

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$R_{BS}$	Bootstrap Diode Resitance	$V_{DD} = 15V, T_C = 25^\circ C$	-	280	-	$\Omega$

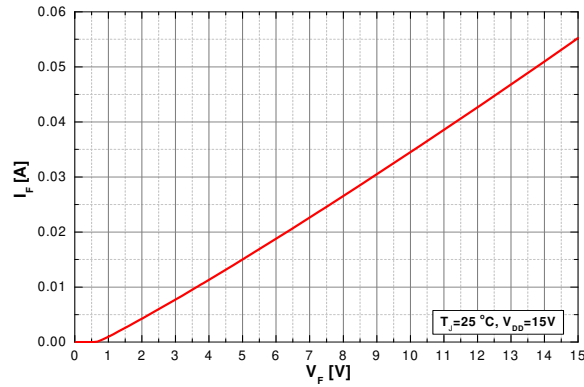


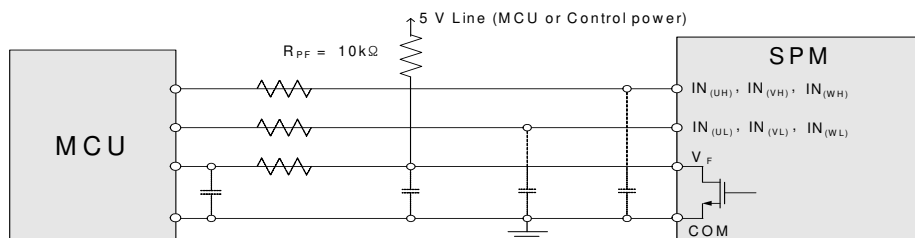
Figure 6. Built-In Bootstrap Diode Charatersts

## Recommended Operating Conditions

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{PN}$	Supply Voltage	Applied between P - $N_U, N_V, N_W$	-	300	400	V
$V_{DD}$	Control Supply Voltage	Applied between $V_{DD}$ - COM	14.0	15	16.5	V
$V_{BS}$	High - Side Bias Voltage	Applied between $V_{B(U)} - V_{S(U)}, V_{B(V)} - V_{S(V)}, V_{B(W)} - V_{S(W)}$	13.0	15	18.5	V
$dV_{DD}/dt, dV_{BS}/dt$	Control Supply Variation		-1	-	1	V / $\mu s$
$t_{dead}$	Blanking Time for Preventing Arm - Short	For each input signal	0.5	-	-	$\mu s$
$f_{PWM}$	PWM Input Signal	$-40^\circ C < T_J < 150^\circ C$	-	-	20	kHz
$V_{SEN}$	Voltage for Current Sensing	Applied between $N_U, N_V, N_W$ - COM (Including surge voltage)	-4		4	V
$P_{WIN(ON)}$	Minimun Input Pulse Width	(Note 10)	0.7	-	-	$\mu s$
$P_{WIN(OFF)}$			0.7	-	-	

**Note:**

10. This product might not make response if input pulse width is less than the recommended value.



**Note:**

11. RC coupling at each input (parts shown dotted) might change depending on the PWM control scheme used in the application and the wiring impedance of the application's printed circuit board. The input signal section of the SPM 55 product integrates 10 k $\Omega$  (typ.) pull-down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.

Figure 7. Recommended MCU I/O Interface Circuit

## Mechanical Characteristics and Ratings

Parameter	Conditions		Min.	Typ.	Max.	Unit
Device Flatness	See Figure 8		-50	-	100	μm
Mounting Torque	Mounting Screw: - M3 Note Figure 9	Recommended 0.7 N • m	0.6	0.7	0.8	N • m
		Recommended 7.1 kg • cm	5.9	6.9	7.9	kg • cm
Weight			-	6.0	-	g

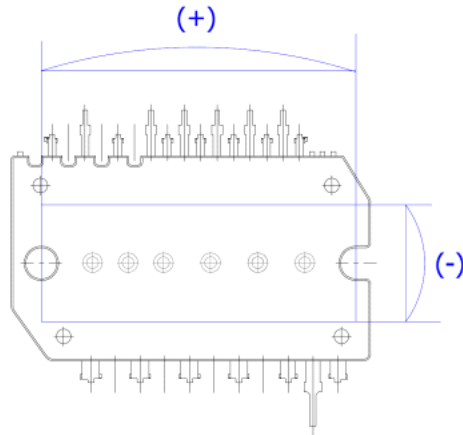


Figure 8. Flatness Measurement Position

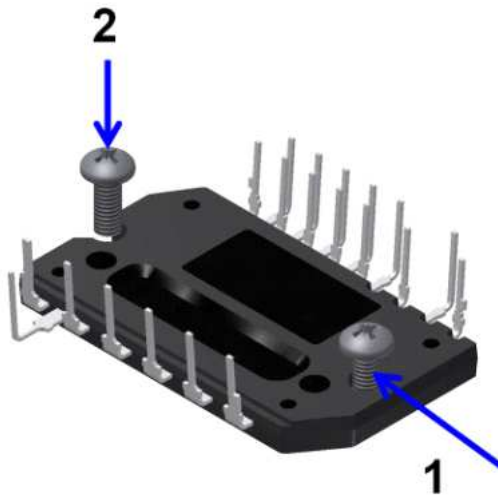
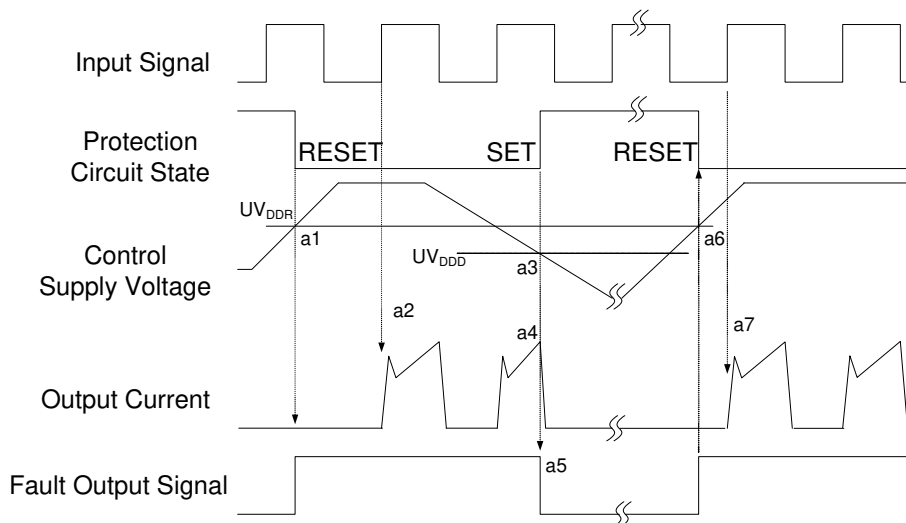


Figure 9. Mounting Screws Torque Order

**Note:**

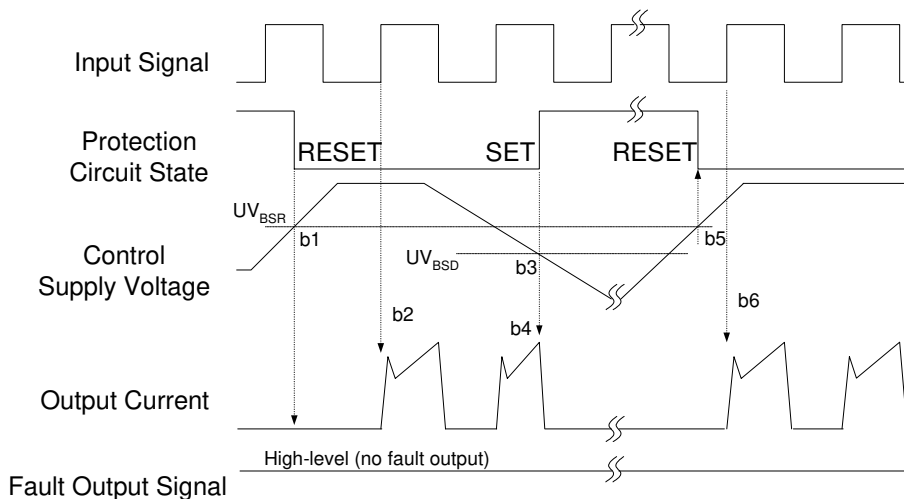
12. Do not make over torque when mounting screws. Much mounting torque may cause package cracks, as well as bolts and Al heat-sink destruction.
13. Avoid one side tightening stress. Figure 10 shows the recommended torque order for mounting screws. Uneven mounting can cause the ceramic substrate of the Motion SPM 55 product to be damaged. The Pre-screwing torque is set to 20 ~ 30 % of maximum torque rating.

## Time Charts of Protective Function



- a1 : Control supply voltage rises: After the voltage rises  $UV_{DDR}$ , the circuits start to operate when next input is applied.
- a2 : Normal operation: IGBT ON and carrying current.
- a3 : Under voltage detection ( $UV_{DDD}$ ).
- a4 : IGBT OFF in spite of control input condition.
- a5 : Fault output operation starts.
- a6 : Under voltage reset ( $UV_{DDR}$ ).
- a7 : Normal operation: IGBT ON and carrying current.

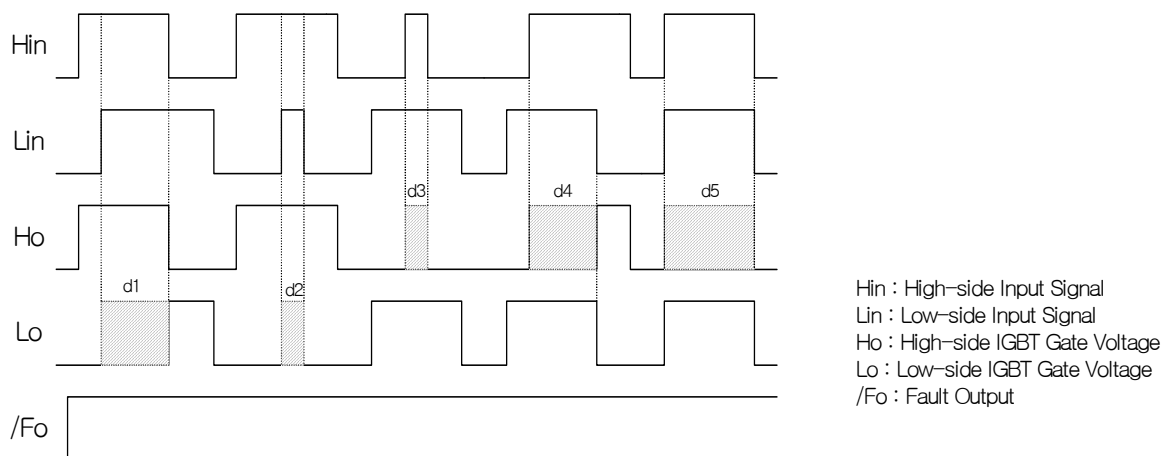
**Figure 10. Under-Voltage Protection (Low-Side)**



- b1 : Control supply voltage rises: After the voltage reaches  $UV_{BSR}$ , the circuits start to operate when next input is applied.
- b2 : Normal operation: IGBT ON and carrying current.
- b3 : Under voltage detection ( $UV_{BSD}$ ).
- b4 : IGBT OFF in spite of control input condition, but there is no fault output signal.
- b5 : Under voltage reset ( $UV_{BSR}$ )
- b6 : Normal operation: IGBT ON and carrying current

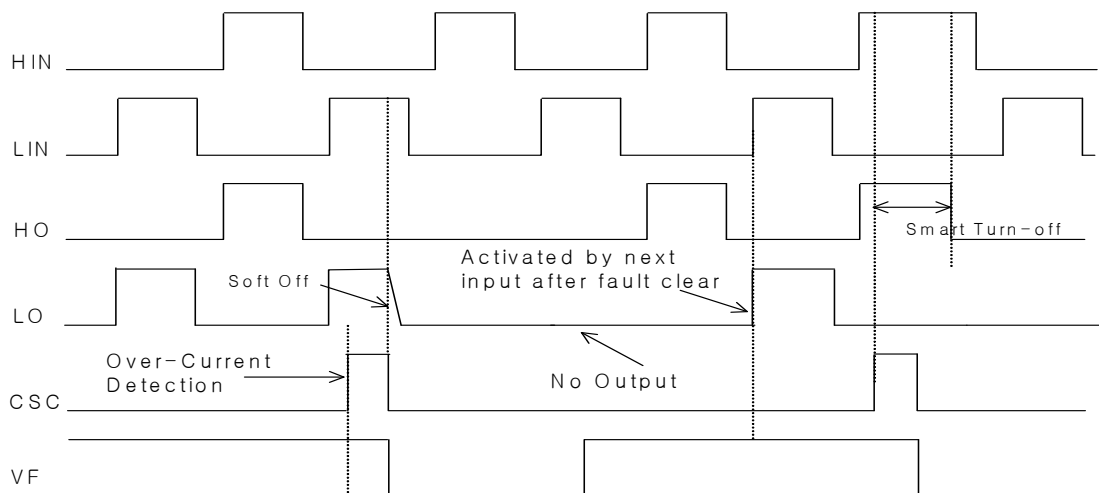
**Figure 11. Under-Voltage Protection (High-Side)**

(with the external shunt resistance and CR connection)

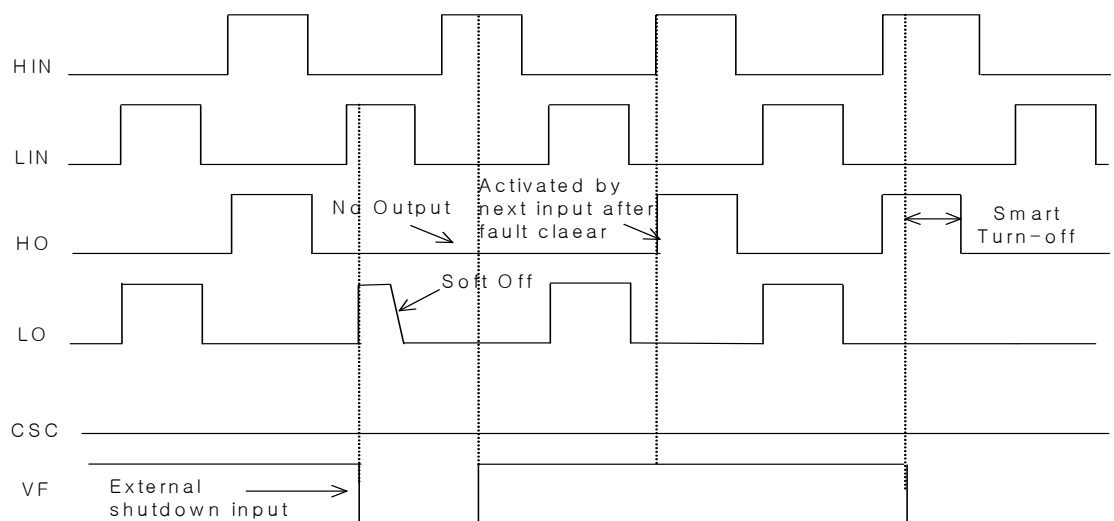


- d1 : High Side First - Input - First - Output Mode
- d2 : Low Side Noise Mode : No Lo
- d3 : High Side Noise Mode : No Ho
- d4 : Low Side First - Input - First - Output Mode
- d5 : In - Phase Mode : No Ho

**Figure 12. Inter-Lock Function**

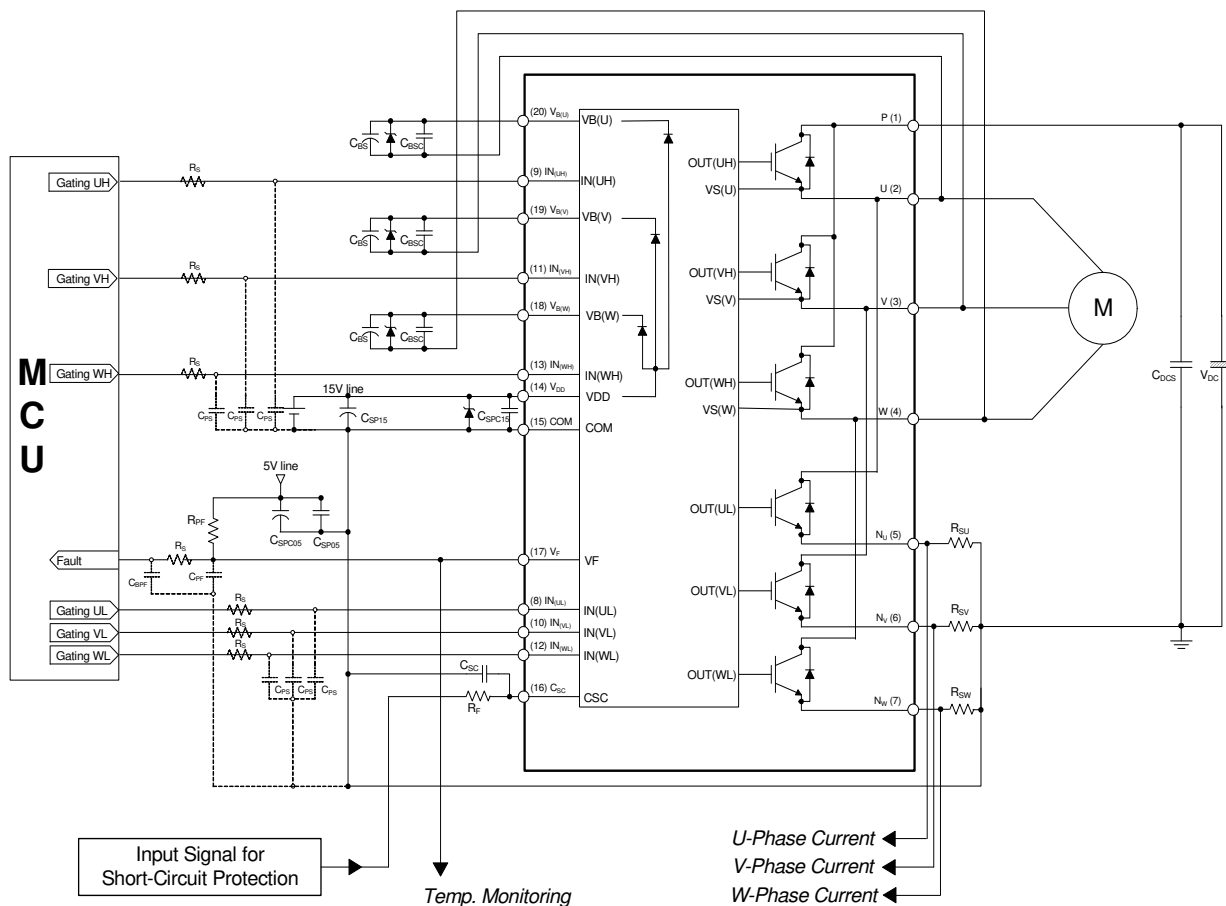


**Figure 13. Fault-Out Function By Over Current Protection**



HIN : High-side Input Signal  
 LIN : Low-side Input Signal  
 HO : High-Side Output Signal  
 LO : Low-Side Output Signal  
 CSC : Over Current Detection Input  
 VF : Shutdown Input Function

**Figure 14. Shutdown Input Function By External Command**

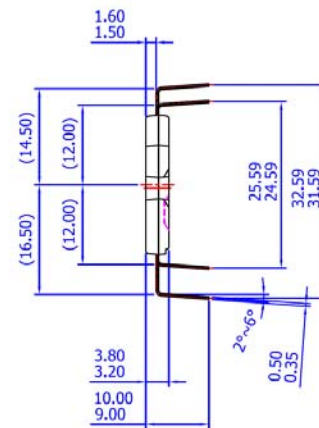
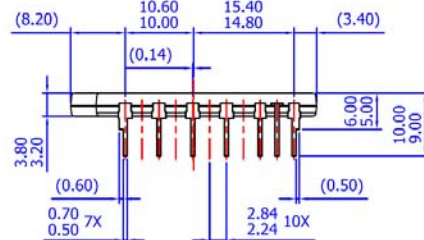
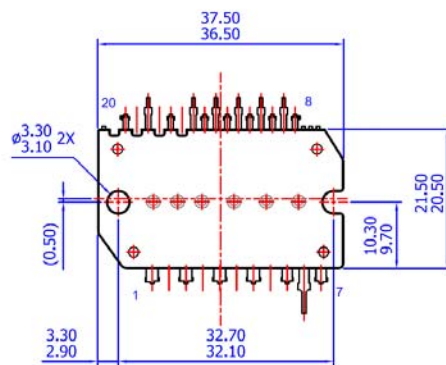
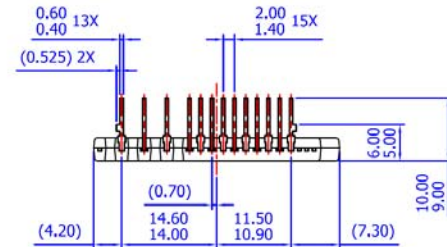
**Note:**

- 1) To avoid malfunction, the wiring of each input should be as short as possible. (less than 2 ~ 3 cm)
- 2) By virtue of integrating an application specific type of HVIC inside the SPM® 55 product, direct coupling to MCU terminals without any opto-coupler or transformer isolation is possible.
- 3)  $V_F$  is open-drain type. This signal line should be pulled up to the positive side of the MCU or control power supply with a resistor that makes  $I_{FO}$  up to 5 mA. Please refer to Figure 15.
- 4)  $C_{SP15}$  of around seven times larger than bootstrap capacitor  $C_{BS}$  is recommended.
- 5) Input signal is active-HIGH type. There is a 10 k $\Omega$  resistor inside the IC to pull down each input signal line to GND. RC coupling circuits is recommended for the prevention of input signal oscillation.  $R_S C_{PS}$  time constant should be selected in the range 50 ~ 150 ns. (Recommended  $R_S = 100 \Omega$ ,  $C_{PS} = 1 \text{ nF}$ )
- 6) To prevent errors of the protection function, the wiring around  $R_F$  and  $C_{SC}$  should be as short as possible.
- 7) In the short-circuit protection circuit, please select the  $R_F C_{SC}$  time constant in the range 1.5 ~ 2  $\mu\text{s}$ .
- 8) The connection between control GND line and power GND line which includes the  $N_U$ ,  $N_V$ ,  $N_W$  must be connected to only one point. Please do not connect the control GND to the power GND by the broad pattern. Also, the wiring distance between control GND and power GND should be as short as possible.
- 9) Each capacitor should be mounted as close to the pins of the Motion SPM 55 product as possible.
- 10) To prevent surge destruction, the wiring between the smoothing capacitor and the P and GND pins should be as short as possible. The use of a high frequency non-inductive capacitor of around 0.1 ~ 0.22  $\mu\text{F}$  between the P and GND pins is recommended.
- 11) Relays are used at almost every systems of electrical equipments of home appliances. In these cases, there should be sufficient distance between the CPU and the relays.
- 12) The zener diode or transient voltage suppressor should be adopted for the protection of ICs from the surge destruction between each pair of control supply terminals. (Recommended zener diode is 22 V / 1 W, which has the lower zener impedance characteristic than about 15  $\Omega$ )
- 13) Please choose the electrolytic capacitor with good temperature characteristic in  $C_{BS}$ . Also, choose 0.1 ~ 0.2  $\mu\text{F}$  R-category ceramic capacitors with good temperature and frequency characteristics in  $C_{BSC}$ .
- 14) For the detailed information, please refer to the application notes.

**Figur15. Typical Application Circuit**



# Detailed Package Outline Drawings (FNB50560TD1, Short Lead)



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