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December 2012

FOD8318
2.5 A Output Current, IGBT Drive Optocoupler with Active Miller Clamp, Desaturation Detection, and Isolated Fault Sensing

Features

- High noise immunity characterized by common mode rejection
  - 35 kV / µs Minimum Common Mode Rejection (Vcm = 1500 V_{peak})
- 2.5 A peak output current driving capability for most 1200 V / 150 A IGBT
- Optically isolated fault sensing feedback
- Active Miller clamp to shut off the IGBT during high dv/dt without needing a negative supply voltage
- "Soft" IGBT turn-off
- Built-in IGBT protection
  - Desaturation detection
  - Under-voltage lock out (UVLO) protection
- Wide supply voltage range from 15 V to 30 V
  - Use of P-Channel MOSFETs at output stage enables output voltage swing close to the supply rail (rail-to-rail output)
- 3.3 V / 5 V, CMOS/TTL-compatible inputs
- High Speed
  - 500 ns max. propagation delay over full operating temperature range
- Extended industrial temperate range, -40°C to 100°C temperature range
- Safety and regulatory approvals
  - UL1577, 4,243 V_{RMS} for 1 min.
  - DIN EN/IEC 60747-5-5,1,414 V_{peak} working insulation voltage, 8000 V_{peak} transient isolation voltage ratings
- $R_{DS(ON)}$ of 1 Ω (typ.) offers lower power dissipation
- User configurable: inverting, non-inverting, auto-reset, auto-shutdown
- 8 mm creepage and clearance distances

Applications

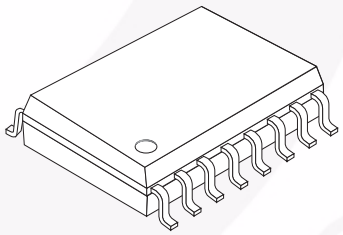
- Industrial inverter
- Induction heating
- Isolated IGBT drive

Description

The FOD8318 is an advanced 2.5 A output current IGBT drive optocoupler capable of driving most 1200 V / 150 A IGBTs. It is ideally suited for fast-switching driving of power IGBTs and MOSFETs used in motor control inverter applications and high-performance power systems. It consists of an integrated gate drive optocoupler featuring low $R_{DS(ON)}$ CMOS transistors to drive the IGBT from rail to rail and an integrated high-speed isolated feedback for fault sensing. The FOD8318 has an active Miller clamp fuction to shut off the IGBT during a high dv/dt situation without the need of a negative supply voltage. It offers critical protection features necessary for preventing fault conditions that lead to destructive thermal runaway of IGBTs.

It utilizes Fairchild's proprietary Optoplanar® coplanar packaging technology and optimized IC design to achieve high noise immunity, characterized by high common mode rejection and power supply rejection specifications.

The device is housed in a compact 16-pin small outline plastic package that meets the 8 mm creepage and clearance requirements.



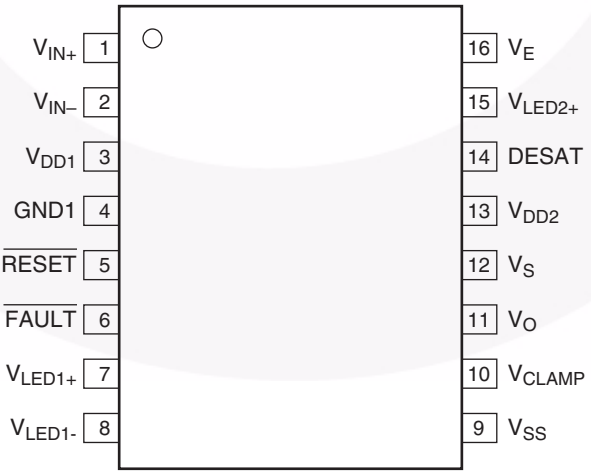
Truth Table

V_{IN+}	V_{IN-}	UVLO ($V_{DD2} - V_E$)	DESAT Detected?	$\overline{FAULT}$	V_{OUT}*
X	X	Active	X	X	LOW
X	X	X	Yes	LOW	LOW
LOW	X	X	X	X	LOW
X	HIGH	X	X	X	LOW
HIGH	LOW	Not Active	No	HIGH	HIGH

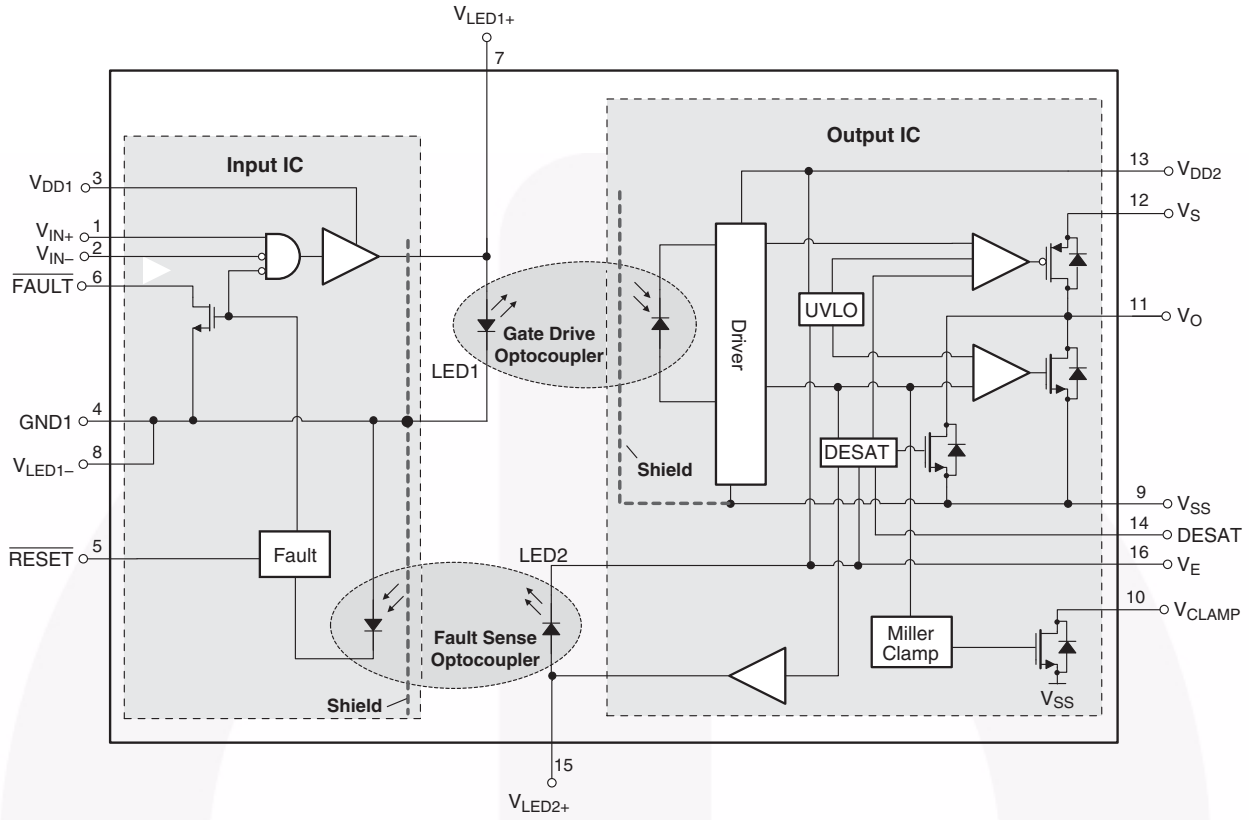
*V_{OUT} is always LOW with 'clamp' being active (gate voltage < 2 V above V_{SS}).

Pin Definitions

Pin #	Name	Description
1	V_{IN+}	Non-inverting gate drive control input
2	V_{IN-}	Inverting gate drive control input
3	V_{DD1}	Positive input supply voltage (3 V to 5.5 V)
4	GND1	Input ground
5	$\overline{RESET}$	Fault reset input
6	$\overline{FAULT}$	Fault output
7	V_{LED1+}	LED 1 anode (must be left unconnected)
8	V_{LED1-}	LED 1 cathode (must be connected to ground)
9	V_{SS}	Output supply voltage (negative)
10	V_{CLAMP}	Active Miller clamp supply voltage
11	V_O	Gate drive output voltage
12	V_S	Source of pull-up PMOS transistor
13	V_{DD2}	Positive output supply voltage
14	DESAT	Desaturation voltage input
15	V_{LED2+}	LED 2 anode (must be left unconnected)
16	V_E	Output supply voltage / IGBT emitter



Block Diagram



Safety and Insulation Ratings

As per DIN EN/IEC 60747-5-5. This optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings shall be ensured by means of protective circuits.

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Installation Classifications per DIN VDE 0110/1.89 Table 1				
	For Rated Mains Voltage < 150 Vrms		I–IV		
	For Rated Mains Voltage < 300 Vrms		I–IV		
	For Rated Mains Voltage < 450 Vrms		I–IV		
	For Rated Mains Voltage < 600 Vrms		I–IV		
	For Rated Mains Voltage < 1000 Vrms		I–III		
	Climatic Classification		40/100/21		
	Pollution Degree (DIN VDE 0110/1.89)		2		
CTI	Comparative Tracking Index	175			
V_{PR}	Input to Output Test Voltage, Method b, V_{IORM} x 1.875 = V_{PR}, 100 % Production Test with t_m = 1 s, Partial Discharge < 5 pC	2,651			V_{peak}
	Input to Output Test Voltage, Method a, V_{IORM} x 1.5 = V_{PR}, Type and Sample Test with t_m = 60 s, Partial Discharge < 5 pC	2,121			V_{peak}
V_{IORM}	Maximum Working Insulation Voltage	1,414			V_{peak}
V_{IOTM}	Highest Allowable Over Voltage	8,000			V_{peak}
	External Creepage	8			mm
	External Clearance	8			mm
	Insulation Thickness	0.5			mm
	Safety Limit Values – Maximum Values Allowed in the Event of a Failure				
T_{Case}	Case Temperature	150			°C
$P_{S,INPUT}$	Input Power	100			mW
$P_{S,OUTPUT}$	Output Power	600			mW
R_{IO}	Insulation Resistance at T_S, V_{IO} = 500 V	10^9			¾

Absolute Maximum Ratings (T_A = 25 ºC unless otherwise specified)

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Value	Units
T_{STG}	Storage Temperature	-40 to +125	ºC
T_{OPR}	Operating Temperature	-40 to +100	ºC
T_J	Junction Temperature	-40 to +125	ºC
T_{SOL}	Lead Wave Solder Temperature (no solder immersion) *Refer to page 28 for reflow temperature profile.*	260 for 10 s	ºC
$I_{\overline{FAULT}}$	Fault Output Current	15	mA
$I_{O(PEAK)}$	Peak Output Current(1)	3	A
$V_E - V_{SS}$	Negative Output Supply Voltage(2)	0 to 15	V
$V_{DD2} - V_E$	Positive Output Supply Voltage	-0.5 to 35 – ($V_E - V_{SS}$)	V
$V_{O(peak)}$	Gate Drive Output Voltage	-0.5 to 35	V
$V_{DD2} - V_{SS}$	Output Supply Voltage	-0.5 to 35	V
V_{DD1}	Positive Input Supply Voltage	-0.5 to 6	V
V_{IN+}, V_{IN-} and $V_{\overline{RESET}}$	Input Voltages	-0.5 to V_{DD1}	V
$V_{\overline{FAULT}}$	Fault Pin Voltage	-0.5 to V_{DD1}	V
V_S	Source of Pull-up PMOS Transistor Voltage	V_{SS} + 6.5 to V_{DD2}	V
V_{DESAT}	DESAT Voltage	V_E to V_E + 11	V
I_{CLAMP}	Peaking Clamping Sinking Current	1.7	A
V_{CLAMP}	Miller Clamping Voltage	-0.5 to V_{DD2}	V
PD_I	Input Power Dissipation(3)(5)	100	mW
PD_O	Output Power Dissipation(4)(5)	600	mW

Notes:

1. Maximum pulse width = 10 µs, maximum duty cycle = 0.2 %.
2. This negative output supply voltage is optional. It's only needed when negative gate drive is implemented. A schottky diode is recommended to be connected between V_E and V_{SS} to protect against a reverse voltage greater than 0.5 V. Refer to application information, *"6. Active Miller Clamp Function" on page 25*.
3. No derating required across temperature range.
4. Derate linearly above 64 °C, free air temperature at a rate of 10.2 mW/°C
5. Functional operation under these conditions is not implied. Permanent damage may occur if the device is subjected to conditions outside these ratings.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
T_A	Ambient Operating Temperature	-40	+100	ºC
V_{DD1}	Input Supply Voltage(6)	3	5.5	V
$V_{DD2} - V_{SS}$	Total Output Supply Voltage	15	30	V
$V_E - V_{SS}$	Negative Output Supply Voltage	0	15	V
$V_{DD2} - V_E$	Positive Output Supply Voltage(6)	15	$30 - (V_E - V_{SS})$	V
V_S	Source of Pull-up PMOS Transistor Voltage	$V_{SS} + 7.5$	V_{DD2}	V

Note:

6. During power up or down, it is important to ensure that VIN+ remains LOW until both the input and output supply voltages reach the proper recommended operating voltage to avoid any momentary instability at the output state. *Refer to "Time to Good Power" section on page 25.*

Isolation Characteristics

Apply over all recommended conditions, typical value is measured at T_A = 25 ºC

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{ISO}	Input-Output Isolation Voltage	T_A = 25 ºC, R.H.< 50 %, t = 1.0 min, I_{I-O} ð 10 µA, 50 Hz(7)(8)(9)	4,243			V_{RMS}
R_{ISO}	Isolation Resistance	V_{I-O} = 500 V(7)		10^{11}		¾
C_{ISO}	Isolation Capacitance	V_{I-O} = 0 V, freq = 1.0 MHz(7)		1		pF

Notes:

7. Device is considered a two terminal device: pins 1 to 8 are shorted together and pins 9 to 16 are shorted together.
8. 4,243 V_{RMS} for 1-minute duration is equivalent to 5,091 V_{RMS} for 1-second duration.
9. The Input-Output Isolation Voltage is a dielectric voltage rating as per UL1577. It should not be regarded as an input-output continuous voltage rating. For the continuous working voltage rating, refer to the equipment level safety specification or *DIN EN/IEC 60747-5-5 Safety and Insulation Ratings Table on page 4*.

Electrical Characteristics

Apply over all recommended conditions; typical value is measured at V_{DD1} = 5 V, $V_{DD2} - V_{SS}$ = 30 V, $V_E - V_{SS}$ = 0 V, T_A = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Figure
V_{IN+L}, V_{IN-L}, $V_{\overline{RESETL}}$	Logic Low Input Voltages				0.8	V	
V_{IN+H}, V_{IN-H}, $V_{\overline{RESETH}}$	Logic High Input Voltages		2.0			V	
I_{IN+L}, I_{IN-L}, $I_{\overline{RESETL}}$	Logic Low Input Currents	V_{IN} = 0.4 V	-0.5	-0.001		mA	
$I_{\overline{FAULTL}}$	$\overline{FAULT}$ Logic Low Output Current	$V_{\overline{FAULT}}$ = 0.4 V	5.0	12.0		mA	1, 35
$I_{\overline{FAULTH}}$	$\overline{FAULT}$ Logic High Output Current	$V_{\overline{FAULT}} = V_{DD1}$	-40	0.002		µA	35
I_{OH}	High Level Output Current	$V_O = V_{DD2} - 3$ V	-1	-3		A	2, 7, 36
		$V_O = V_{DD2} - 6$ V(10)	-2.5			A	

Electrical Characteristics (Continued)

Apply over all recommended conditions; typical value is measured at V_{DD1} = 5 V, $V_{DD2} – V_{SS}$ = 30 V, $V_E – V_{SS}$ = 0 V, T_A = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Figure
I_{OL}	Low Level Output Current	$V_O = V_{SS} + 3$ V	1	3		A	3, 37
		$V_O = V_{SS} + 6$ V(11)	2.5			A	
I_{OLF}	Low Level Output Current During Fault Condition	$V_O – V_{SS}$ = 14 V	90	185	230	mA	4, 41
V_{OH}	High Level Output Voltage	I_O = –100 mA (12)(13)(14)	V_S – 1.0 V	V_S – 0.5 V		V	5, 7, 38
V_{OL}	Low Level Output Voltage	I_O = 100 mA		0.1	0.5	V	6, 8, 38
I_{DD1H}	High Level Supply Current	$V_{IN+} = V_{DD1}$ = 5.5 V, $V_{IN–}$ = 0 V		14	17	mA	9, 39
I_{DD1L}	Low Level Supply Current	$V_{IN+} = V_{IN-}$ = 0 V, V_{DD1} = 5.5 V		2	3	mA	
I_{DD2H}	High Level Output Supply Current	V_O = Open(14)		1	3	mA	10, 11, 40
I_{DD2L}	Low Level Output Supply Current	V_O = Open		0.8	2.8	mA	
I_{SH}	High Level Source Current	I_O = 0 mA		0.65	1.5	mA	40
I_{SL}	Low Level Source Current	I_O = 0 mA		0.6	1.4	mA	40
I_{EL}	V_E Low Level Supply Current		-0.5	-0.2		mA	13, 40
I_{EH}	V_E High Level Supply Current		-0.5	-0.25		mA	
I_{CHG}	Blanking Capacitor Charge Current	V_{DESAT} = 2 V(14)(15)	-0.13	-0.25	-0.37	mA	12, 41
I_{DSCHG}	Blanking Capacitor Discharge Current	V_{DESAT} = 7 V	10	36		mA	41
V_{UVLO+}	Under-Voltage Lockout Threshold(14)	V_O > 5 V at 25 °C		11.5	13.5	V	15, 29, 42
V_{UVLO-}		V_O < 5 V at 25 °C	9	10		V	
$UVLO_{HYS}$	Under-Voltage Lockout Threshold Hysteresis	At 25 °C	0.4	1.5		V	
V_{DESAT}	DESAT Threshold(14)	$V_{DD2} – V_E > V_{UVLO-}$, V_O < 5 V	6	7	9	V	16, 41
V_{CLAMP_THRES}	Clamping Threshold Voltage			2.2		V	33, 52
I_{CLAMPL}	Clamp Low Level Sinking Current	$V_O = V_{SS} + 2.5$ V	0.35	1.2		A	32, 51

Notes:

10. Maximum pulse width = 10 µs, maximum duty cycle = 0.2 %.
11. Maximum pulse width = 4.99 ms, maximum duty cycle = 99.8 %.
12. V_{OH} is measured with the DC load current in this testing (maximum pulse width = 1 ms, maximum duty cycle = 20 %). When driving capacitive loads, V_{OH} approaches V_{DD} as I_{OH} approaches zero units.
13. Positive output supply voltage ($V_{DD2} – V_E$) should be at least 15 V. This ensures adequate margin in excess of the maximum under-voltage lockout threshold V_{UVLO+} of 13.5 V.
14. When $V_{DD2} – V_E > V_{UVLO}$ and output state V_O of the FOD8318 is allowed to go HIGH, the DESAT detection feature is active and provides the primary source of IGBT protection. UVLO is needed to ensure DESAT detection is functional.
15. The blanking time, t_{BLANK}, is adjustable by an external capacitor (C_{BLANK}) where $t_{BLANK} = C_{BLANK} * (V_{DESAT} / I_{CHG})$.

Switching Characteristics

Apply over all recommended conditions; typical value is measured at V_{DD1} = 5 V, $V_{DD2} - V_{SS}$ = 30 V, $V_E - V_{SS}$ = 0 V, T_A = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Figure
t_{PHL}	Propagation Delay Time to Logic Low Output[17]	Rg = 10 ¾, Cg = 10 nF, f = 10 kHz, Duty Cycle = 50 %[16]		300	500	ns	17, 18, 19, 20, 21, 22, 43, 51
t_{PLH}	Propagation Delay Time to Logic High Output[18]			250	500	ns	
PWD	Pulse Width Distortion, $\lvert t_{PHL} - t_{PLH} \rvert$[19]			50	300	ns	
PDD Skew	Propagation Delay Difference Between Any Two Parts or Channels, ($t_{PHL} - t_{PLH}$)[20]		–350		350	ns	
t_R	Output Rise Time (10 % – 90 %)			34		ns	43, 53
t_F	Output Fall Time (90 % – 10 %)			34		ns	
$t_{DESAT(90\ \%)}$	DESAT Sense to 90 % V_O Delay[21]	Rg = 10 ¾, Cg = 10 nF, $V_{DD2} - V_{SS}$ = 30 V		850		ns	23, 44
$t_{DESAT(10\ \%)}$	DESAT Sense to 10 % V_O Delay[21]			2	3	µs	24, 26, 27, 44
$t_{DESAT(\overline{FAULT})}$	DESAT Sense to Low Level $\overline{FAULT}$ Signal Delay[22]			1.8	5	µs	25, 44, 54
$t_{DESAT(LOW)}$	DESAT Sense to DESAT Low Propagation Delay[23]			850		ns	44
$t_{\overline{RESET}(\overline{FAULT})}$	$\overline{RESET}$ to High Level $\overline{FAULT}$ Signal Delay[24]		3	6	20	µs	28, 45, 54
$PW_{\overline{RESET}}$	$\overline{RESET}$ Signal Pulse Width		1.2			µs	
$t_{UVLO\ ON}$	UVLO Turn On Delay[25]	V_{DD2} = 20 V in 1.0ms Ramp		4		µs	29, 46
$t_{UVLO\ OFF}$	UVLO Turn Off Delay[26]			3		µs	
t_{GP}	Time to Good Power[27]	V_{DD2} = 0 to 30 V in 10 µs Ramp		30		µs	30, 31, 46
$\lvert CM_H \rvert$	Common Mode Transient Immunity at Output High	T_A = 25 ºC, V_{DD1} = 5 V, V_{DD2} = 25 V, V_{SS} = Ground, V_{CM} = 1500 V_{peak}[28]	35	50		kV/µs	48, 49
$\lvert CM_L \rvert$	Common Mode Transient Immunity at Output Low	T_A = 25 ºC, V_{DD1} = 5 V, V_{DD2} = 25 V, V_{SS} = Ground, V_{CM} = 1500 V_{peak}[29]	35	50		kV/µs	47, 50

Notes:

16. This load condition approximates the gate load of a 1200 V / 150 A IGBT.
17. t_{PHL} propagation delay is measured from the 50 % level on the falling edge of the input pulse (V_{IN+}, V_{IN-}) to the 50 % level of the falling edge of the V_O signal. *Refer to Figure 53.*
18. t_{PHL} propagation delay is measured from the 50 % level on the rising edge of the input pulse (V_{IN+}, V_{IN-}) to the 50 % level of the rising edge of the V_O signal. *Refer to Figure 53.*
19. PWD is defined as $\lvert t_{PHL} - t_{PLH} \rvert$ for any given device.
20. The difference between t_{PHL} and t_{PLH} between any two FOD8318 parts under same operating conditions, with equal loads.
21. This is the amount of time the DESAT threshold must be exceeded before V_O begins to go LOW. This is supply voltage dependent. *Refer to Figure 54.*

22. This is the amount of time from when the DESAT threshold is exceeded, until the $\overline{\text{FAULT}}$ output goes LOW. *Refer to Figure 54.*
23. This is the amount of time the DESAT threshold must be exceeded before V_O begins to go LOW and the $\overline{\text{FAULT}}$ output to go LOW. *Refer to Figure 54.*
24. This is the amount of time from when $\overline{\text{RESET}}$ is asserted LOW, until $\overline{\text{FAULT}}$ output goes HIGH. *Refer to Figure 54.*
25. $t_{UVLO\ ON}$ UVLO turn-on delay is measured from V_{UVLO+} threshold voltage of the output supply voltage (V_{DD2}) to the 5 V level of the rising edge of the V_O signal.
26. $t_{UVLO\ OFF}$ UVLO turn-off delay is measured from V_{UVLO-} threshold voltage of the output supply voltage (V_{DD2}) to the 5 V level of the falling edge of the V_O signal.
27. t_{GP} time to good power is measured from 13.5 V level of the rising edge of the output supply voltage (V_{DD2}) to the 5 V level of the rising edge of the V_O signal.
28. Common mode transient immunity at output HIGH state is the maximum tolerable negative dVcm / dt on the trailing edge of the common mode pulse, V_{CM}, to assure that the output remains in HIGH state (i.e., V_O > 15 V or $\overline{\text{FAULT}}$ > 2 V).
29. Common mode transient immunity at output LOW state is the maximum positive tolerable dVcm / dt on the leading edge of the common mode pulse, V_{CM}, to assure that the output remains in a LOW state (i.e., V_O < 1.0 V or $\overline{\text{FAULT}}$ < 0.8 V).

Typical Performance Characteristics

Figure 1. Fault Logic Low Output Current ($I_{\overline{FAULTL}}$) vs. Fault Logic Low Output Voltage ($V_{\overline{FAULTL}}$)

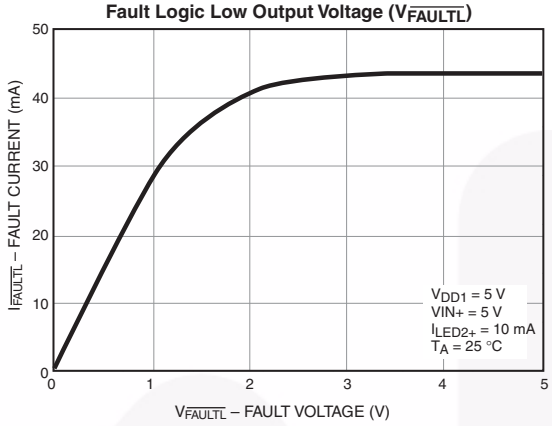


Figure 2. Output High Current (I_{OH}) vs. Temperature

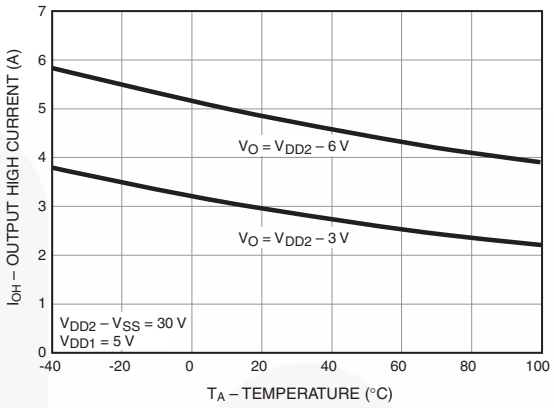


Figure 3. Output Low Current (I_{OL}) vs. Temperature

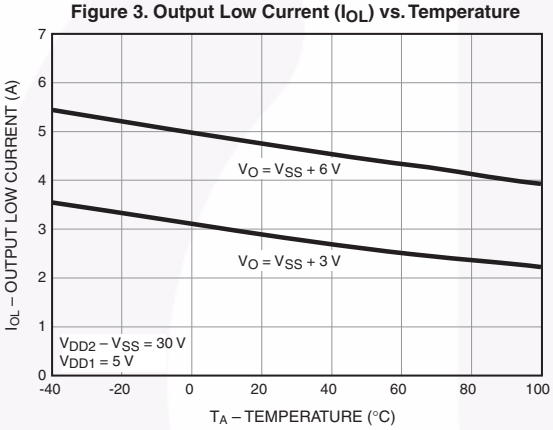


Figure 4. Low Level Output Current (I_{OLF}) vs. Output Voltage (V_O)

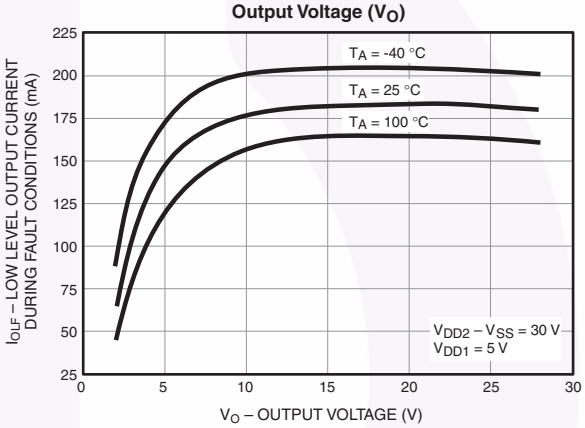


Figure 5. Output High Voltage (V_{OH}–V_{DD2}) vs. Temperature

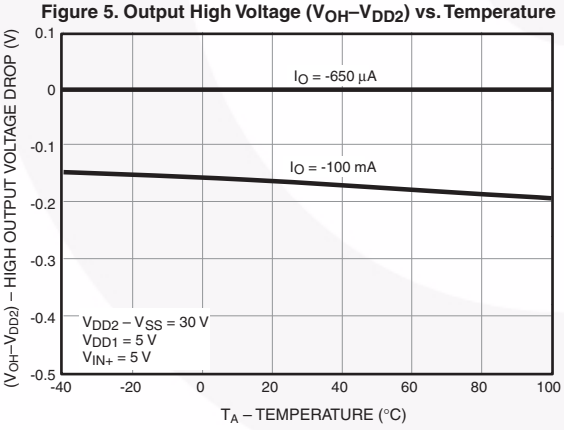
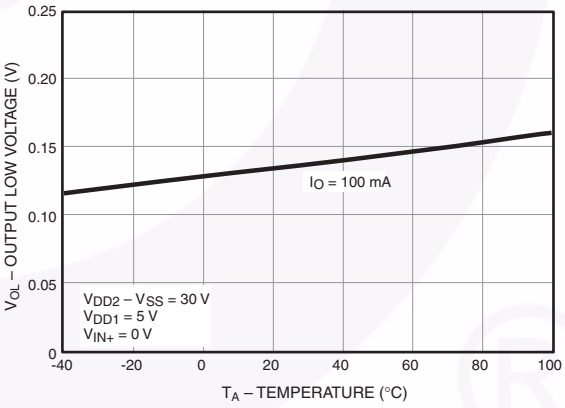


Figure 6. Output Low Voltage (V_{OL}) vs. Temperature



Typical Performance Characteristics (Continued)

Figure 7. Output High Voltage (V_{OH}) vs. Output High Current (I_{OH})

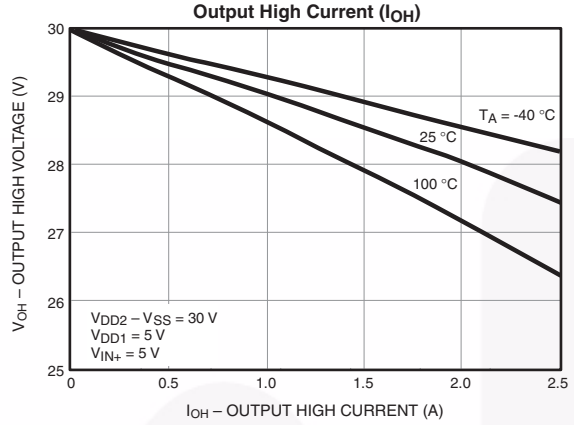


Figure 8. Output Low Voltage (V_{OL}) vs. Output Low Current (I_{OL})

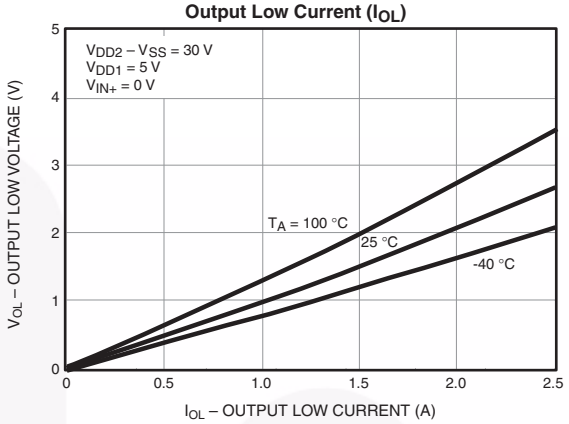


Figure 9. Supply Current (I_{DD1}) vs. Temperature

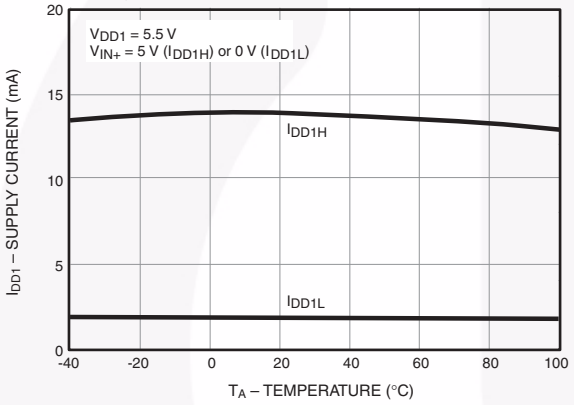


Figure 10. Output Supply Current (I_{DD2}) vs. Temperature

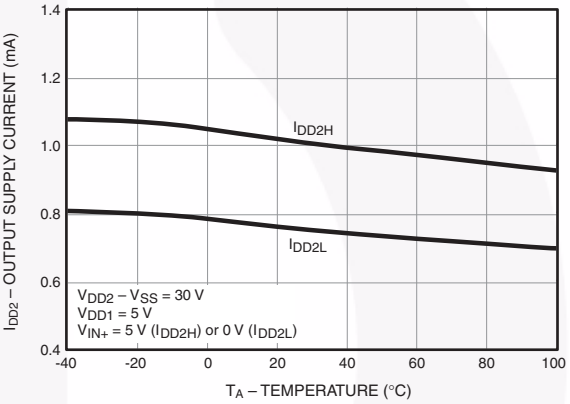


Figure 11. Output Supply Current (I_{DD2}) vs. Output Supply Voltage (V_{DD2})

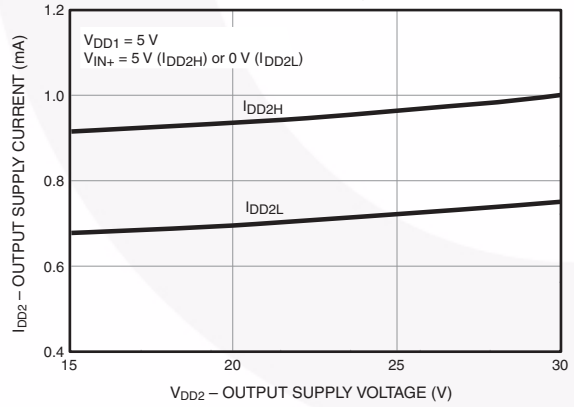
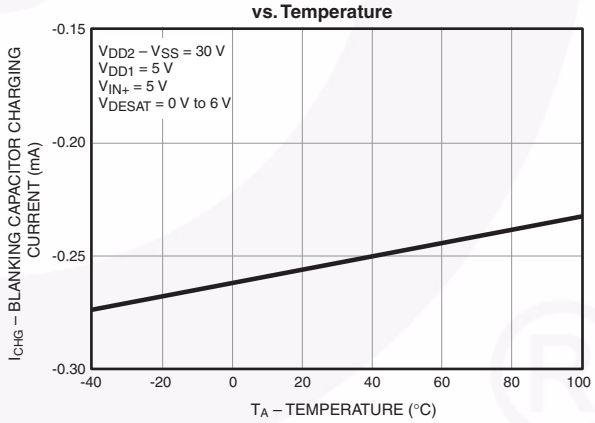


Figure 12. Blanking Capacitor Charging Current (I_{CHG}) vs. Temperature



Typical Performance Characteristics (Continued)

Figure 13. Supply Current (I_E) vs. Temperature

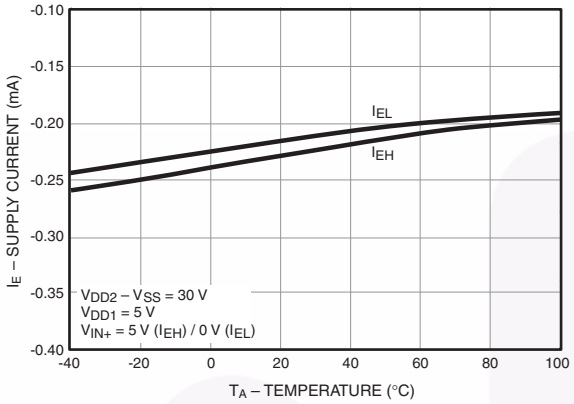


Figure 14. Source Current (I_S) vs. Output Current (I_O)

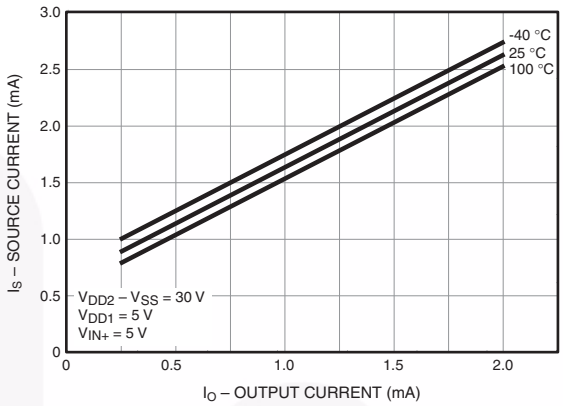


Figure 15. Under-Voltage Lockout Threshold (V_{UVLO}) vs. Temperature

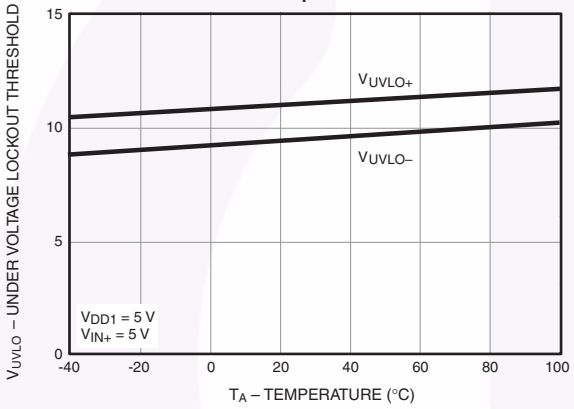


Figure 16. DESAT Threshold (V_{DESAT}) vs. Temperature

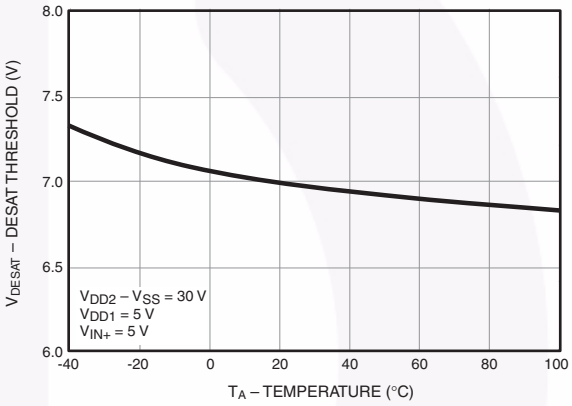


Figure 17. Propagation Delay (t_P) vs. Temperature

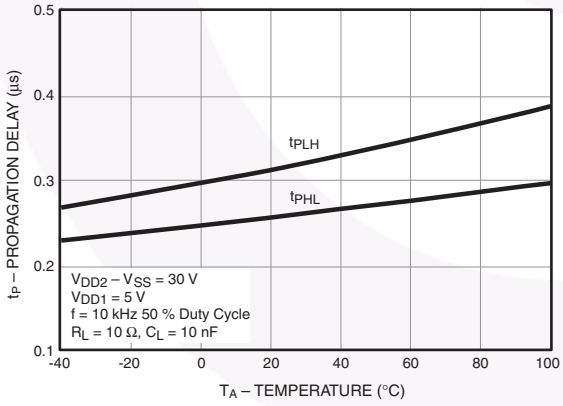
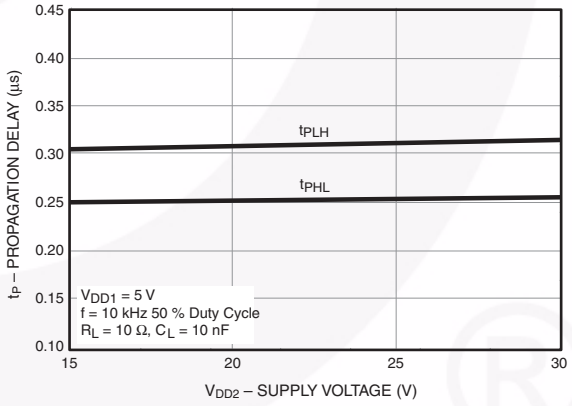


Figure 18. Propagation Delay (t_P) vs. Supply Voltage (V_{DD2})



Typical Performance Characteristics (Continued)

Figure 19. Propagation Delay to Logic High Output (t_{PLH}) vs. Temperature

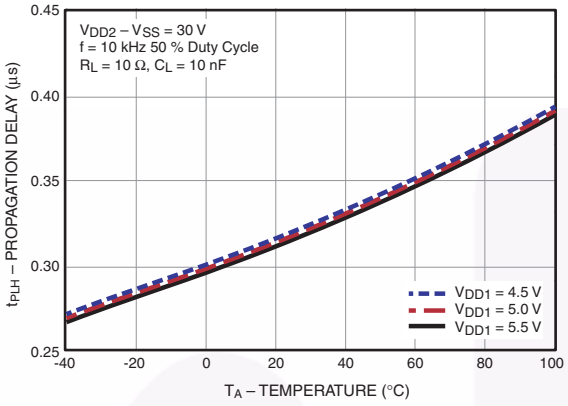


Figure 20. Propagation Delay to Logic Low Output (t_{PHL}) vs. Temperature

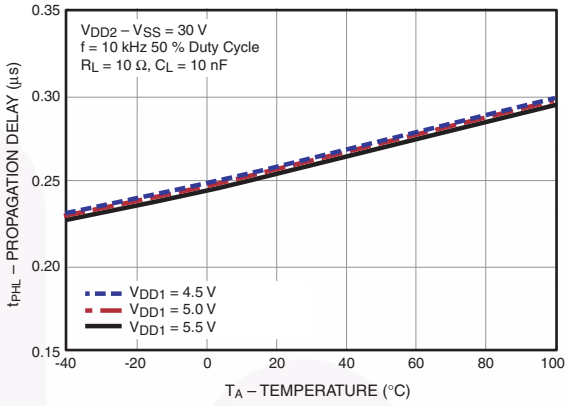


Figure 21. Propagation Delay (t_P) vs. Load Capacitance (C_L)

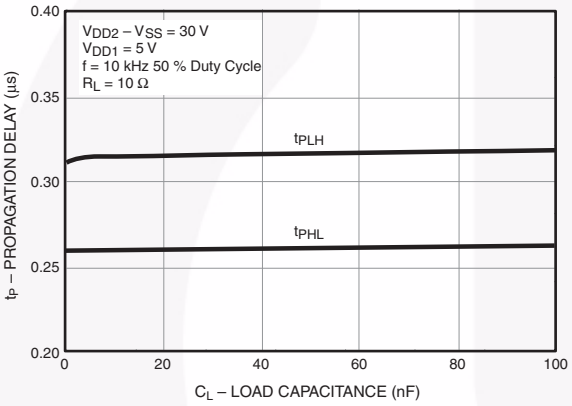


Figure 22. Propagation Delay (t_P) vs. Load Resistance (R_L)

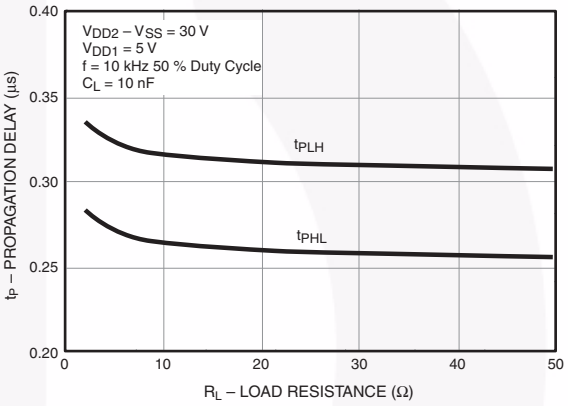


Figure 23. DESAT Sense to 90 % V_O ($t_{DESAT(90\ \%)}$) vs. Temperature

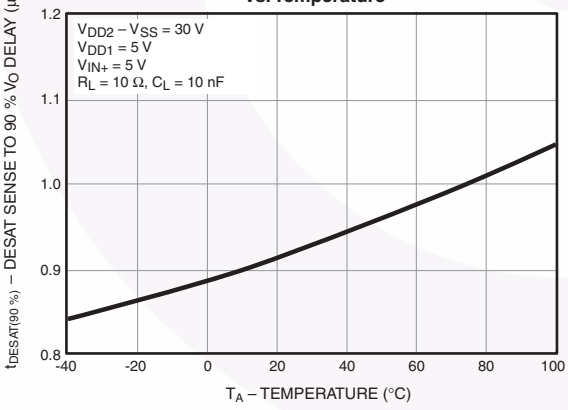
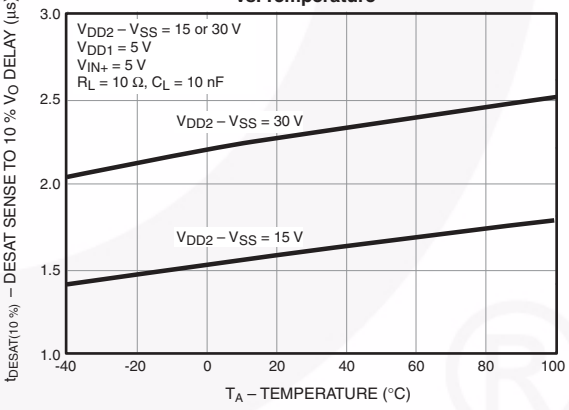


Figure 24. DESAT Sense to 10 % V_O Delay ($t_{DESAT(10\ \%)}$) vs. Temperature



Typical Performance Characteristics (Continued)

Figure 25. DESAT Sense to Low Fault Signal Delay ($t_{DESAT(\overline{FAULT})}$) vs. Temperature

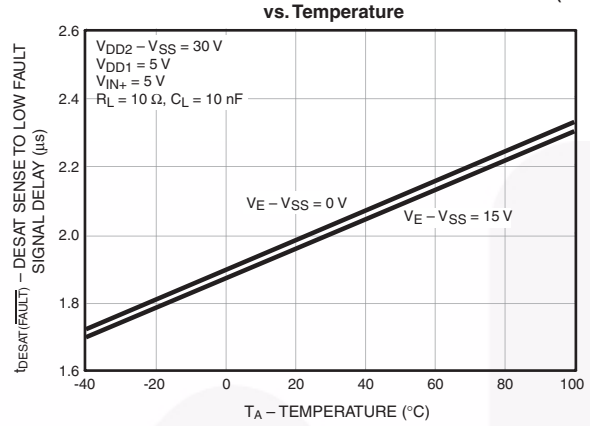


Figure 26. DESAT Sense to 10 % V_O Delay ($t_{DESAT(10\ \%)}$) vs. Load Capacitance (C_L)

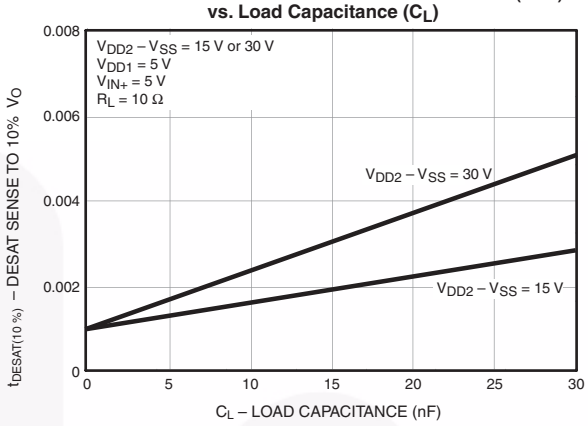


Figure 27. DESAT Sense to 10 % V_O Delay ($t_{DESAT(10\ \%)}$) vs. Load Resistance (R_L)

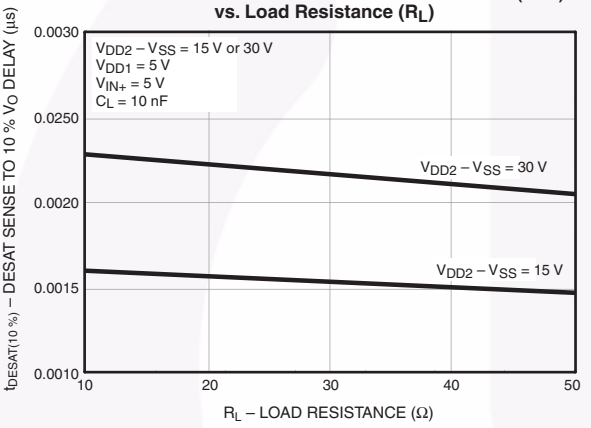


Figure 28. RESET to High Level FAULT Signal Delay ($t_{\overline{RESET}(\overline{FAULT})}$) vs. Temperature

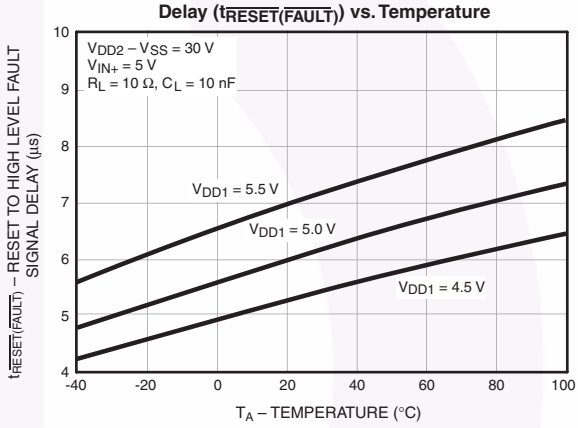


Figure 29. Under Voltage Lockout Threshold Delay (t_{UVLO}) vs. Temperature

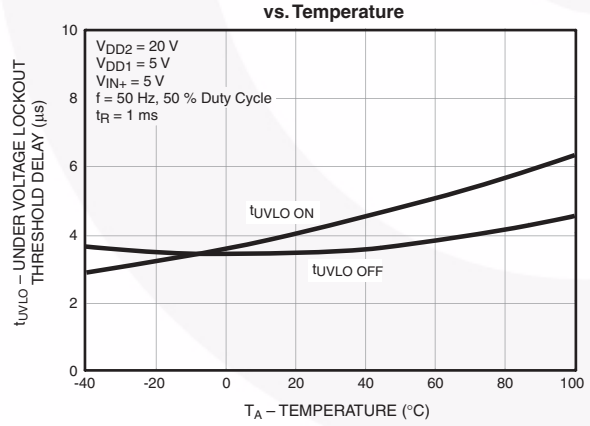
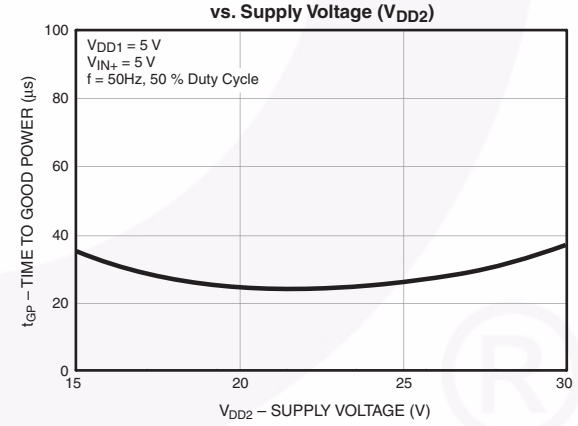


Figure 30. Time to Good Power (t_{GP}) vs. Supply Voltage (V_{DD2})



Typical Performance Characteristics (Continued)

Figure 31. Time to Good Power (t_{GP}) vs. Temperature

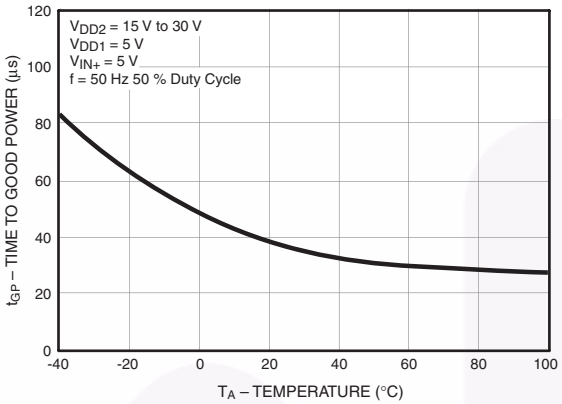


Figure 32. Clamp Low Level Sinking Current (I_{CLAMPL}) vs. Temperature

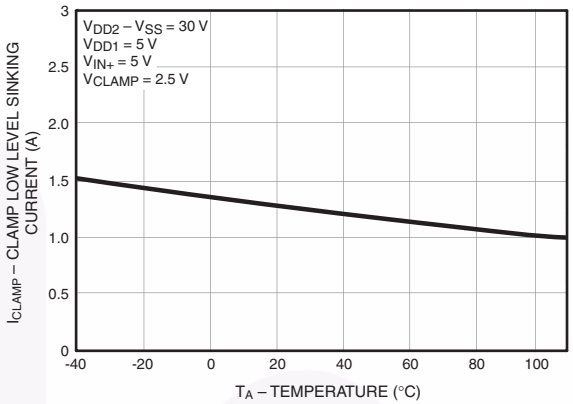


Figure 33. Clamping Threshold Voltage (V_{CLAMP}) vs. Temperature

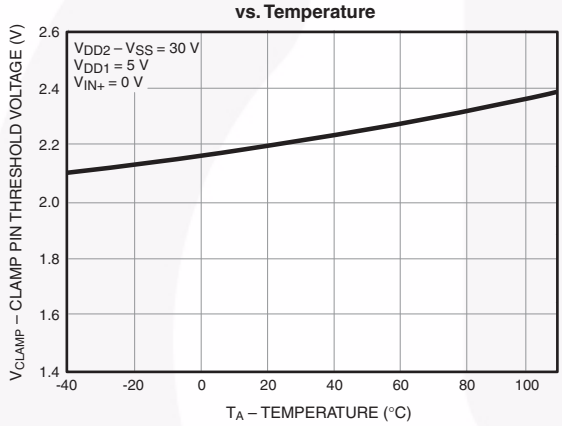
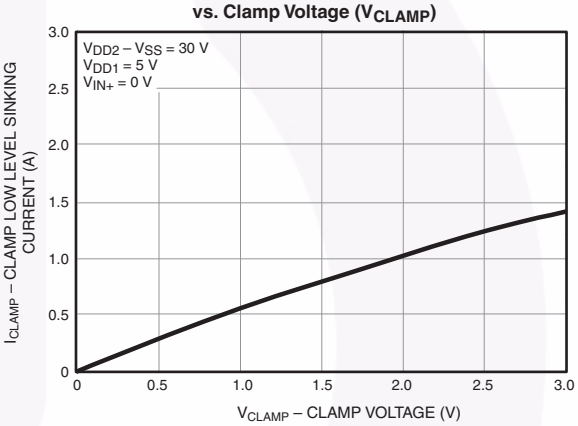
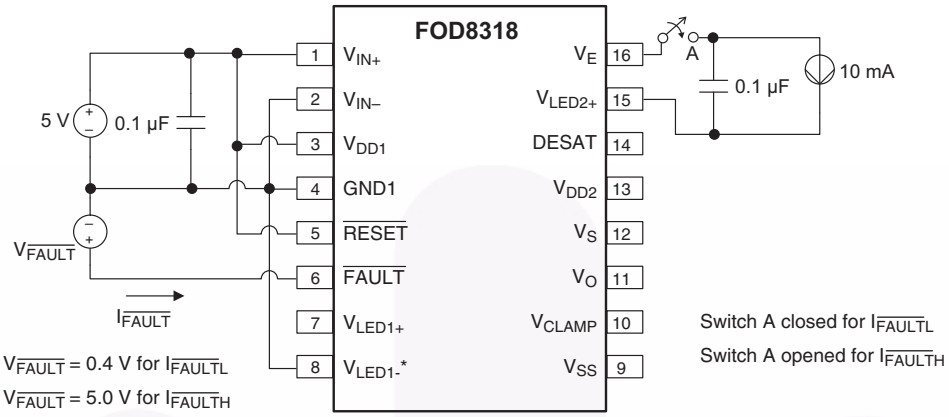


Figure 34. Clamp Low Level Sinking Current (I_{CLAMPL}) vs. Clamp Voltage (V_{CLAMP})

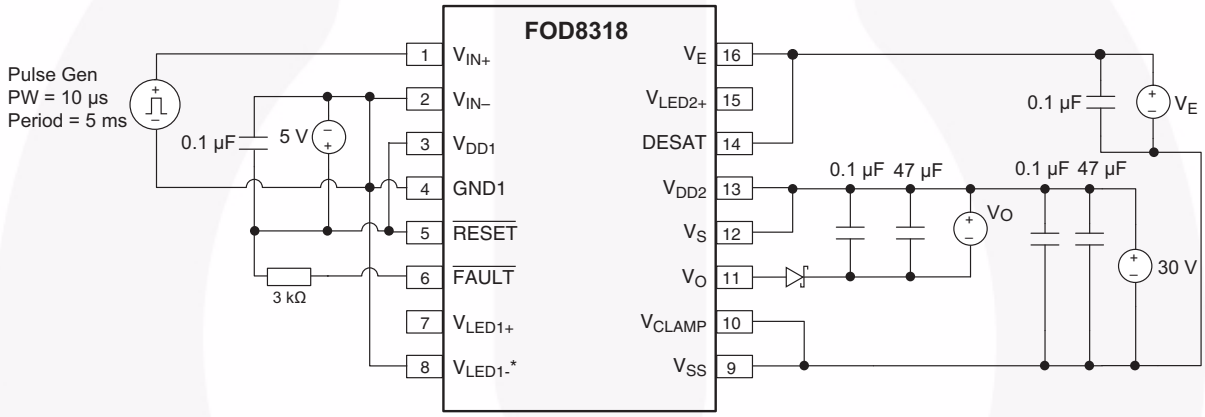


Test Circuits



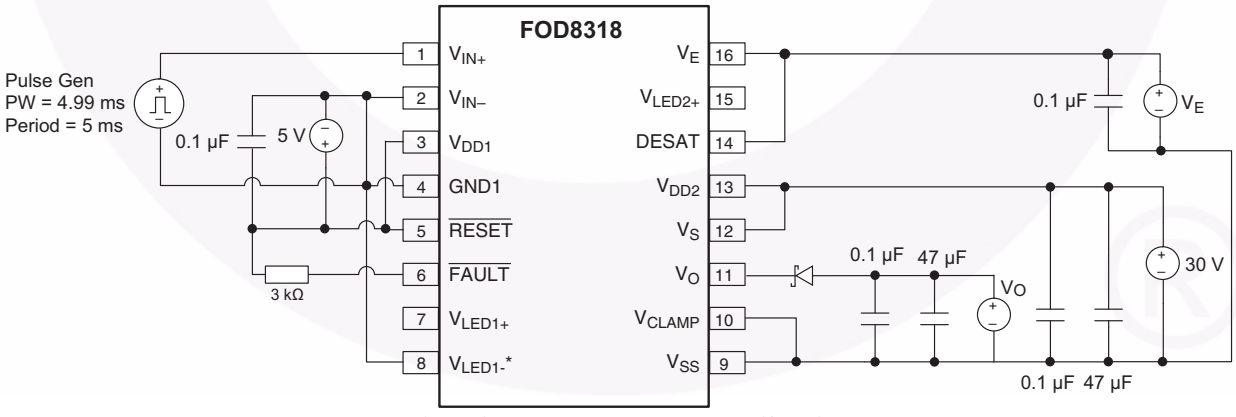
*Pin 8 (V_{LED1-}) is internally connected to pin 4 (GND1).

Figure 35. Fault Output Current ($I_{\overline{FAULTL}}$) and ($I_{\overline{FAULTH}}$) Test Circuit



*Pin 8 (V_{LED1-}) is internally connected to pin 4 (GND1).

Figure 36. High Level Output Current (I_{OH}) Test Circuit



*Pin 8 (V_{LED1-}) is internally connected to pin 4 (GND1).

Figure 37. Low Level Output Current (I_{OL}) Test Circuit

Test Circuits (Continued)

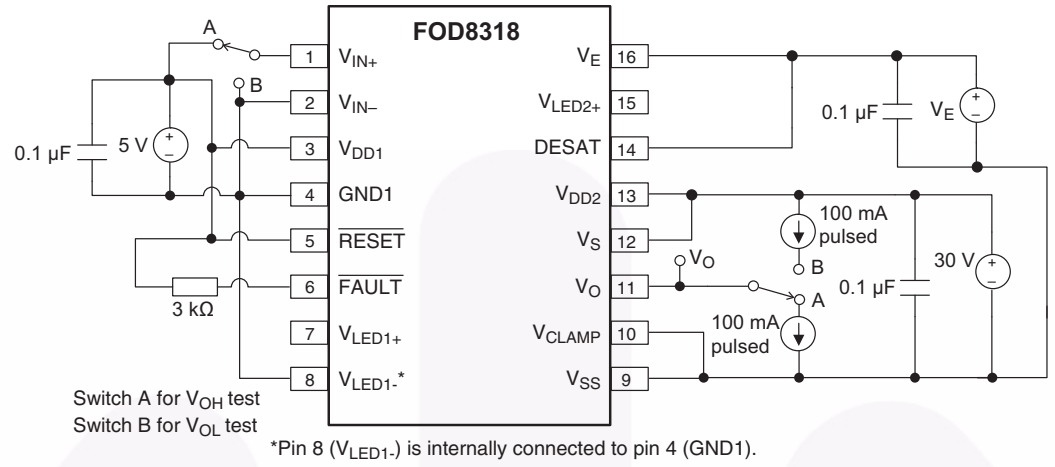


Figure 38. High Level (V_{OH}) and Low Level (V_{OL}) Output Voltage Test Circuit

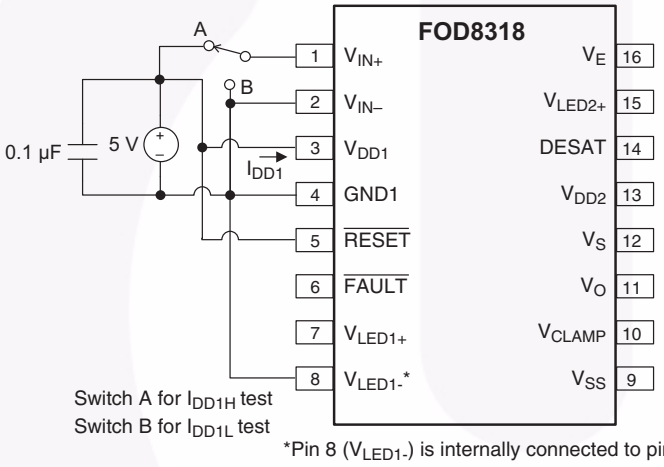


Figure 39. High Level (I_{DD1H}) and Low Level (I_{DD1L}) Supply Current Test Circuit

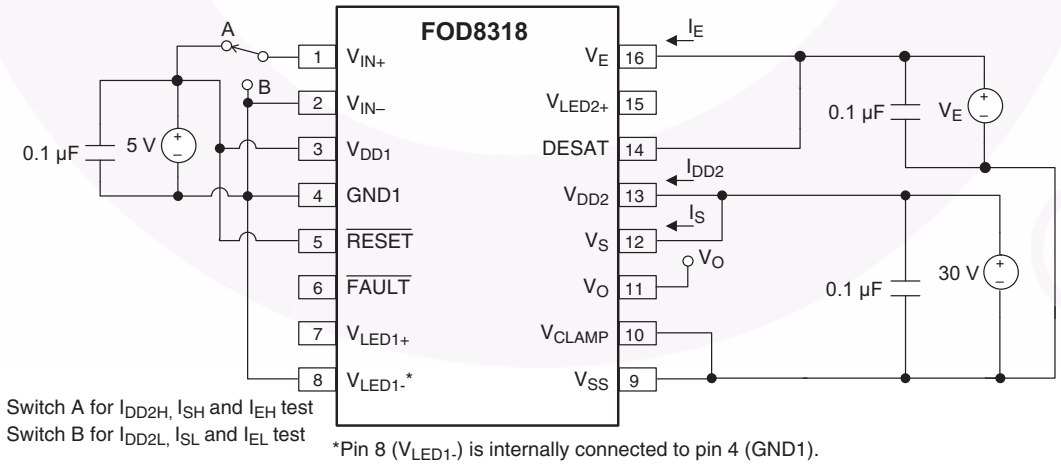
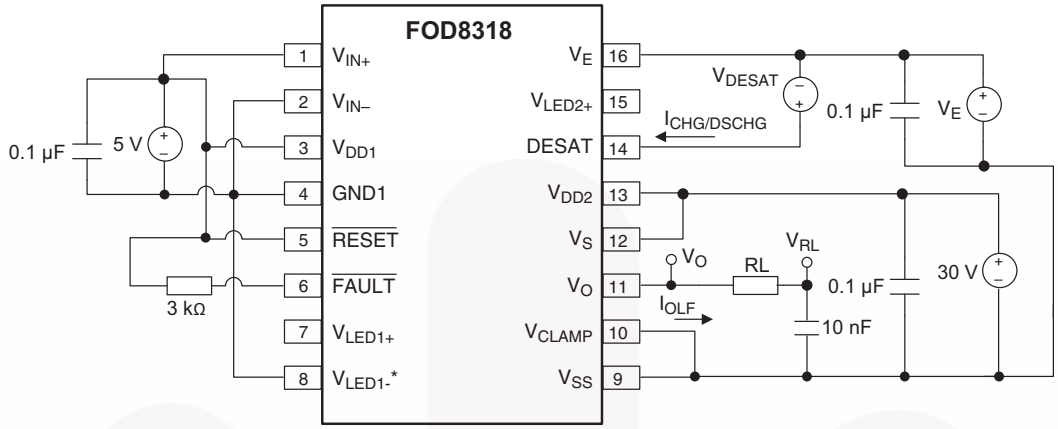


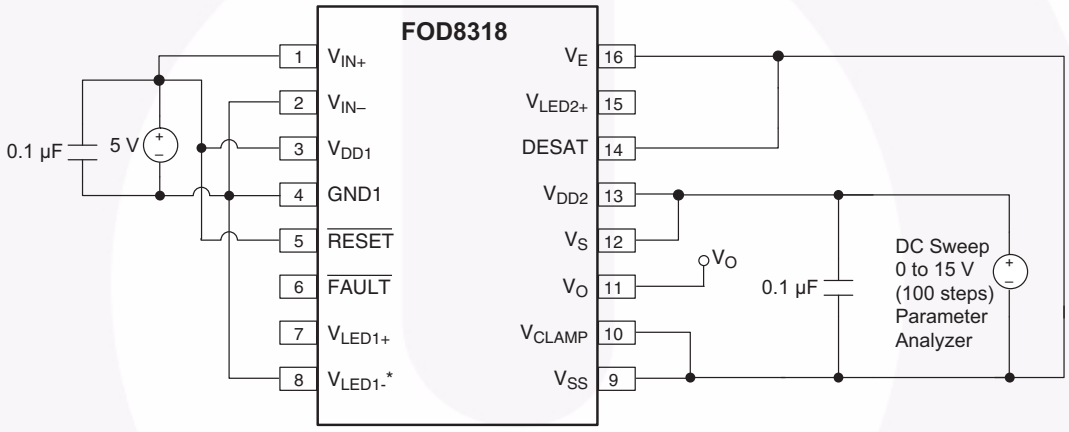
Figure 40. High Level (I_{DD2H}), Low Level (I_{DD2L}) Output Supply Current, High Level (I_{SH}), Low Level (I_{SL}) Source Current, V_E High Level (I_{EH}), and V_E Low Level (I_{EL}) Supply Current Test Circuit

Test Circuits (Continued)



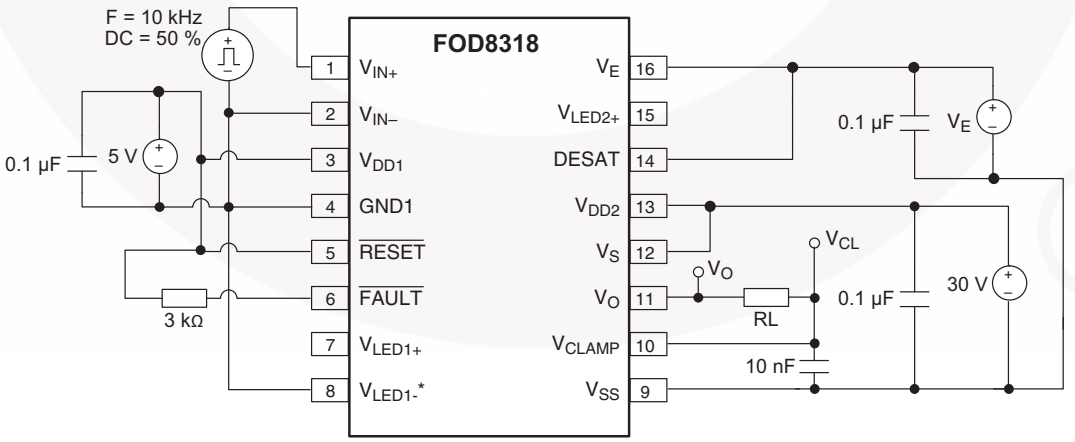
*Pin 8 (V_{LED1-}) is internally connected to pin 4 (GND1).

Figure 41. Low Level Output Current During Fault Conditions (I_{OLF}), Blanking Capacitor Charge Current (I_{CHG}), Blanking Capacitor Discharging Current (I_{DSCHG}), and DESAT Threshold (V_{DESAT}) Test Circuit



*Pin 8 (V_{LED1-}) is internally connected to pin 4 (GND1).

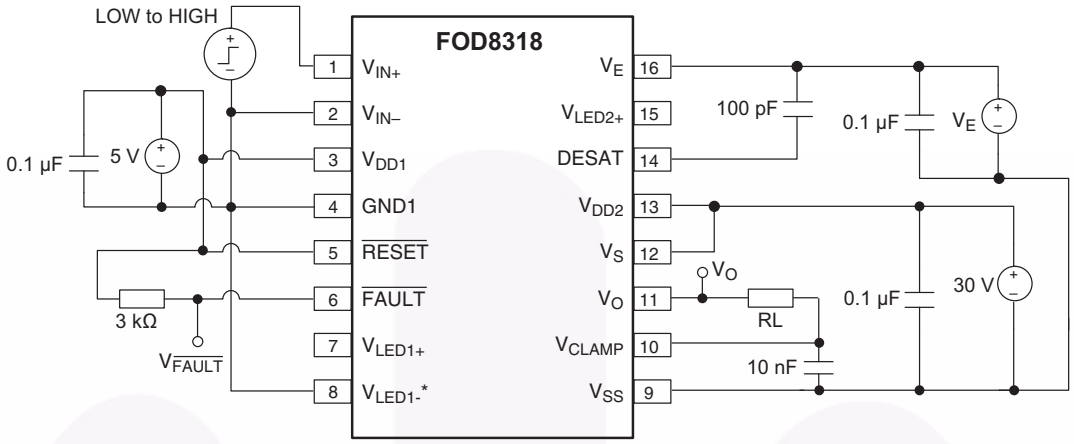
Figure 42. Under-Voltage Lockout Threshold (V_{UVLO}) Test Circuit



*Pin 8 (V_{LED1-}) is internally connected to pin 4 (GND1).

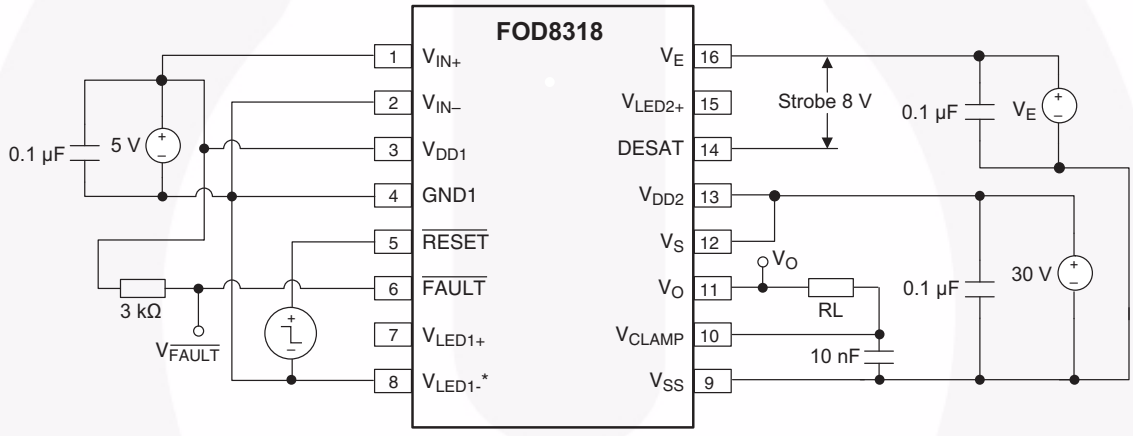
Figure 43. Propagation Delay (t_{PLH}, t_{PHL}), Pulse Width Distortion (PWD), Rise Time (t_R), and Fall Time (t_F) Test Circuit

Test Circuits (Continued)



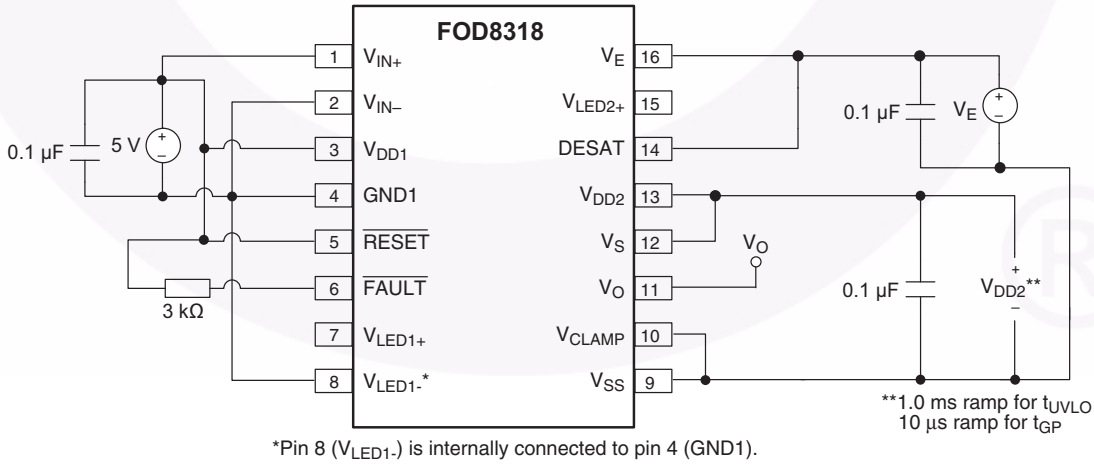
*Pin 8 (V_{LED1-}) is internally connected to pin 4 (GND1).

Figure 44. DESAT Sense ($t_{DESAT(90\ \%)}$, $t_{DESAT(10\ \%)}$), DESAT Fault ($t_{DESAT(\overline{FAULT})}$), and ($t_{DESAT(LOW)}$) Test Circuit



*Pin 8 (V_{LED1-}) is internally connected to pin 4 (GND1).

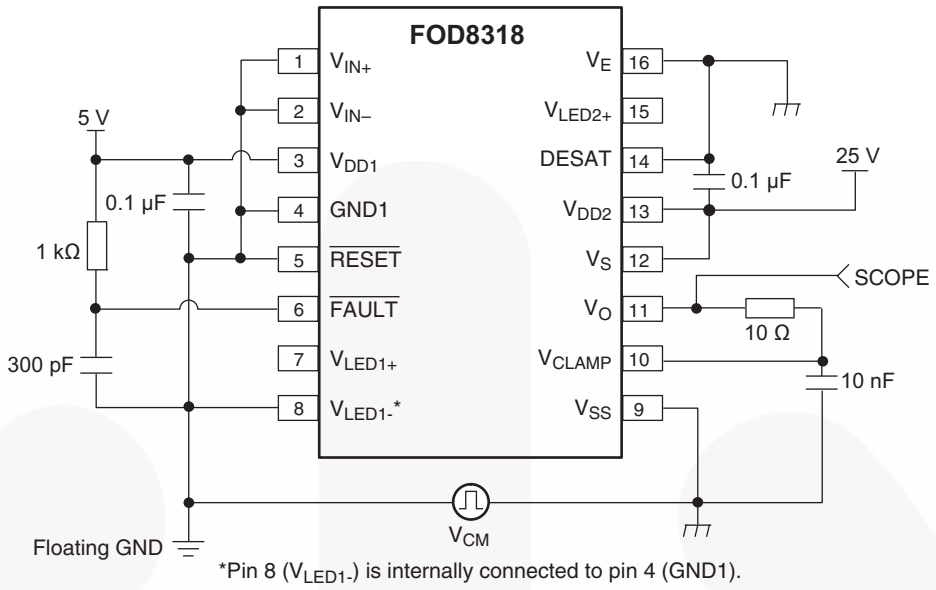
Figure 45. Reset Delay ($t_{\overline{RESET}(\overline{FAULT})}$) Test Circuit



*Pin 8 (V_{LED1-}) is internally connected to pin 4 (GND1).

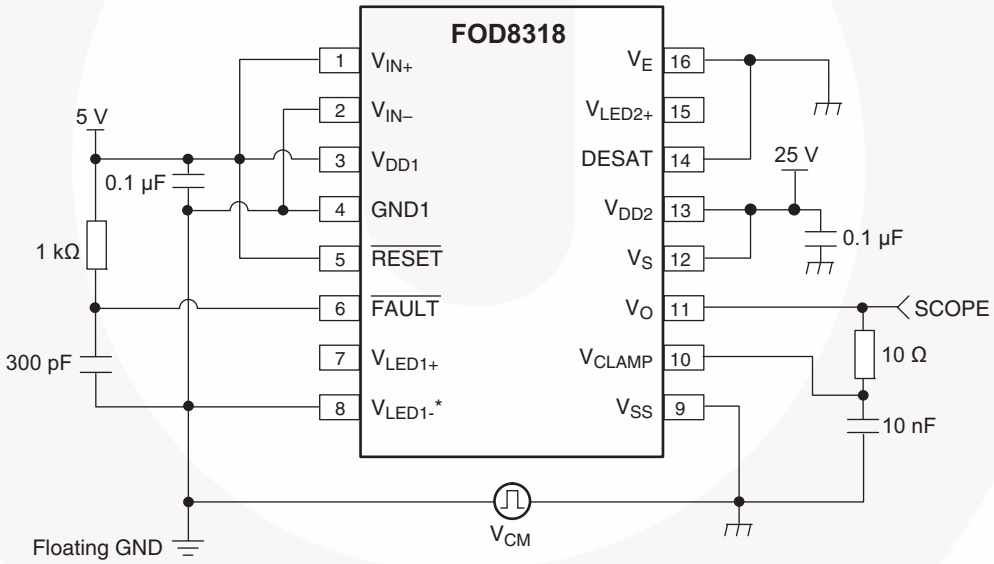
Figure 46. Under-Voltage Lockout Delay (t_{UVLO}) and Time to Good Power (t_{GP}) Test Circuit

Test Circuits (Continued)



*Pin 8 (V_{LED1-}) is internally connected to pin 4 (GND1).

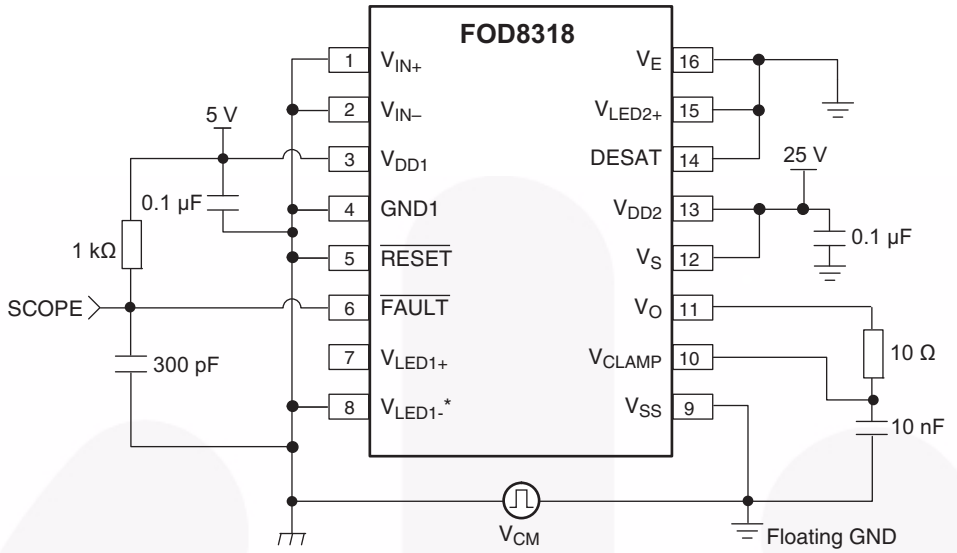
Figure 47. Common Mode Low (CM_L) Test Circuit at LED1 Off



*Pin 8 (V_{LED1-}) is internally connected to pin 4 (GND1).

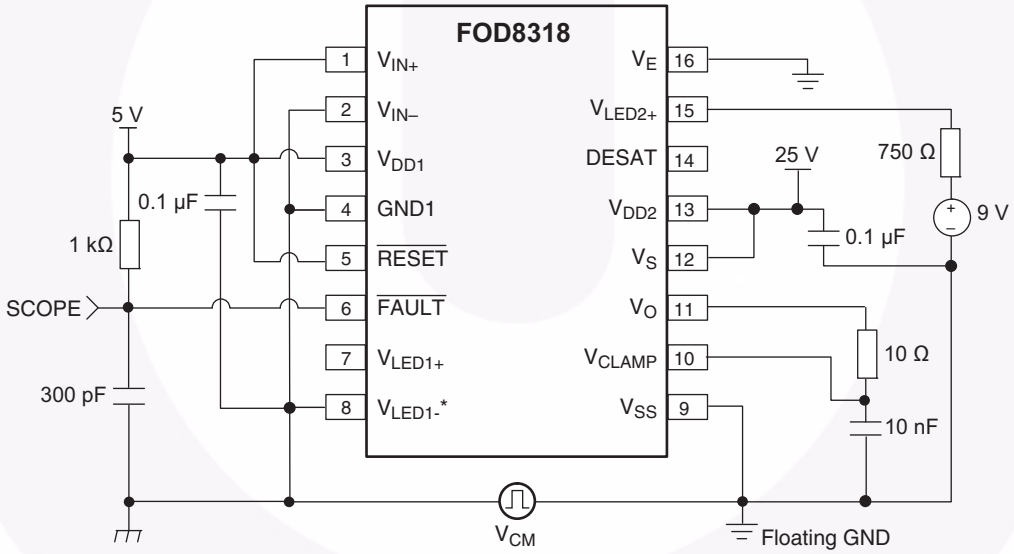
Figure 48. Common Mode High (CM_H) Test Circuit at LED1 On

Test Circuits (Continued)



*Pin 8 (V_{LED1-}) is internally connected to pin 4 (GND1).

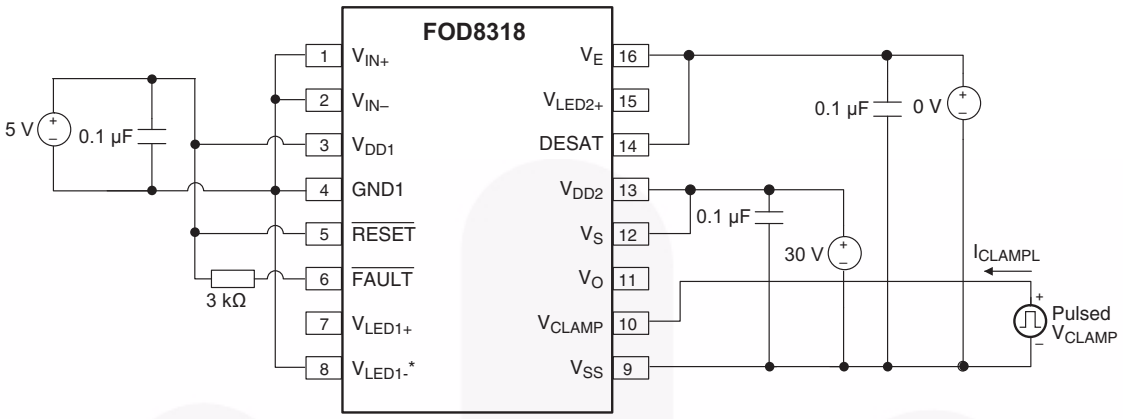
Figure 49. Common Mode High (CM_H) Test Circuit at LED2 Off



*Pin 8 (V_{LED1-}) is internally connected to pin 4 (GND1).

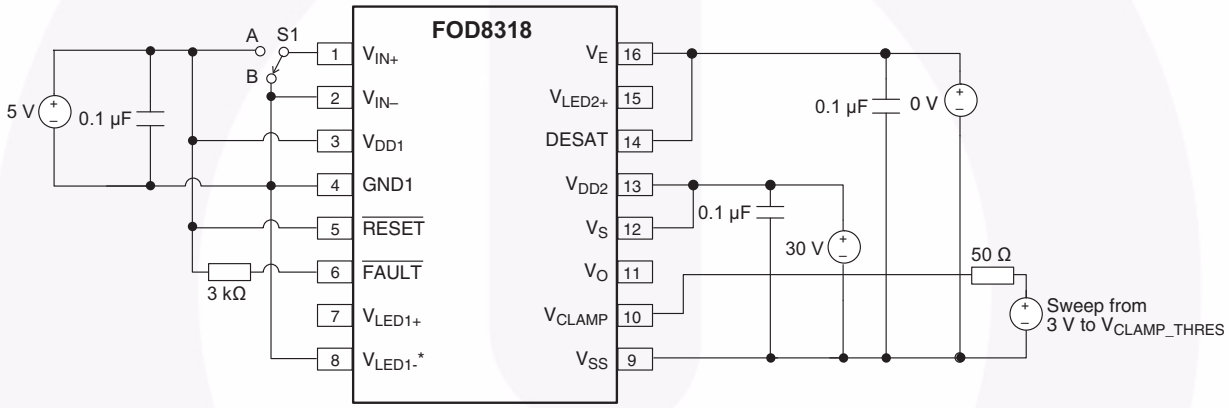
Figure 50. Common Mode Low (CM_L) Test Circuit at LED2 On

Test Circuits (Continued)



*Pin 8 (V_{LED1-}) is internally connected to pin 4 (GND1).

Figure 51. Clamp Low Level Sinking Current (I_{CLAMPL})



*Pin 8 (V_{LED1-}) is internally connected to pin 4 (GND1).

Initially set S1 to A before connecting 3 V to clamp pin. Then switch to B before sweeping down to get the V_{CLAMP_THRES}, clamping threshold voltage.

Figure 52. Clamp Pin Threshold Voltage (V_{CLAMP})

Timing Diagrams

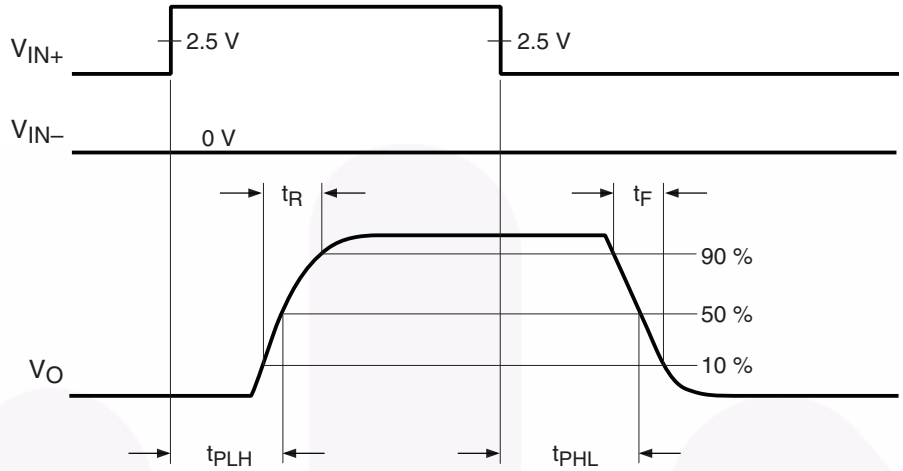


Figure 53. Propagation Delay (t_{PLH}, t_{PHL}), Rise Time (t_R), and Fall Time (t_F) Timing Diagram

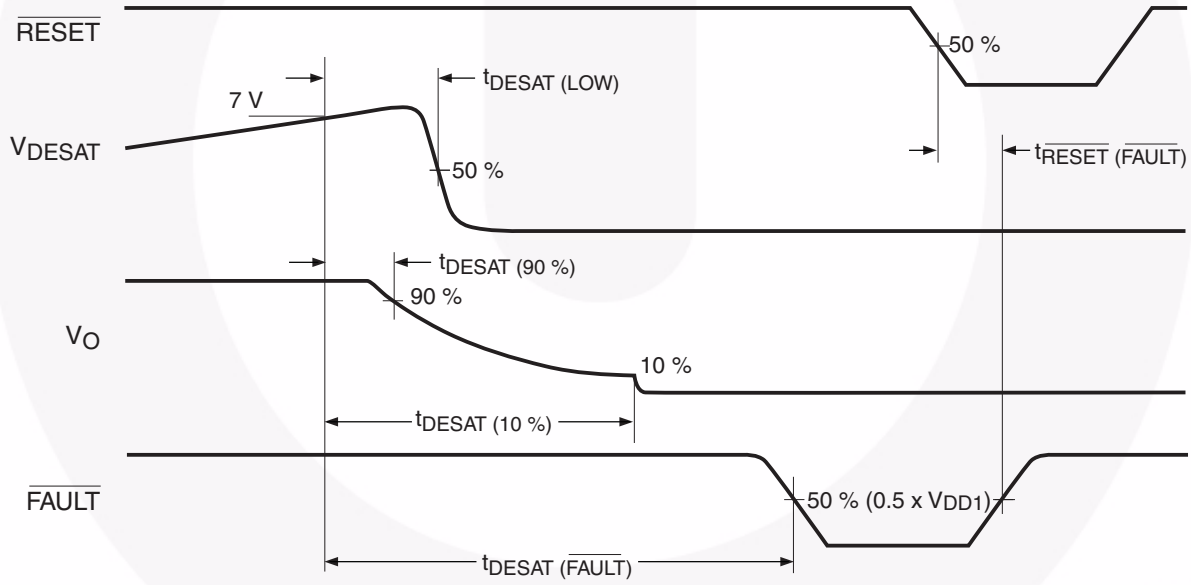


Figure 54. Definitions for Fault Reset Input ($\overline{RESET}$), Desaturation Voltage Input (DESAT), Output Voltage (V_O), and Fault Output ($\overline{FAULT}$) Timing Waveforms

Application Information

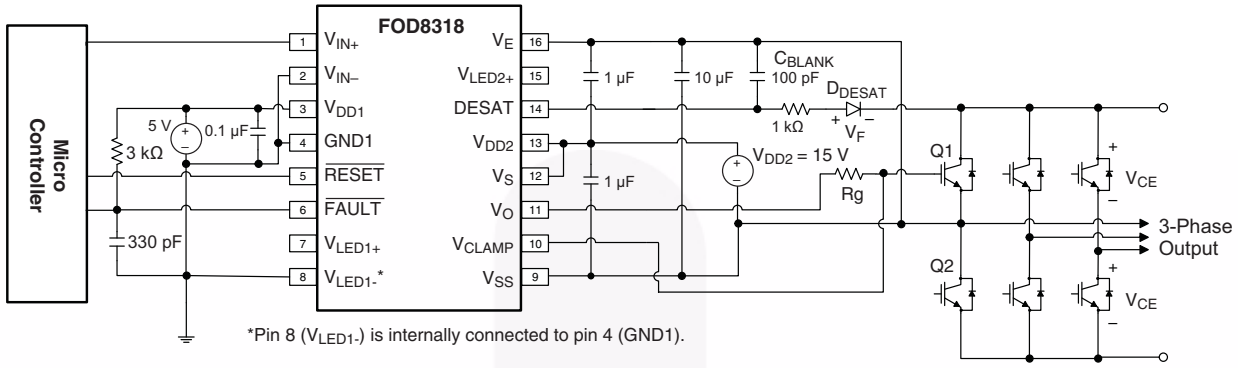


Figure 55. Recommended Application Circuit

Functional Description

The functional behavioral of FOD8318 is illustrated by the detailed internal schematic shown in Figure 56. This explains the interaction and sequence of internal and external signals, together with the timing diagrams.

1. Non-Inverting and Inverting Inputs

There are two CMOS/TTL-compatible inputs, V_{IN+} and V_{IN-}, to control the IGBT in non-inverting and inverting configurations, respectively. When V_{IN-} is set to LOW state, V_{IN+} controls the driver output, V_O, in non-inverting configuration. When V_{IN+} is set to HIGH state, V_{IN-} controls the driver output in inverting configuration.

The relationship between the inputs and output are illustrated in the Figure 57.

During normal operation, when no fault is detected, the $\overline{\text{FAULT}}$ output, which is an open-drain configuration, is latched to HIGH state. This allows the gate driver to be controlled by the input logic signal.

When a fault is detected, the $\overline{\text{FAULT}}$ output is latched to LOW state. This condition remains until the input logic is pulled to LOW and the $\overline{\text{RESET}}$ pin is also pulled LOW for a period longer than $PW_{\overline{\text{RESET}}}$.

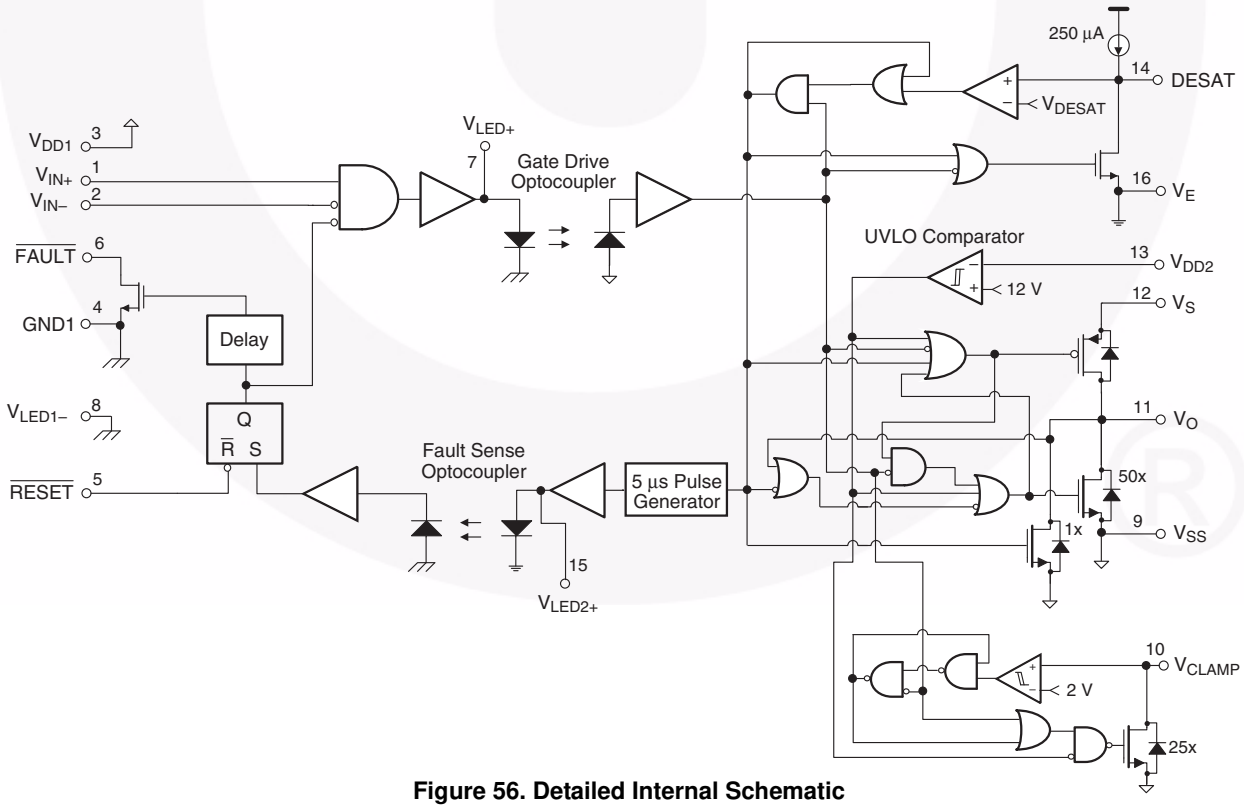


Figure 56. Detailed Internal Schematic