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May 2017

FOD8334
Input LED Drive, 4.0 A Peak Output Current, IGBT Drive Optocoupler with Desaturation Detection, Isolated Fault Sensing, and Active Miller Clamp

Features

- Input LED Drive Facilitates Receiving Digitally Encoded Signals from PWM Output
- Optically Isolated Fault-Sensing Feedback
- Active Miller Clamp to Shut Off IGBT During High dv/dt without Negative Supply Voltage
- High Noise Immunity Characterized by Common Mode Rejection – 35 kV/µs Minimum, V_{CM} = 1500 V_{PEAK}
- 4.0 A Maximum Peak Output Current Driving Capability for Medium Power IGBT
  - P-Channel MOSFETs at Output Stage Enable Output Voltage Swing Close to Supply Rail (Rail-to-Rail Output)
  - Wide Supply Voltage Range: 15 V to 30 V
- Integrated IGBT Protection
  - Desaturation Detection
  - "Soft" IGBT Turn-Off
  - Under-Voltage Lockout (UVLO) with Hysteresis
- Fast Switching Speed Over Full Operating Temperature Range
  - 250 ns Maximum Propagation Delay
  - 100 ns Maximum Pulse Width Distortion
- Extended Industrial Temperature Range:
  - –40°C to 100°C
- Safety and Regulatory Approvals
  - UL1577, 4,243 V_{RMS} for 1 Minute
  - DIN-EN/IEC60747-5-5 (Pending Approvals):
    1,414 V_{PEAK} Working Insulation Voltage Rating
    8,000 V_{PEAK} Transient Isolation Voltage Rating
    8 mm Creepage and Clearance Distance

Applications

- AC and Brushless DC Motor Drive
- Industrial Inverter
- Uninterruptible Power Supply
- Induction Heating
- Isolated IGBT/Power MOSFET Gate Drive

Description

The FOD8334 is an advanced 4.0 A peak output current IGBT drive optocoupler capable of driving medium-power IGBTs with ratings up to 1,200 V and 150 A. It is suited for fast-switching driving of power IGBTs and MOSFETs in motor-control inverter applications and high-performance power systems. The FOD8334 offers protection features necessary for preventing fault conditions that lead to destructive thermal runaway of IGBTs.

The device utilizes Fairchild's proprietary Optoplanar® coplanar packaging technology and optimized IC design to achieve reliable high isolation and high noise immunity, characterized by high common-mode rejection and power supply rejection specifications. The device is housed in a wide-body, 16-pin, small-outline, plastic package.

The gate-driver channel consists of an aluminum gallium arsenide (AlGaAs) light-emitting diode (LED) optically coupled to an integrated high-speed driver circuit with a low-RDS(ON) MOSFET output stage. The fault-sense channel consists of an AlGaAs LED optically coupled to an integrated high-speed feedback circuit for fault sensing.

Related Resources

- *FOD8316—2.5 A Output Current, IGBT Drive Optocoupler with Desaturation, Isolated Fault Sensing*
- *FOD8318—2.5 A Output Current, IGBT Drive Optocoupler with Active Miller Clamp, Desaturation Detection, and Isolated Fault Sensing*
- *FOD8333 – Input LED Drive, 2.5 A Output Current, IGBT Drive Optocoupler with Desaturation Detection, Isolated Fault Sensing, Active Miller Clamp, and Automatic Fault Reset*
- *FOD8332 – Input LED Drive, 2.5 A Output Current, IGBT Drive Optocoupler with Desaturation Detection, Isolated Fault Sensing, Active Miller Clamp*
- *AN-3009—Standard Gate-Driver Optocouplers*
- *www.fairchildsemi.com/search/tree/optoelectronics*

Truth Table

LED	UVLO ($V_{DD} - V_E$)	DESAT Detected?	$\overline{FAULT}$[1]	V_O
X	Active	X	HIGH	LOW
On	Not Active	Yes	LOW	LOW
Off	X	X	HIGH	LOW
On	Not Active	No	HIGH	HIGH

Note:

1. $\overline{FAULT}$ pin is connected to a pull-up resistor.

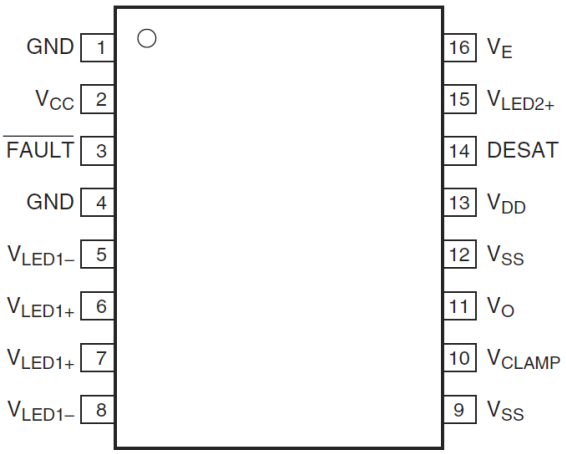
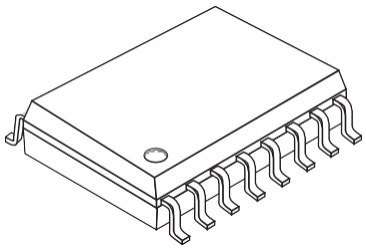


Figure 1. Pin Configuration



Pin Definitions

Pin #	Name	Description
1	GND	Ground for Fault-Sense Optocoupler
2	V_{CC}	Positive Supply Voltage (3 V to 15 V) for Fault Sense Optocoupler
3	$\overline{FAULT}$	Fault-Sense Output
4	GND	Ground for Fault-Sense Optocoupler
5	V_{LED1-}	LED1 Cathode
6	V_{LED1+}	LED1 Anode
7	V_{LED1+}	LED1 Anode
8	V_{LED1-}	LED1 Cathode
9	V_{SS}	Negative Output Supply Voltage
10	V_{CLAMP}	Clamp Supply Voltage
11	V_O	Gate-Drive Output Voltage
12	V_{SS}	Negative Output Supply Voltage
13	V_{DD}	Positive Output Supply Voltage
14	DESAT	Desaturation Voltage Input
15	V_{LED2+}	LED2 Anode (Do not connect. Leave floating.)
16	V_E	Output Supply Voltage/IGBT Emitter

Block Diagram

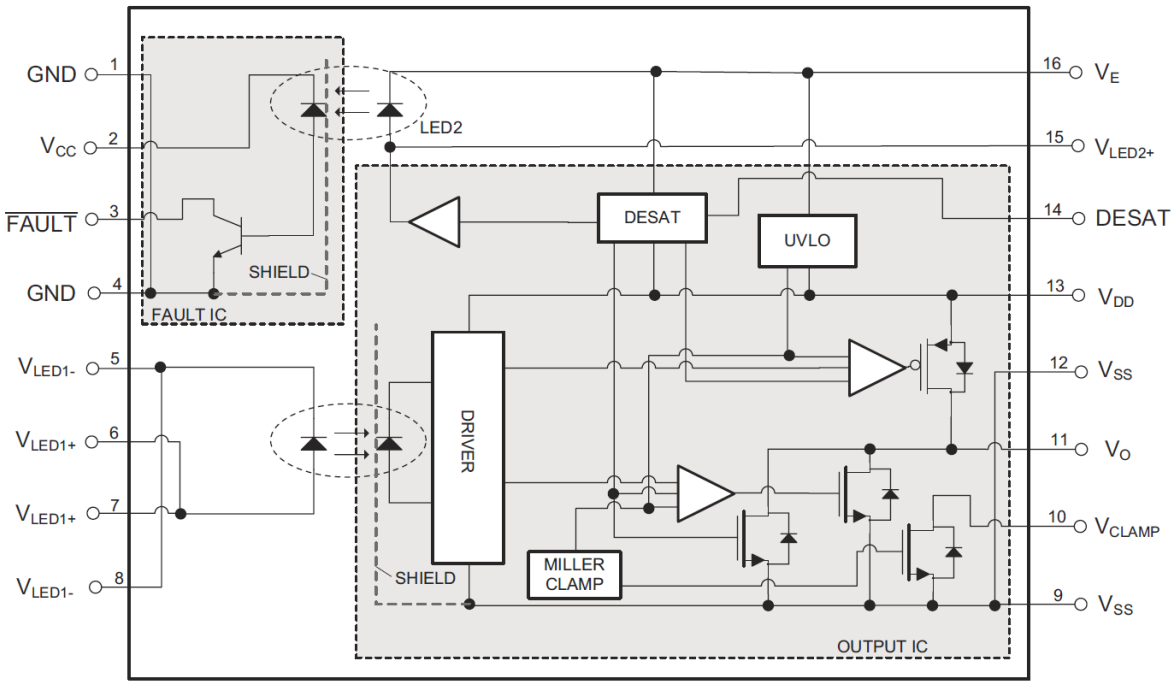


Figure 2. Functional Block Diagram

Safety and Insulation Ratings

As per DIN EN/IEC 60747-5-5, this optocoupler is suitable for “safe electrical insulation” only within the safety limit data. Compliance with the safety ratings must be ensured by means of protective circuits.

Parameter		Characteristics
Installation Classifications per DIN VDE 0110/1.89 Table 1 Rated Mains Voltage	< 150 V_{RMS}	I–IV
	< 300 V_{RMS}	I–IV
	< 450 V_{RMS}	I–IV
	< 600 V_{RMS}	I–IV
	< 1000 V_{RMS}	I–III
Climatic Classification		40/100/21
Pollution Degree (DIN VDE 0110/1.89)		2

Symbol	Parameter	Min.	Typ.	Max.	Unit
CTI	Comparative Tracking Index (DIN IEC 112/VDE 0303 Part 1)	175			
V_{PR}	Input-to-Output Test Voltage, Method b, V_{IORM} x 1.875 = V_{PR}, 100% Production Test with t_m = 1 s, Partial Discharge < 5 pC	2651			V_{peak}
	Input-to-Output Test Voltage, Method a, V_{IORM} x 1.6 = V_{PR}, Type and Sample Test with t_m = 10 s, Partial Discharge < 5 pC	2262			V_{peak}
V_{IORM}	Maximum Working Insulation Voltage	1414			V_{peak}
V_{IOTM}	Highest Allowable Over Voltage	8000			V_{peak}
	External Creepage	8.0			mm
	External Clearance	8.0			mm
	Insulation Thickness	0.5			mm
T_{Case}	Safety Limit Values – Maximum Values in Failure; Case Temperature	150			°C
$P_{S,INPUT}$	Safety Limit Values – Maximum Values in Failure; Input Power	100			mW
$P_{S,OUTPUT}$	Safety Limit Values – Maximum Values in Failure; Output Power	600			mW
R_{IO}	Insulation Resistance at TS, VIO = 500 V	10^9			Ω

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. T_A = 25ºC unless otherwise specified.

Symbol	Parameter	Value	Units
T_{STG}	Storage Temperature	-40 to +125	ºC
T_{OPR}	Operating Temperature	-40 to +100	ºC
T_J	Junction Temperature	-40 to +125	ºC
T_{SOL}	Lead Solder Temperature (not certified for wave immersion) *Refer to reflow temperature profile on page 31*	260 for 10 s	ºC
PD_I	Input Power Dissipation(2)(3)	45	mW
PD_O	Output Power Dissipation(3)(4)	600	mW
Gate Drive Channel			
$I_{F(AVG)}$	Average Input Current	25	mA
$I_{F(PEAK)}$	Peak Transient Forward Current (Pulse Width < 1 µs)	1.0	A
$I_{OH(PEAK)}$	Peak Output High Current(5)	4.0	A
$I_{OL(PEAK)}$	Peak Output Low Current(5)	4.0	A
V_R	Reverse Input Voltage	5.0	V
$V_E - V_{SS}$	Negative Output Supply Voltage(6)	-0.5 to 15	V
V_{DD} – VE	Positive Output Supply Voltage	-0.5 to 35 – ($V_E - V_{SS}$)	V
$V_{O(PEAK)} - V_{SS}$	Gate Drive Output Voltage	-0.5 to 35	V
$V_{DD} - V_{SS}$	Output Supply Voltage	-0.5 to 35	V
V_{DESAT}	Desaturation Voltage	V_E to V_E + 25	V
I_{DESAT}	Desaturation Current	60	mA
$V_{CLAMP} - V_{SS}$	Active Miller Clamping Voltage	-0.5 to 35	V
I_{CLAMP}	Peaking Clamping Sinking Current	1.7	A
$t_{R(IN)}$, $t_{F(IN)}$	Input Signal Rise and Fall Time	500	ns
Fault Sense Channel			
V_{CC}	Positive Input Supply Voltage	-0.5 to 20	V
$V_{\overline{FAULT}}$	FAULT Output Voltage	-0.5 to 20	V
$I_{\overline{FAULT}}$	FAULT Output Current	16.0	mA

Notes:

2. No derating required across temperature range.
3. Functional operation under these conditions is not implied. Permanent damage may occur if the device is subjected to conditions outside these ratings.
4. Derate linearly above 25°C, free air temperature at a rate of 6.2 mW/°C.
5. Maximum pulse width = 10 µs.
6. This negative output supply voltage is optional. It is only needed when negative gate drive is implemented.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
T_A	Ambient Operating Temperature	-40	+100	ºC
$I_{F(ON)}$	Input Current (ON)	7	16	mA
$V_{F(OFF)}$	Input Voltage (OFF)	-3.6	0.8	V
V_{CC}	Supply Voltage	3	15	V
$V_{DD} – V_{SS}$	Total Output Supply Voltage	15	30	V
$V_{DD} – V_E$	Positive Output Supply Voltage(7)	15	$30 – (V_E – V_{SS})$	V
$V_E – V_{SS}$	Negative Output Supply Voltage	0	15	V
t_{PW}	Input Pulse Width	500		ns

Note:

7. During power up or down, ensure that both the input and output supply voltages reach the proper recommended operating voltages to avoid any momentary instability at the output state.

Isolation Characteristics

Apply over all recommended conditions; typical value is measured at T_A = 25ºC.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{ISO}	Input-Output Isolation Voltage	T_A = 25°C, Relative Humidity < 50%, t = 1.0 minute, $I_{I-O} \leq$ 10 µA, 50 Hz(8)(9)(10)	4,243			V_{RMS}
R_{ISO}	Isolation Resistance	V_{I-O} = 500 V(8)		10^{11}		
C_{ISO}	Isolation Capacitance	V_{I-O} = 0 V, Frequency = 1.0 MHz(8)		1		pF

Notes:

8. Device is considered a two-terminal device: pins 1 to 8 are shorted together and pins 9 to 16 are shorted together.
9. 4,243 V_{RMS} for 1-minute duration is equivalent to 5,091 V_{RMS} for 1-second duration.
10. The input-output isolation voltage is a dielectric voltage rating per UL1577. It should not be regarded as an input-output continuous voltage rating. For the continuous working voltage rating, refer to equipment-level safety specification or DIN EN/IEC 60747-5-5 Safety and Insulation Ratings Table on page 4.

Electrical Characteristics

Apply over all recommended conditions; typical value is measured at V_{CC} = 5 V, V_{DD} – V_{SS} = 30 V, V_E – V_{SS} = 0 V, and T_A = 25°C; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Figure
Gate Drive Channel							
V_F	Input Forward Voltage	I_F = 10 mA	1.10	1.45	1.80	V	5
$\Delta(V_F/T_A)$	Temperature Coefficient of Forward Voltage			-1.5		mV/ºC	
BV_R	Input Reverse Breakdown Voltage	I_R = 10 µA	5			V	
C_{IN}	Input Capacitance	f = 1 MHz, V_F = 0 V		60		pF	
I_{FLH}	Threshold Input Current, Low-to-High	I_O = 0 mA, V_O > 5 V		2.5	7.0	mA	30
V_{FHL}	Threshold Input Voltage, High-to-Low	I_O = 0 mA, V_O < 5 V	0.8			V	31
I_{OH}	High Level Output Current	V_O = V_{DD} – 10 V, I_F = 10mA(11)	-3.0	-4.0		A	6, 10, 32
I_{OL}	Low Level Output Current	V_O = V_{SS} + 10 V, I_F = 0 mA(11)	3.0	4.0		A	7, 11, 33
$R_{DS,OH}$	High Level Output $R_{DS(ON)}$	I_{OH} = -3A(11)	0.5	1.3	3.5	Ω	10
$R_{DS,OL}$	Low Level Output $R_{DS(ON)}$	I_{OL} = 3A(11)	0.5	1.0	3.0	Ω	11
I_{OLF}	Low Level Output Current During Fault Condition	V_O – V_{SS} = 14 V	70	125	170	mA	34
V_{OH}	High Level Output Voltage	I_F = 10 mA, I_O = –100 mA (12)(13)(14)	V_{DD} – 1.0	V_{DD} – 0.2		V	8, 10, 35
V_{OL}	Low Level Output Voltage	I_F = 0 mA, I_O = 100 mA		0.1	0.5	V	9, 11, 36
I_{DDH}	High Level Supply Current	V_O = Open(14), I_O = 0 mA		2.5	5.0	mA	12, 13, 37
I_{DDL}	Low Level Supply Current	V_O = Open, I_O = 0 mA		2.5	5.0	mA	12, 13, 38
I_{EL}	V_E Low Level Supply Current		-0.8	-0.5		mA	38
I_{EH}	V_E High Level Supply Current		-0.50	-0.25		mA	37
I_{CHG}	Blanking Capacitor Charge Current	V_{DESAT} = 2 V(14)(15)	-0.33	-0.25	-0.13	mA	14, 39
I_{DSCHG}	Blanking Capacitor Discharge Current	V_{DESAT} = 7 V	10	40		mA	39
V_{UVLO+}	Under-Voltage Lockout Threshold(13)	I_F = 10 mA, V_O > 5 V	10.8	11.7	12.7	V	40
V_{UVLO-}		I_F = 10 mA, V_O < 5 V	9.8	10.7	11.7	V	
$UVLO_{HYS}$	Under-Voltage Lockout Threshold Hysteresis			1.0		V	
V_{DESAT}	DESAT Threshold(13)	V_{DD} – V_E > $V_{ULVO–}$	6.0	6.5	7.2	V	15, 39
V_{CLAMP_THRES}	Clamping Threshold Voltage			2.0		V	41
I_{CLAMPL}	Clamp Low Level Sinking Current	V_O = V_{SS} + 2.5 V	0.35	1.10		A	16, 42

Electrical Characteristics (Continued)

Apply over all recommended conditions; typical value is measured at V_{CC} = 5 V, V_{DD} – V_{SS} = 30 V, V_E – V_{SS} = 0 V, and T_A = 25°C; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Figure
Fault Feedback Channel							
I_{CCH}	$\overline{FAULT}$ High Level Supply Current	I_{F2} = 0 mA, $V_{\overline{FAULT}}$ = Open, V_{CC} = 15 V		0.0004	2	µA	43
I_{CCL}	$\overline{FAULT}$ Low Level Supply Current	I_{F2} = 16 mA, $V_{\overline{FAULT}}$ = Open, V_{CC} = 15 V		150	200	µA	44
$I_{\overline{FAULTH}}$	$\overline{FAULT}$ Logic High Output Current	$V_{\overline{FAULT}}$ = V_{CC} = 5.5 V		0.02	0.50	µA	45
$I_{\overline{FAULTL}}$	$\overline{FAULT}$ Logic Low Output Current	$V_{\overline{FAULT}}$ = 0.4 V, V_{CC} = 5.5 V	1.1			mA	17, 46

Notes:

11. Maximum pulse width = 10 µs
12. V_{OH} is measured with the DC load current in this testing (maximum pulse width = 1 ms, maximum duty cycle = 20%). When driving capacitive loads, V_{OH} approaches V_{DD} as I_{OH} approaches zero units.
13. Positive output supply voltage (V_{DD} – V_E) should be at least 15 V to ensure adequate margin in excess of the maximum under-voltage lockout threshold, V_{UVLO+}, of 12.7 V.
14. When V_{DD} – V_E > V_{UVLO} and the output state V_O is allowed to go HIGH, the DESAT-detection feature is active and provides the primary source of IGBT protection. UVLO is needed to ensure DESAT detection is functional.
15. The blanking time, t_{BLANK}, is adjustable by an external capacitor (C_{BLANK}), where $t_{BLANK} = C_{BLANK} \times (V_{DESAT} / I_{CHG})$.

Switching Characteristics

Apply over all recommended conditions; typical value is measured at V_{CC} = 5 V, V_{DD} – V_{SS} = 30 V, V_E – V_{SS} = 0 V, and T_A = 25°C; unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ	Max	Units	Figure
t_{PHL}	Propagation Delay to Logic Low Output(17)	Rg = 10 Ω, Cg =10 nF, f = 10 kHz, Duty Cycle = 50%, I_F = 10 mA, V_{DD} – V_{SS} = 30 V(16)	100	135	250	ns	18, 19, 20, 21, 47
t_{PLH}	Propagation Delay to Logic High Output(18)		100	150	250	ns	
PWD	Pulse Width Distortion, $\lvert t_{PHL} - t_{PLH} \rvert$(19)			15	100	ns	47
PDD Skew	Propagation Delay Difference Between Any Two Parts or Channels, ($t_{PHL} - t_{PLH}$)(20)		-150		150	ns	
t_R	Output Rise Time (10% to 90%)			50		ns	47
t_F	Output Fall Time (90% to 10%)			50		ns	
$t_{DESAT(LOW)}$	DESAT Sense to DESAT Low Propagation Delay(23)	Rg = 10 Ω, Cg = 10 nF, V_{DD} – V_{SS} = 30 V (C_{DESAT} = 100pF, R_F = 4.7 kΩ, V_{CC} = 5.5 V)		0.25		µs	
$t_{DESAT(90\%)}$	DESAT Sense to 90% V_O Delay(21)			0.45	0.70	µs	22, 48
$t_{DESAT(10\%)}$	DESAT Sense to 10% V_O Delay(21)			2.8	4.0	µs	23, 24,25, 48
$t_{DESAT(\overline{FAULT})}$	DESAT Sense to Low Level FAULT Signal Delay(22)			0.5	1.5	µs	26, 48
$t_{RESET(\overline{FAULT})}$	RESET to High Level FAULT Signal Delay(24)		0.5	2.3	4.5	µs	27, 48
$t_{DESAT(MUTE)}$	DESAT Input Mute		10.0	22.0	35.0	µs	48
$t_{UVLO\ ON}$	UVLO Turn-On Delay(25)	V_{DD} = 20 V in 1.0 ms Ramp		4.0		µs	49
$t_{UVLO\ OFF}$	UVLO Turn-Off Delay(26)			4.0		µs	
t_{GP}	Time-to-Good Power(27)	V_{DD} = 0 to 30 V in 10 µs Ramp		2.0		µs	28, 29, 49
$\lvert CM_H \rvert$	Common Mode Transient Immunity at Output High	T_A = 25°C, V_{CC} = 5 V, V_{DD} = 25 V, V_{SS} = Ground, C_F = 15 pF, R_F = 4.7 kΩ, V_{CM} = 1500 V_{PEAK}(28)	35	50		kV/µs	51, 52
$\lvert CM_L \rvert$	Common Mode Transient Immunity at Output Low	T_A = 25°C, V_{CC} = 5 V, V_{DD} = 25 V, V_{SS} = Ground, C_F = 15 pF, R_F = 4.7 kΩ, V_{CM} = 1500 V_{PEAK}(29)	35	50		kV/µs	50, 53

Notes:

16. This load condition approximates the gate load of a 1200 V / 150 A IGBT.
17. Propagation delay t_{PHL} is measured from the 50% level on the falling edge of the input pulse to the 50% level of the falling edge of the V_O signal.
18. Propagation delay t_{PLH} is measured from the 50% level on the rising edge of the input pulse to the 50% level of the rising edge of the V_O signal.
19. PWD is defined as $\lvert t_{PHL} - t_{PLH} \rvert$ for any given device.
20. The difference between t_{PHL} and t_{PLH} between any two parts under same operating conditions with equal loads.
21. The length of time the DESAT threshold must be exceeded before V_O begins to go LOW. This is supply voltage dependent.

22. The time from DESAT threshold is exceeded until the FAULT output goes LOW.
23. The length of time the DESAT threshold must be exceeded before V_O begins to go LOW and the FAULT output begins to go LOW.
24. The length of time from when RESET is initiated (via I_F turn-on) until FAULT output goes HIGH.
25. The UVLO turn-on delay, $t_{UVLO\ ON}$, is measured from the V_{UVLO+} threshold level of the rising edge of the output supply voltage (V_{DD}) to the 5 V level of the rising edge of the V_O signal.
26. The UVLO turn-off delay, $t_{UVLO\ OFF}$, is measured from the V_{UVLO-} threshold level of the falling edge of the output supply voltage (V_{DD}) to the 5 V level of the falling edge of the V_O signal.
27. The time to good power, t_{GP}, is measured from the V_{UVLO+} threshold level of the rising edge of the output supply voltage (V_{DD}) to the 5 V level of the rising edge of the V_O signal.
28. Common-mode transient immunity at output HIGH state is the maximum tolerable negative dVCM/dt on the trailing edge of the common-mode pulse, V_{CM}, to assure the output remains in HIGH state (i.e., $V_O > 15$ V or $V_{FAULT} > 2$ V).
29. Common-mode transient immunity at output LOW state is the maximum positive tolerable dVCM/dt on the leading edge of the common-mode pulse, V_{CM}, to ensure the output remains in LOW state (i.e., $V_O < 1.0$ V or $V_{FAULT} < 0.8$ V).

Timing Diagrams

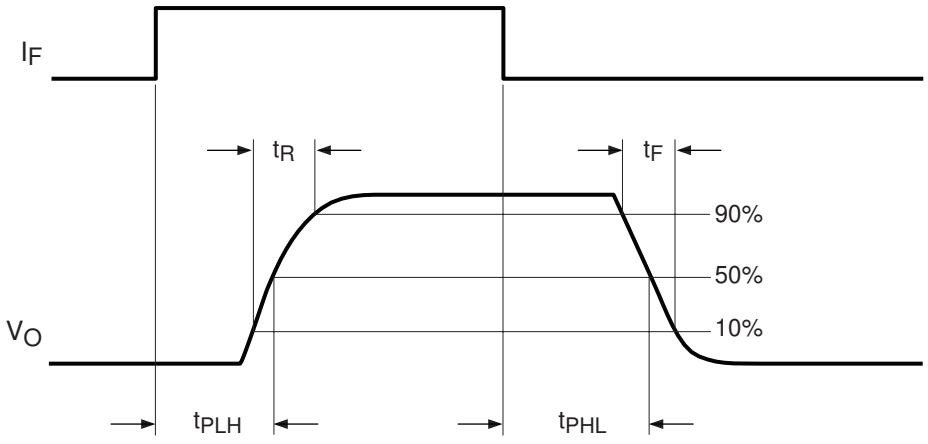


Figure 3. t_{PLH}, t_{PHL}, t_R, and t_F Timing Diagram

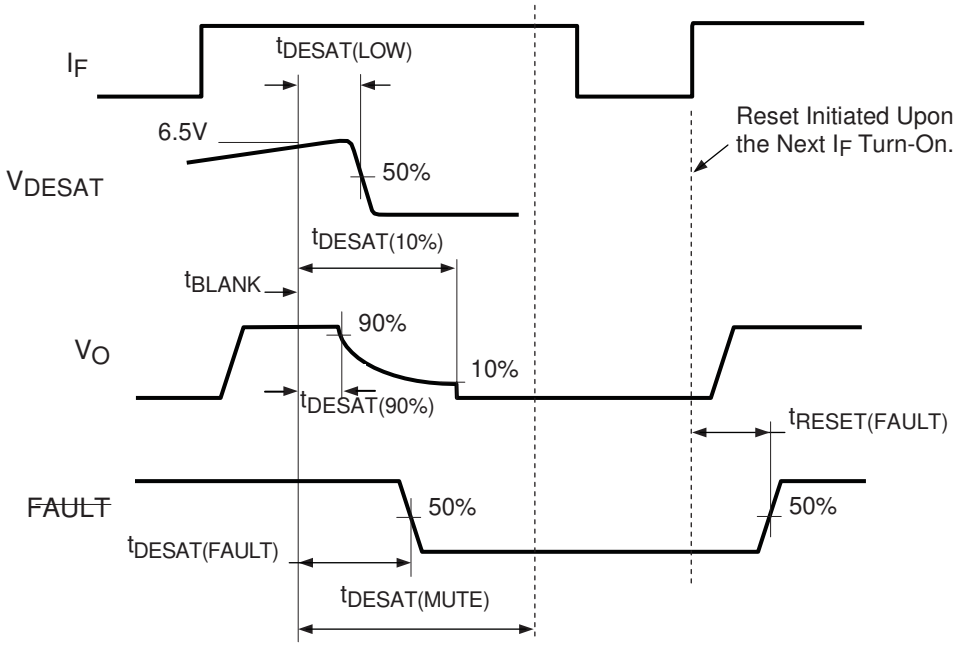


Figure 4. Definitions for DESAT, V_O and $\overline{FAULT}$ Timing Waveforms

Typical Performance Characteristics

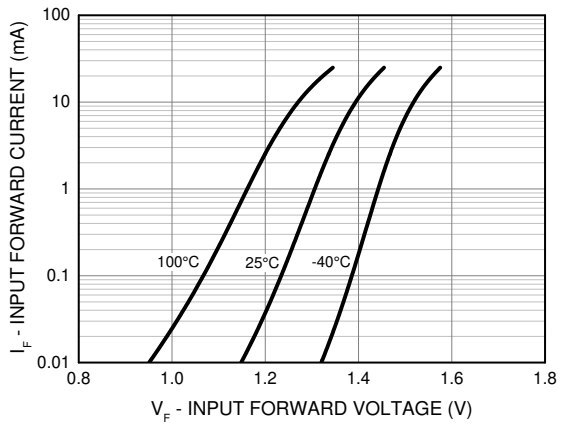


Figure 5. Input Forward Current (I_F) vs. Voltage (V_F)

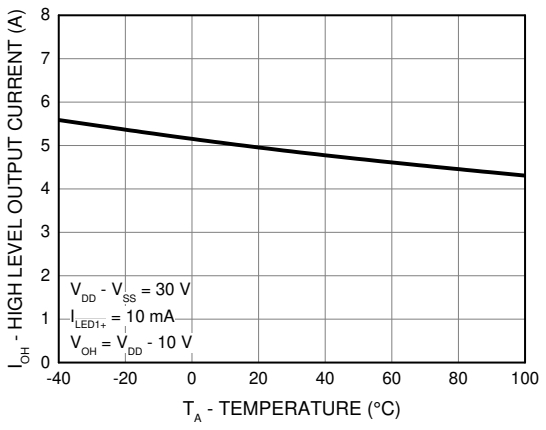


Figure 6. High Level Output Current (I_{OH}) vs. Temperature

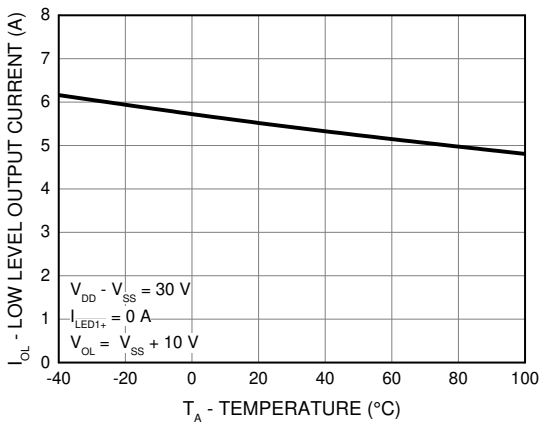


Figure 7. Low Level Output Current (I_{OL}) vs. Temperature

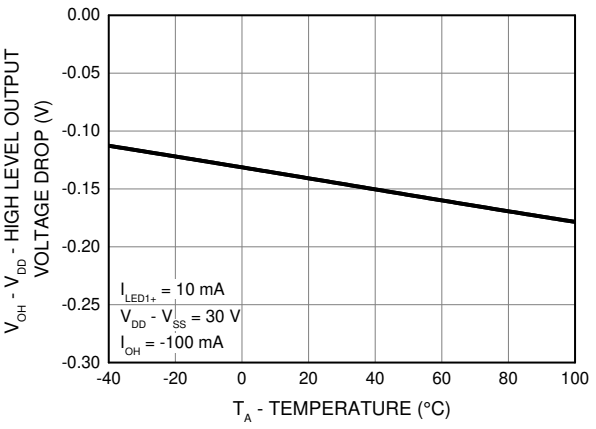


Figure 8. High Level Output Voltage Drop (V_{OH} - V_{DD}) vs. Temperature

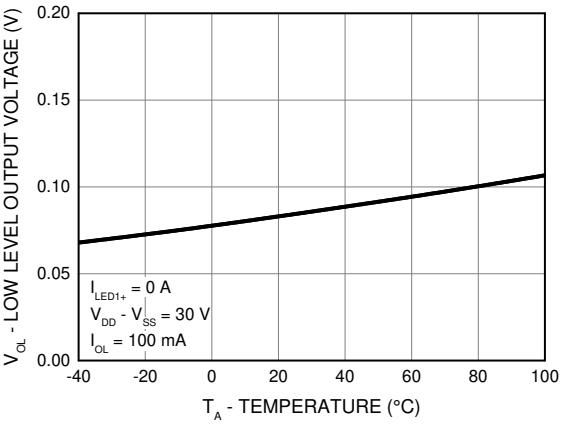


Figure 9. Low Level Output Voltage (V_{OL}) vs. Temperature

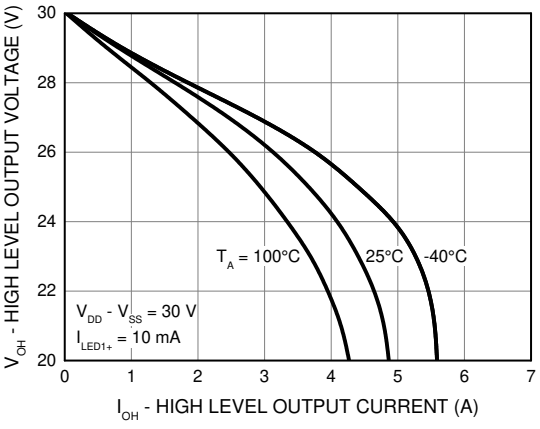


Figure 10. High Level Output Voltage (V_{OH}) vs. High Level Output Current (I_{OH})

Typical Performance Characteristics (Continued)

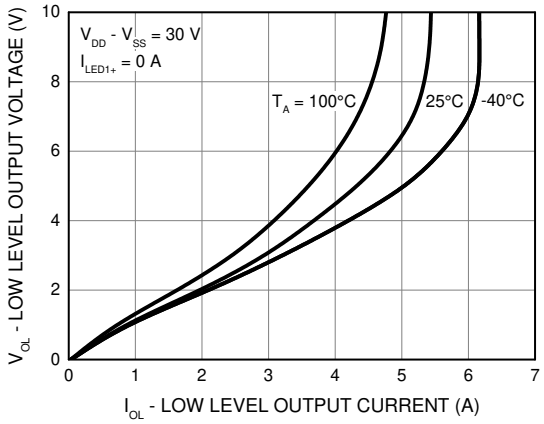


Figure 11. Low Level Output Voltage (V_{OL}) vs. Low Level Output Current (I_{OL})

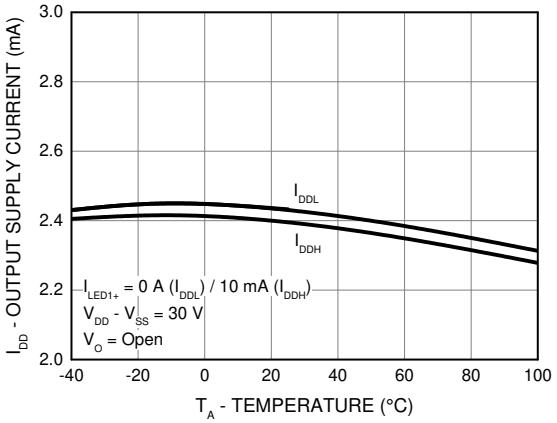


Figure 12. Output Supply Current (I_{DD}) vs. Temperature

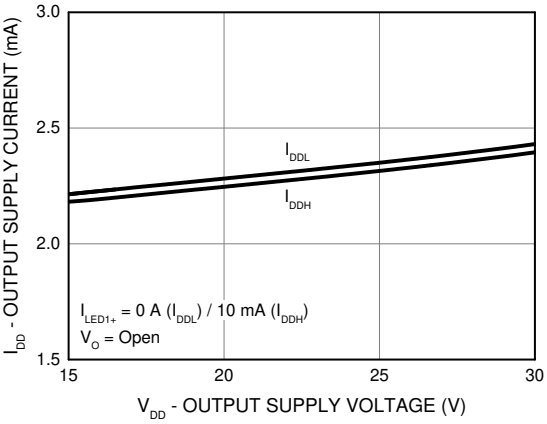


Figure 13. Output Supply Current (I_{DD}) vs. Voltage (V_{DD})

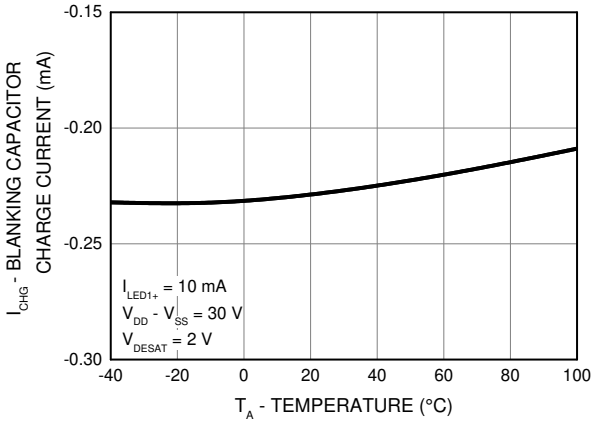


Figure 14. Blanking Capacitor Charge Current (I_{CHG}) vs. Temperature

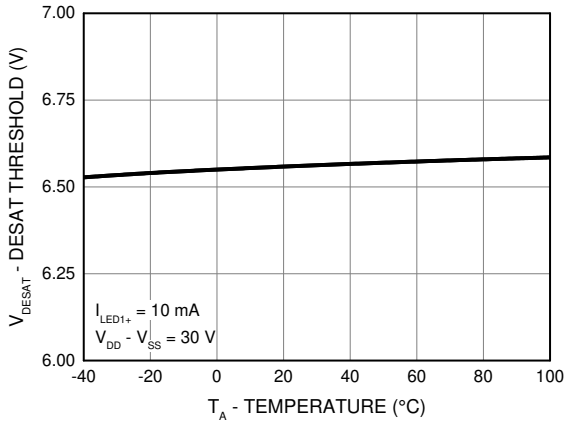


Figure 15. DESAT Threshold (V_{DESAT}) vs. Temperature

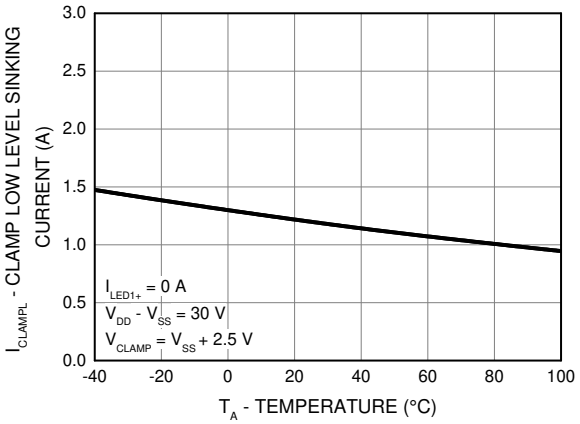


Figure 16. Clamp Low Level Sinking Current (I_{CLAMPL}) vs. Temperature

Typical Performance Characteristics (Continued)

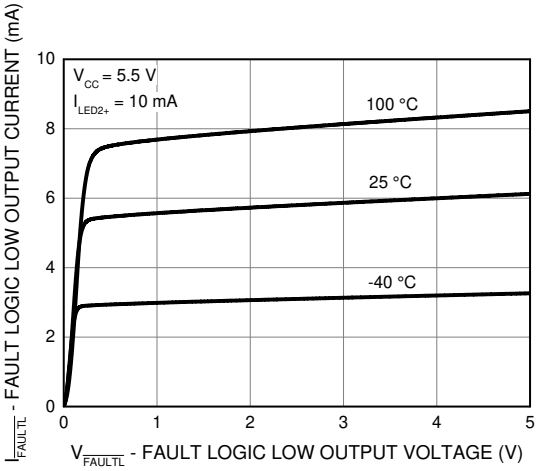


Figure 17. FAULT Logic Low Output Current ($I_{\overline{FAULTL}}$) vs. Voltage ($V_{\overline{FAULTL}}$)

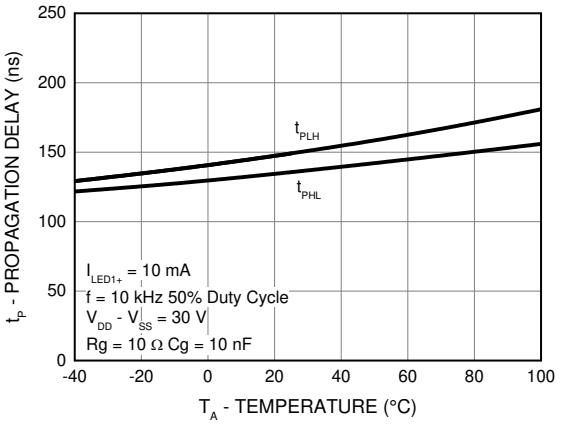


Figure 18. Propagation Delay (t_P) vs. Temperature

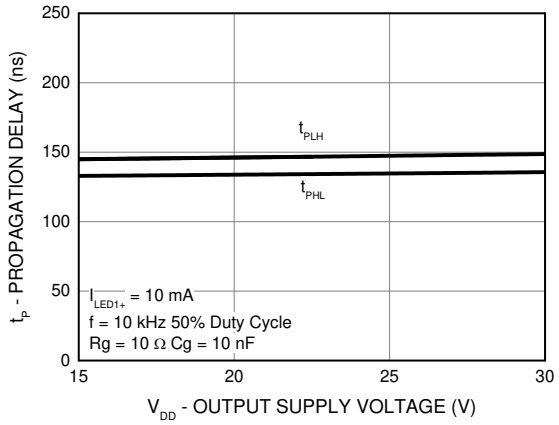


Figure 19. Propagation Delay (t_P) vs. Supply Voltage (V_{DD})

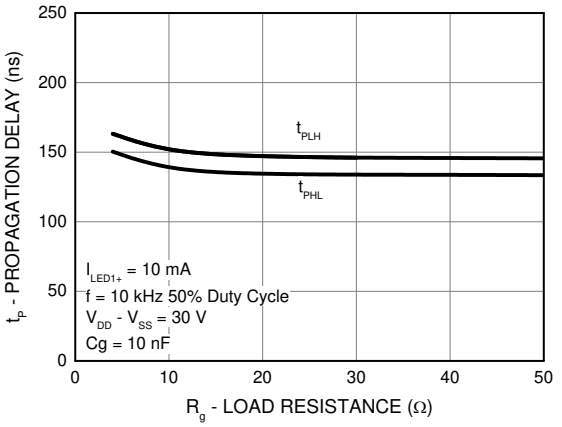


Figure 20. Propagation Delay (t_P) vs. Load Resistance (R_g)

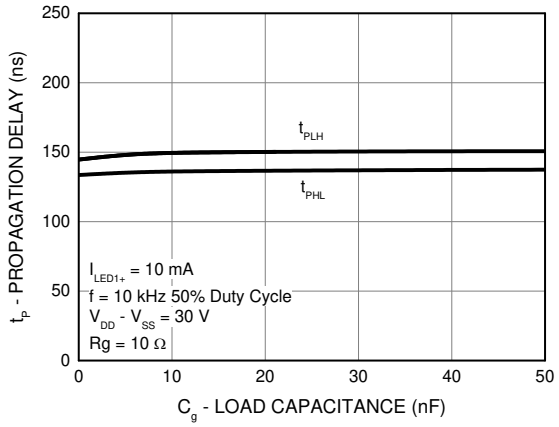


Figure 21. Propagation Delay (t_P) vs. Load Capacitance (C_g)

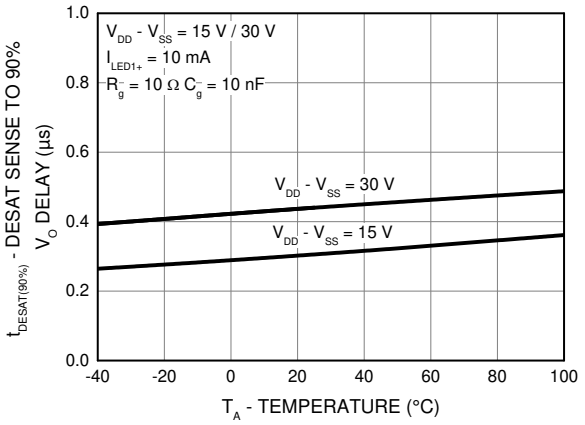


Figure 22. DESAT Sense to 90% V_O Delay ($t_{DESAT(90\%)}$) vs.Temperature

Typical Performance Characteristics (Continued)

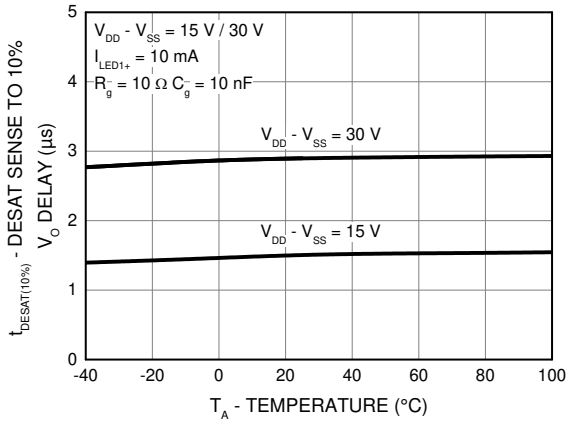


Figure 23. DESAT Sense to 10% V_O Delay ($t_{DESAT(10\%)}$) vs. Temperature

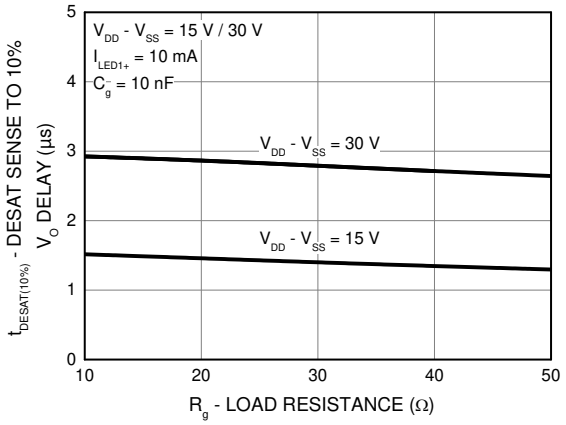


Figure 24. DESAT Sense to 10% V_O Delay ($t_{DESAT(10\%)}$) vs. Load Resistance (R_g)

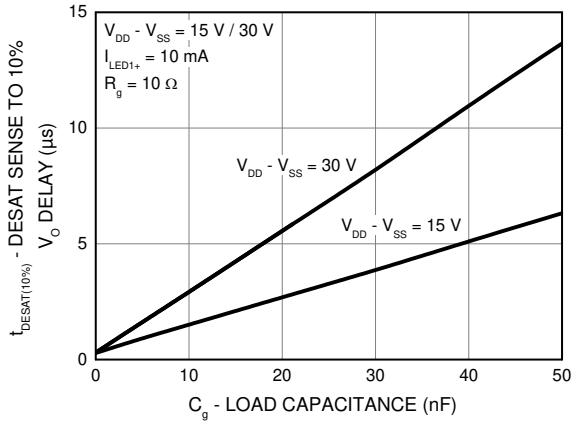


Figure 25. DESAT Sense to 10% V_O Delay ($t_{DESAT(10\%)}$) vs. Load Capacitance (C_g)

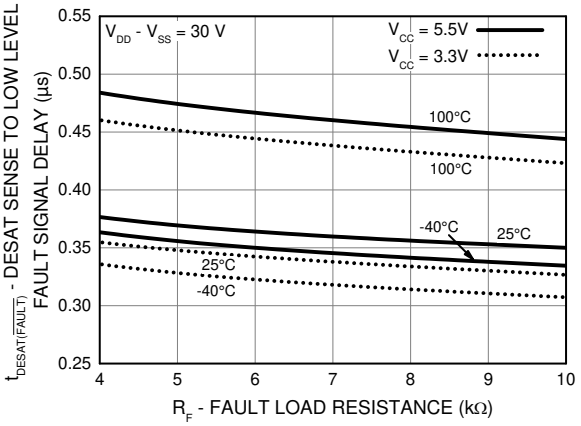


Figure 26. DESAT Sense to Low Level Fault Signal Delay ($t_{DESAT(\overline{FAULT})}$) vs. Fault Load Resistance (R_F)

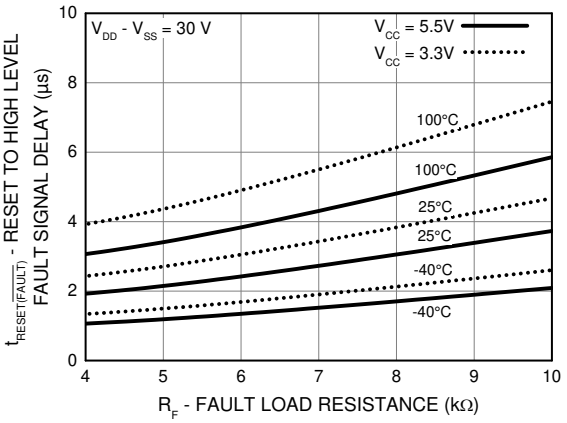


Figure 27. RESET to High Level Fault Signal Delay ($t_{RESET(\overline{FAULT})}$) vs. Fault Load Resistance (R_F)

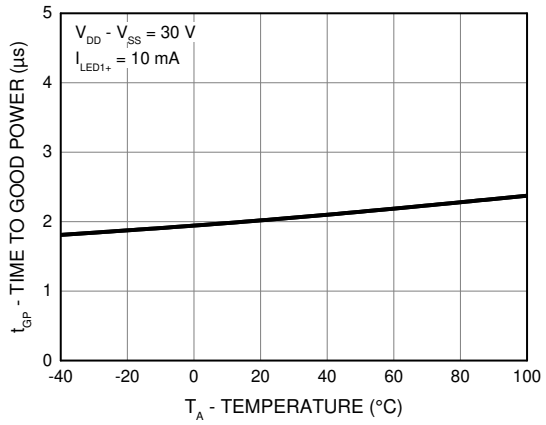


Figure 28. Time to Good Power (t_{GP}) vs. Temperature

Typical Performance Characteristics (Continued)

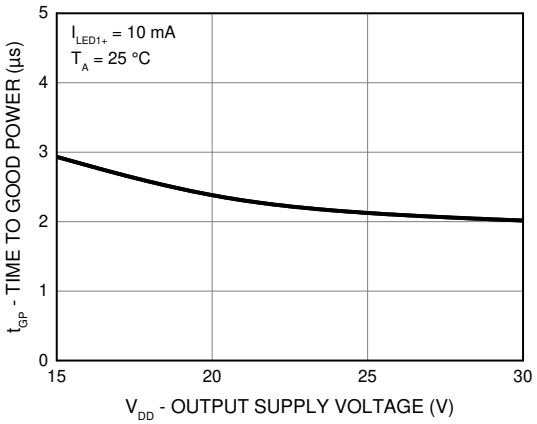


Figure 29. Time to Good Power (t_{GP}) vs. Output Supply Voltage (V_{DD})

Test Circuits

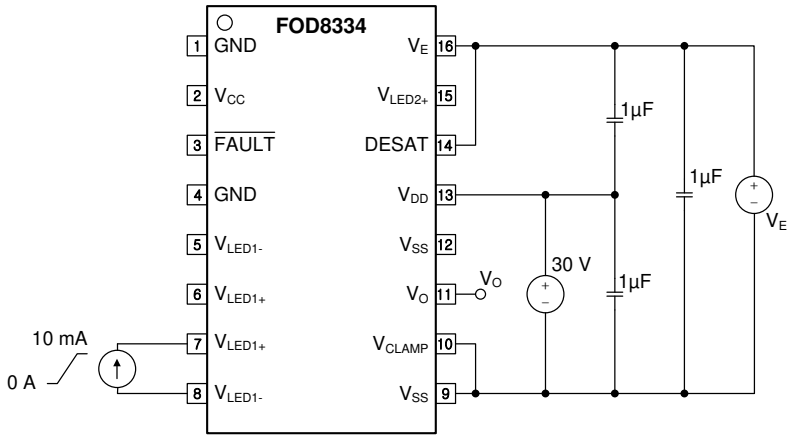


Figure 30. Threshold Input Current Low-to-High (I_{FLH}) Test Circuit

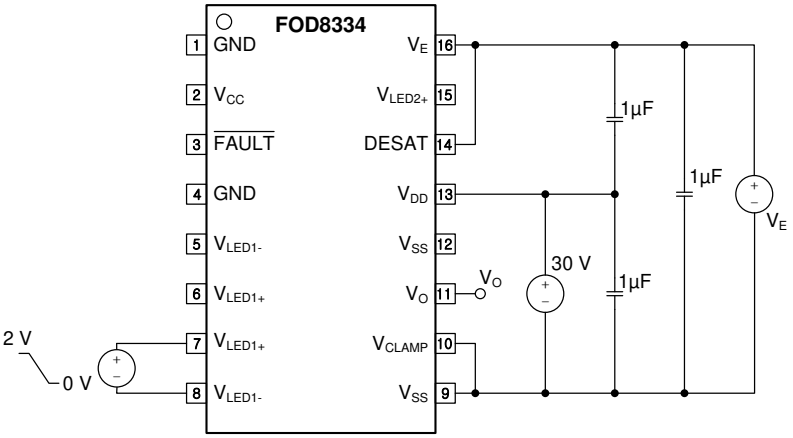


Figure 31. Threshold Input Voltage High-to-Low (V_{FHL}) Test Circuit

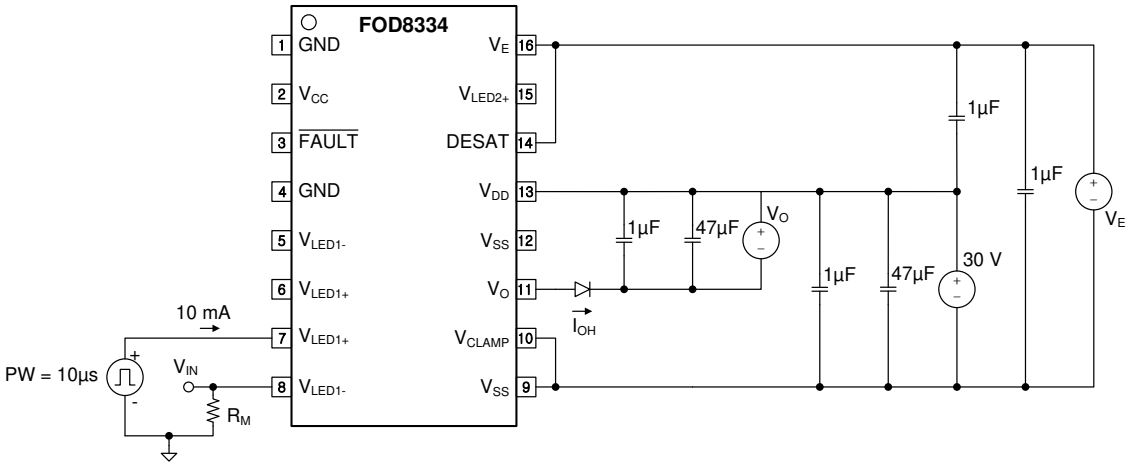


Figure 32. High level Output Current (I_{OH}) Test Circuit

Test Circuits (Continued)

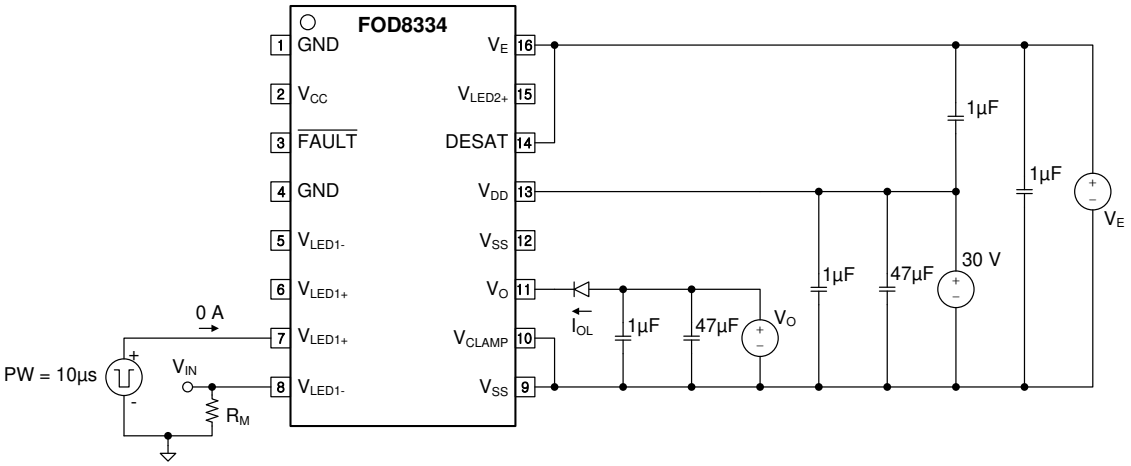


Figure 33. Low Level Output Current (I_{OL}) Test Circuit

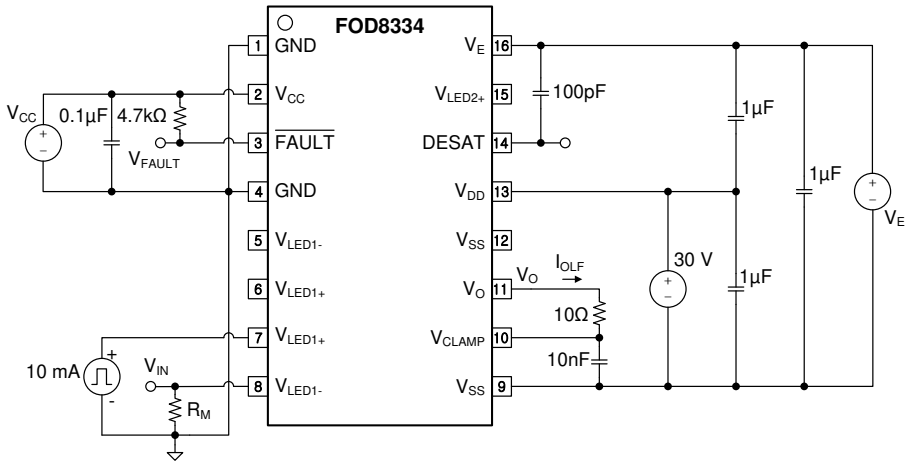


Figure 34. Low Level Output Current During Fault Condition (I_{OLF}) Test Circuit

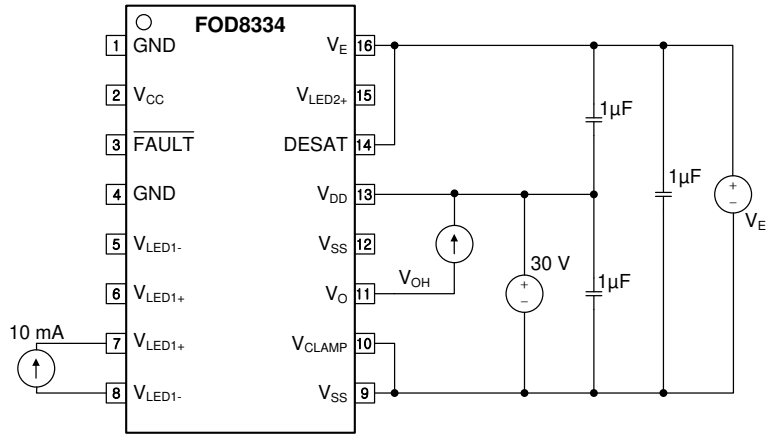


Figure 35. High level Output Voltage (V_{OH}) Test Circuit

Test Circuits (Continued)

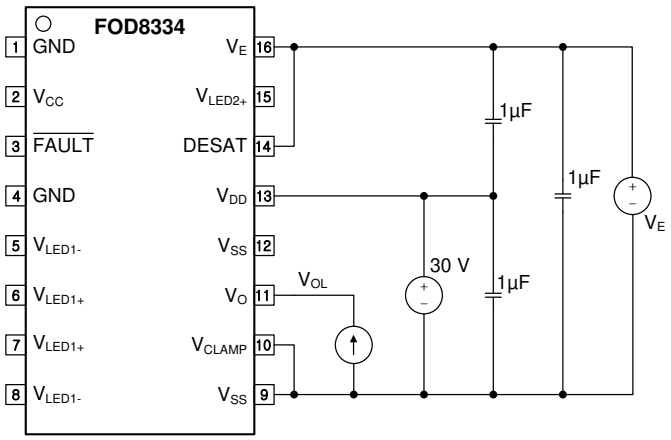


Figure 36. Low Level Output Voltage (V_{OL}) Test Circuit

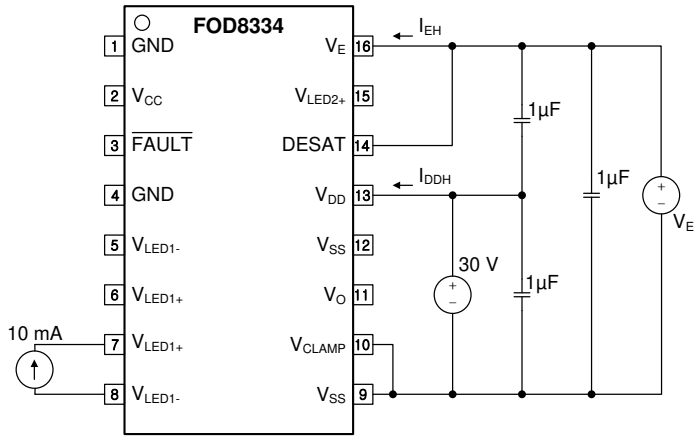


Figure 37. High Level Supply Current (I_{DDH}), V_E High Level Supply Current (I_{EH}) Test Circuit

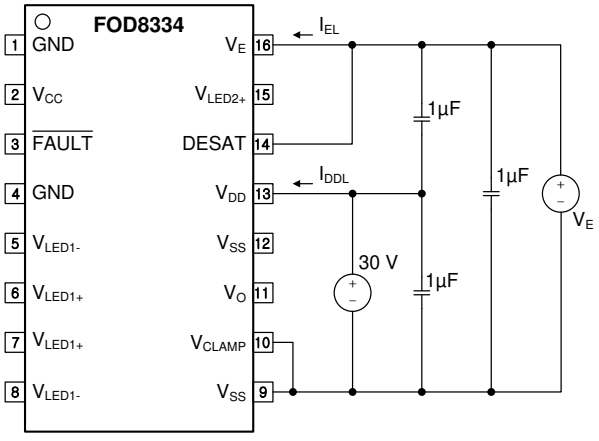


Figure 38. Low Level Supply Current (I_{DDL}), V_E Low Level Supply Current (I_{EL}) Test Circuit

Test Circuits (Continued)

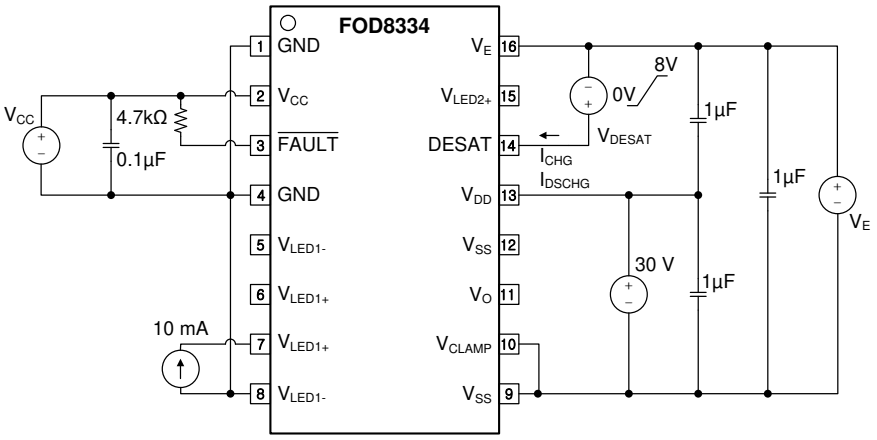


Figure 39. DESAT Threshold (V_{DESAT}), Blanking Capacitor Charge Current (I_{CHG}), Blanking Capacitor Discharge Current (I_{DSCHG}) Test Circuit

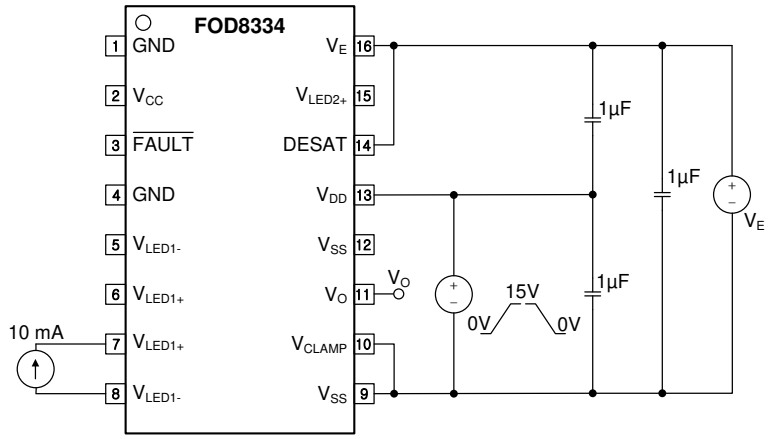


Figure 40. Under-Voltage Lockout Threshold (V_{UVLO+} / V_{UVLO-}), Under-Voltage Lockout Threshold Hysteresis ($UVLO_{HYS}$) Test Circuit

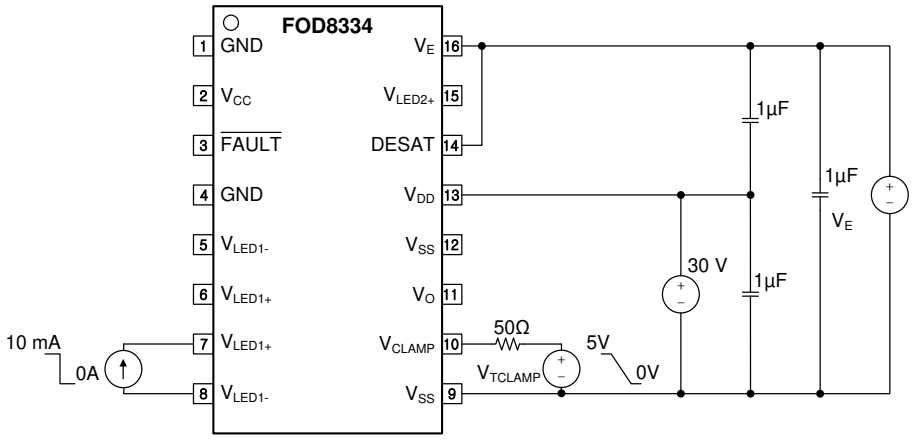


Figure 41. Clamping Threshold Voltage (V_{CLAMP_THRES}) Test Circuit

Test Circuits (Continued)

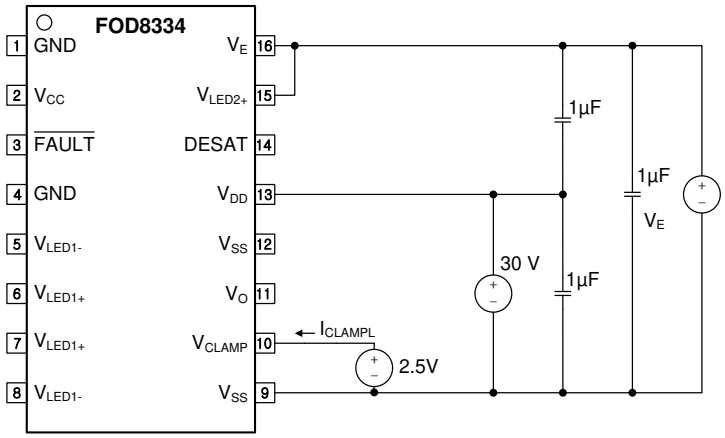


Figure 42. Clamp Low Sinking Current (I_{CLAMPL}) Test Circuit

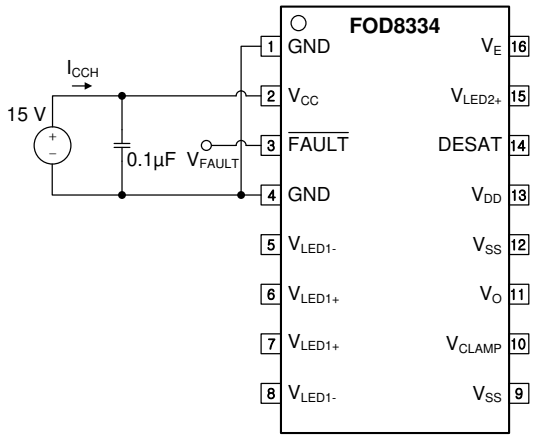


Figure 43. FAULT High Level Supply Current (I_{CCH}) Test Circuit

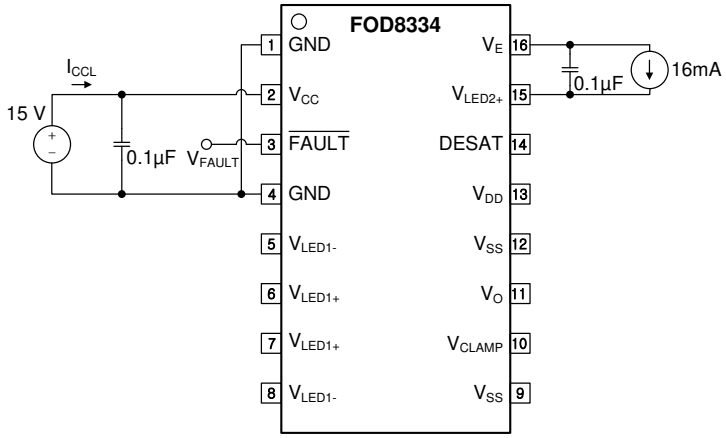


Figure 44. FAULT Low Level Supply Current (I_{CCL}) Test Circuit

Test Circuits (Continued)

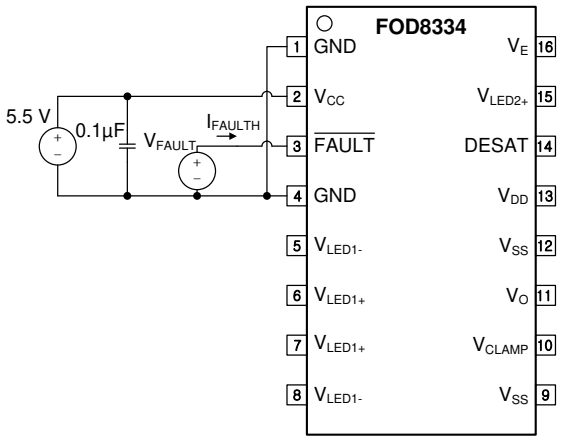


Figure 45. FAULT High Level Output Current ($I_{\overline{FAULTH}}$) Test Circuit

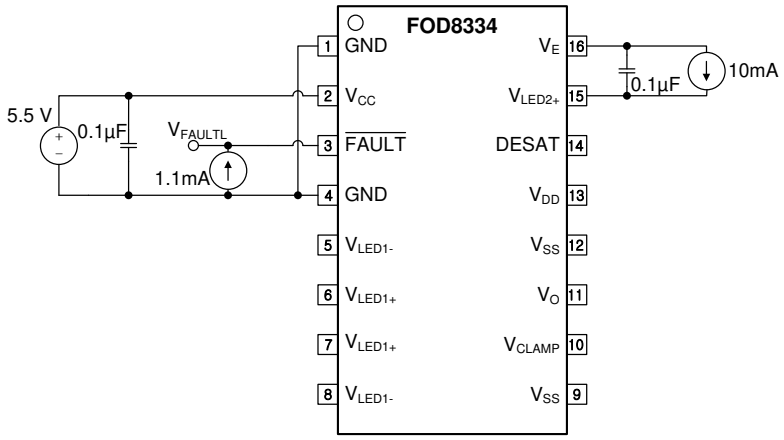


Figure 46. FAULT Low Level Output Voltage ($V_{\overline{FAULTL}}$) Test Circuit

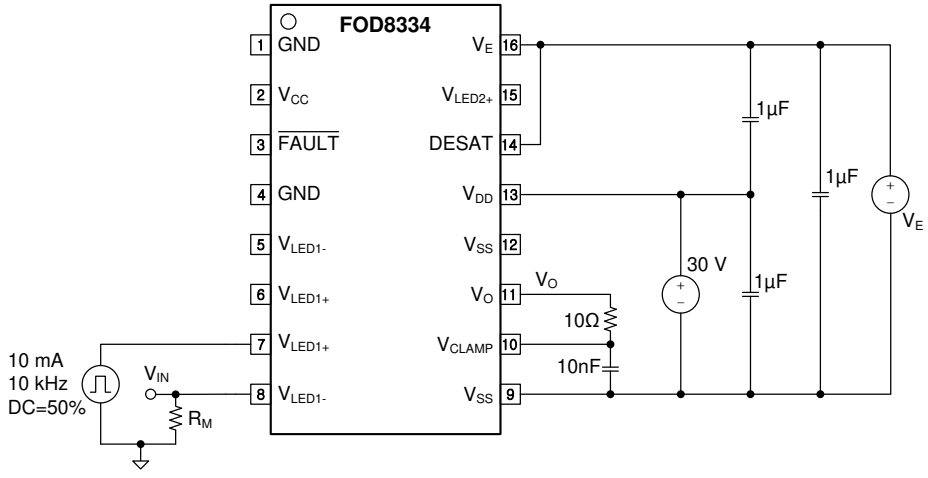


Figure 47. Propagation Delay (t_{PLH}, t_{PHL}), Rise Time (t_R) , Fall Time (t_F), Pulse Width Distortion (PWD)Test Circuit

Test Circuits (Continued)

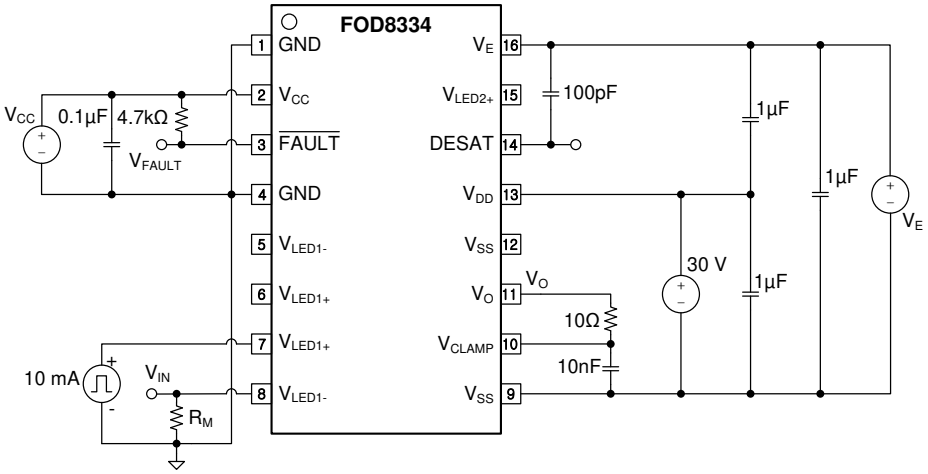


Figure 48. DESAT Sense Delay ($t_{DESAT(90\%)}$, $t_{DESAT(10\%)}$, $t_{DESAT(LOW)}$), DESAT Sense to Low Level FAULT Signal Delay ($t_{DESAT(\overline{FAULT})}$), Reset to High Level FAULT Signal Delay ($t_{RESET(\overline{FAULT})}$), DESAT Input Mute ($t_{DESAT(MUTE)}$) Test Circuit

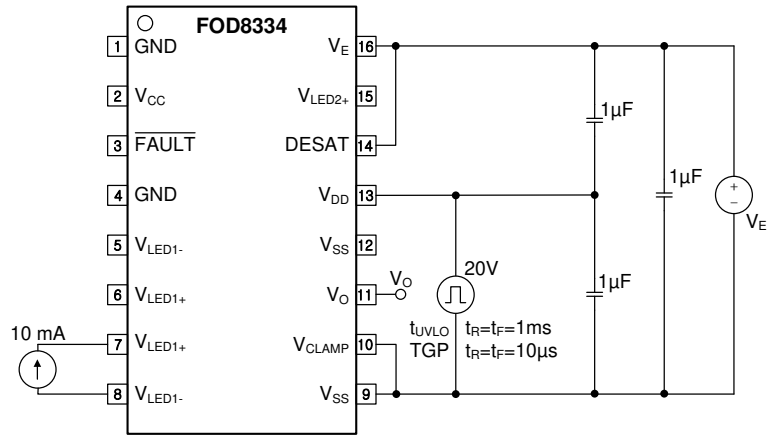


Figure 49. Under-Voltage Lockout Delay (t_{UVLO}), Time to Good Power Delay (t_{GP}) Test Circuit

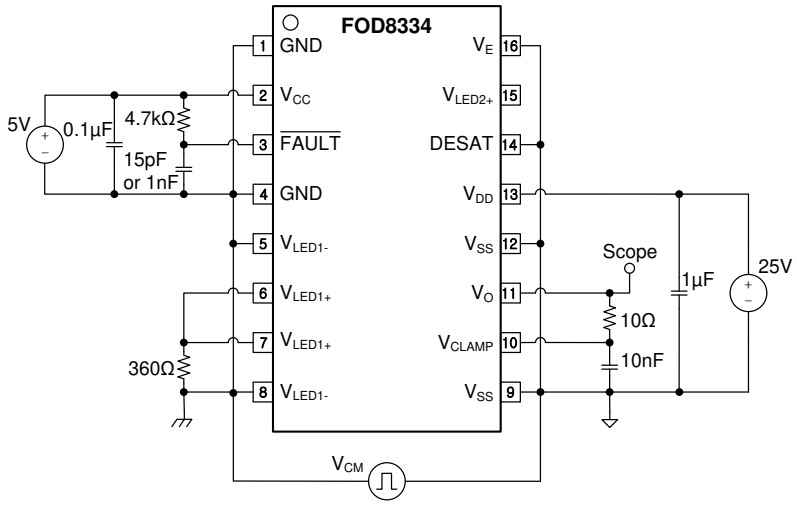


Figure 50. Common-Mode Low (CML) LED1-Off Test Circuit

Test Circuits (Continued)

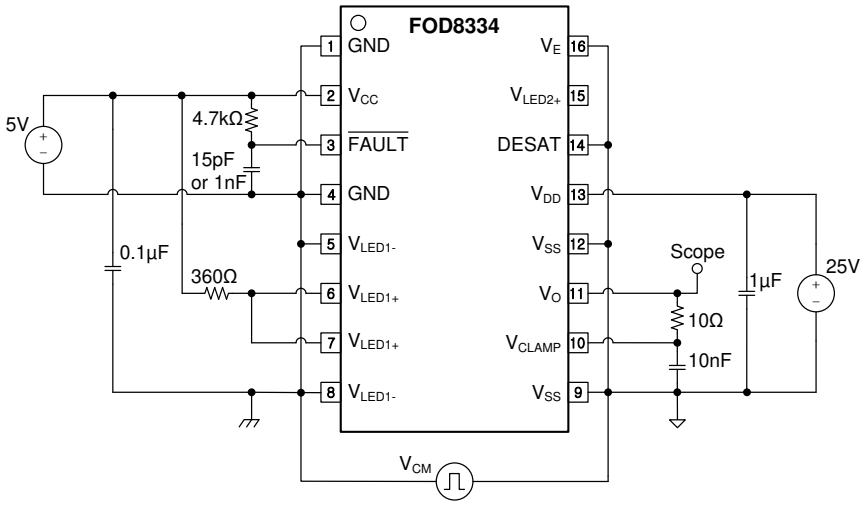


Figure 51. Common-Mode High (CMH) LED1-On Test Circuit

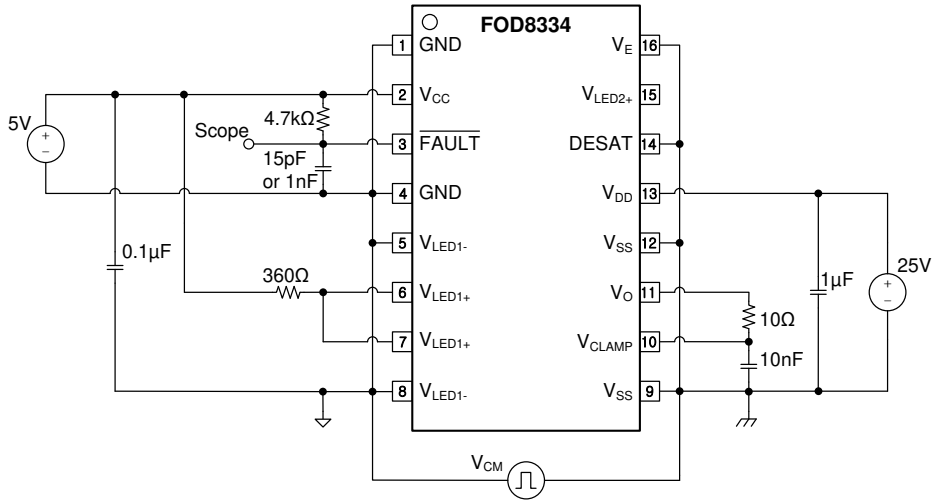


Figure 52. Common-Mode High (CMH) LED2-Off Test Circuit

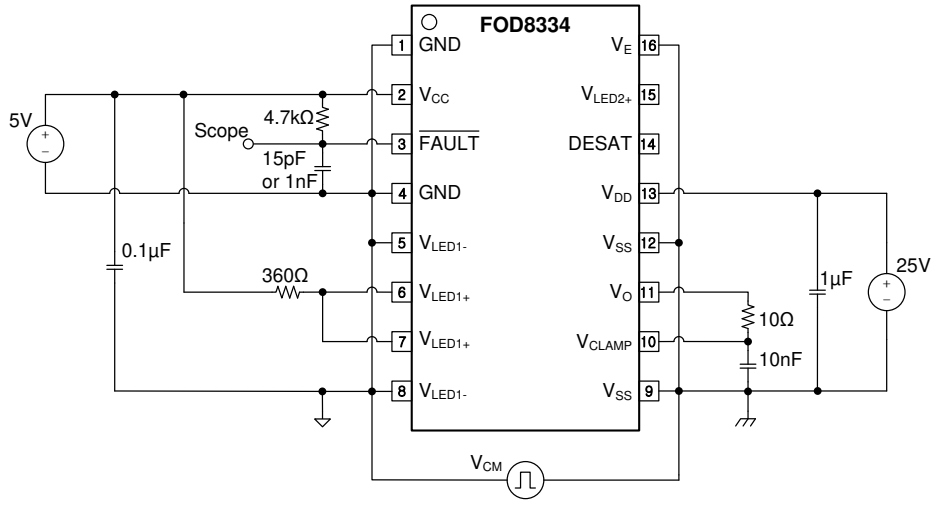


Figure 53. Common-Mode Low (CML) LED2-On Test Circuit