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March 2016

# FQB34P10

## P-Channel QFET<sup>®</sup> MOSFET

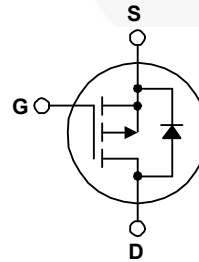
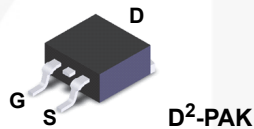
100 V, -33.5 A, 60 mΩ

### Description

This P-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, audio amplifier, DC motor control, and variable switching power applications.

### Features

- 33.5 A, -100 V,  $R_{DS(on)} = 60 \text{ m}\Omega$  (Max.) @  $V_{GS} = .10 \text{ V}$ ,  $I_D = -16.75 \text{ A}$
- Low Gate Charge (Typ. 85 nC)
- Low Crss (Typ. 170 pF)
- 100% Avalanche Tested
- 175°C Maximum Junction Temperature Rating



### Absolute Maximum Ratings T<sub>C</sub> = 25°C unless otherwise noted.

Symbol	Parameter	FQB34P10TM	Unit
$V_{DSS}$	Drain-Source Voltage	-100	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ )	-33.5	A
	- Continuous ( $T_C = 100^\circ\text{C}$ )	-23.5	A
$I_{DM}$	Drain Current - Pulsed (Note 1)	-134	A
$V_{GSS}$	Gate-Source Voltage	$\pm 25$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	2200	mJ
$I_{AR}$	Avalanche Current (Note 1)	-33.5	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	15.5	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	-6.0	V/ns
$P_D$	Power Dissipation ( $T_A = 25^\circ\text{C}$ ) *	3.75	W
	Power Dissipation ( $T_C = 25^\circ\text{C}$ )	155	W
	- Derate above 25°C	1.03	W/°C
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +175	°C
$T_L$	Maximum lead temperature for soldering, 1/8" from case for 5 seconds	300	°C

### Thermal Characteristics

Symbol	Parameter	FQB34P10TM	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.97	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2-oz Copper), Max.	62.5	
	Thermal Resistance, Junction to Ambient (*1 in <sup>2</sup> Pad of 2-oz Copper), Max.	40	

FQB34P10 — P-Channel QFET<sup>®</sup> MOSFET

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FQB34P10TM	FQB34P10	D <sup>2</sup> -PAK	Tape and Reel	330 mm	24 mm	800 units

## Electrical Characteristics

$T_C = 25^\circ\text{C}$  unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-100	--	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	-0.1	--	$V/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = -100\text{ V}, V_{GS} = 0\text{ V}$	--	--	-1	$\mu\text{A}$
		$V_{DS} = -80\text{ V}, T_C = 150^\circ\text{C}$	--	--	-10	$\mu\text{A}$
$I_{GSSF}$	Gate-Body Leakage Current, Forward	$V_{GS} = -25\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA
$I_{GSSR}$	Gate-Body Leakage Current, Reverse	$V_{GS} = 25\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-2.0	--	-4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = -10\text{ V}, I_D = -16.75\text{ A}$	--	0.049	0.06	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = -40\text{ V}, I_D = -16.75\text{ A}$	--	23	--	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = -25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	2240	2910	pF
$C_{oss}$	Output Capacitance		--	730	950	pF
$C_{rss}$	Reverse Transfer Capacitance		--	170	220	pF

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = -50\text{ V}, I_D = -33.5\text{ A},$ $R_G = 25\ \Omega$	--	25	60	ns	
$t_r$	Turn-On Rise Time		--	250	510	ns	
$t_{d(off)}$	Turn-Off Delay Time		(Note 4)	--	160	330	ns
$t_f$	Turn-Off Fall Time		(Note 4)	--	210	430	ns
$Q_g$	Total Gate Charge	$V_{DS} = -80\text{ V}, I_D = -33.5\text{ A},$ $V_{GS} = -10\text{ V}$	--	85	110	nC	
$Q_{gs}$	Gate-Source Charge		(Note 4)	--	15	--	nC
$Q_{gd}$	Gate-Drain Charge		(Note 4)	--	45	--	nC

### Drain-Source Diode Characteristics and Maximum Ratings

$I_S$	Maximum Continuous Drain-Source Diode Forward Current	--	--	-33.5	A	
$I_{SM}$	Maximum Pulsed Drain-Source Diode Forward Current	--	--	-134	A	
$V_{SD}$	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -33.5\text{ A}$	--	--	-4.0	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = -33.5\text{ A},$ $di_F / dt = 100\text{ A}/\mu\text{s}$	--	160	--	ns
$Q_{rr}$	Reverse Recovery Charge		--	0.88	--	$\mu\text{C}$

#### Notes:

1. Repetitive rating : pulse-width limited by maximum junction temperature.
2.  $L = \text{mH}, I_{AS} = -33.5\text{ A}, V_{DD} = -25\text{ V}, R_G = 25\ \Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq -33.5\text{ A}, di/dt \leq 300\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature.



## Typical Characteristics

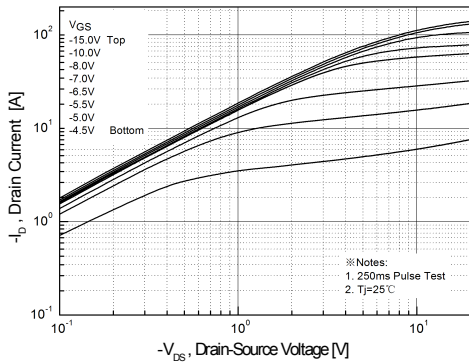


Figure 1. On-Region Characteristics

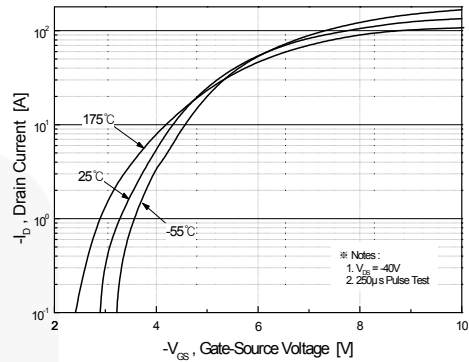


Figure 2. Transfer Characteristics

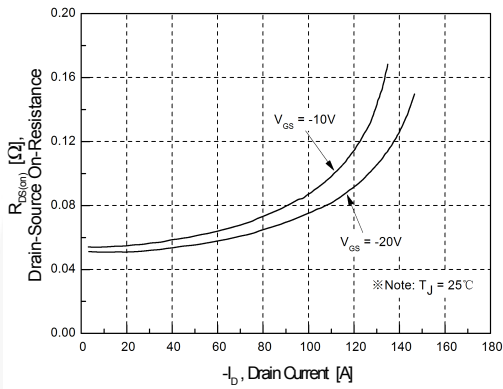


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

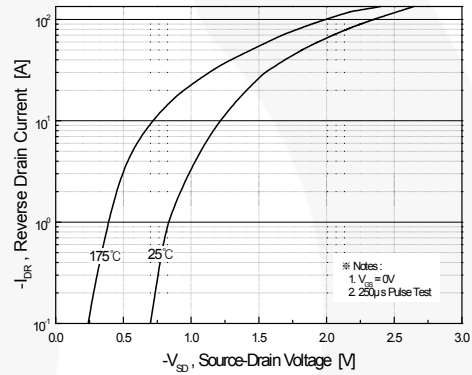


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

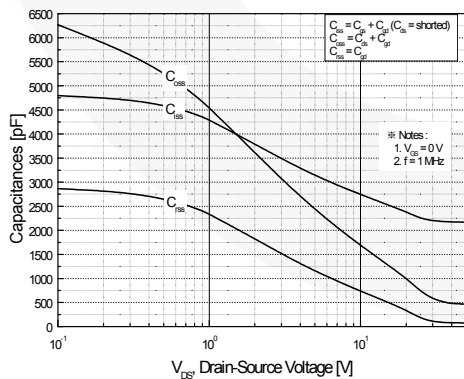


Figure 5. Capacitance Characteristics

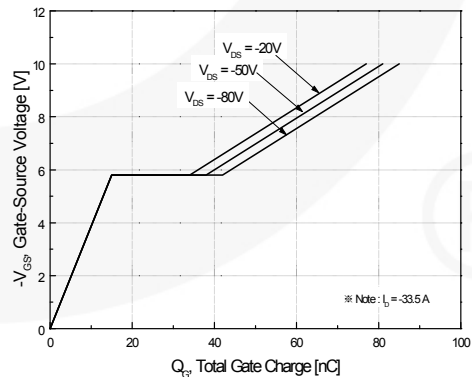
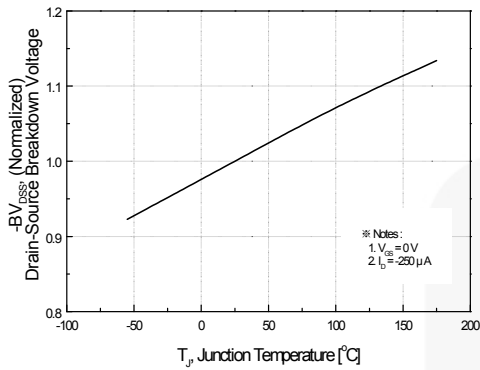
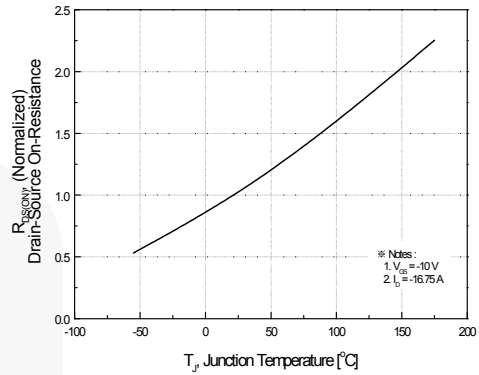


Figure 6. Gate Charge Characteristics

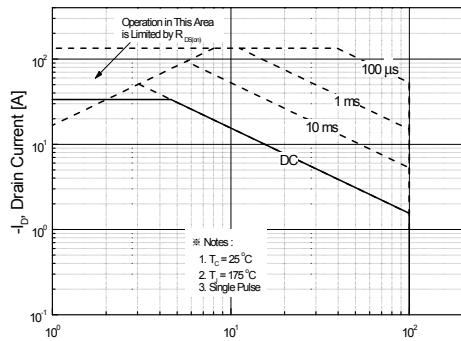
**Typical Characteristics** (Continued)



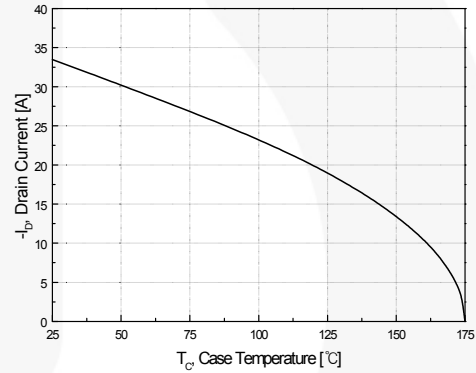
**Figure 7. Breakdown Voltage Variation vs. Temperature**



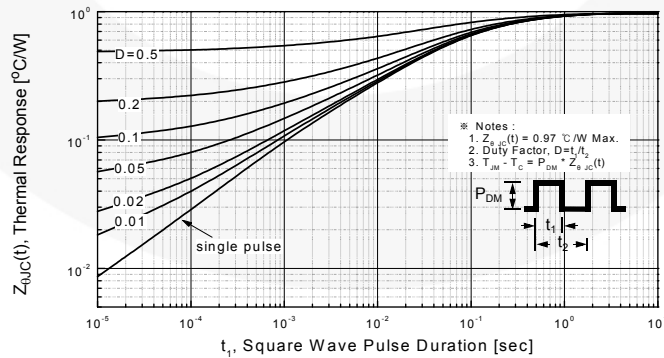
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Transient Thermal Response Curve**

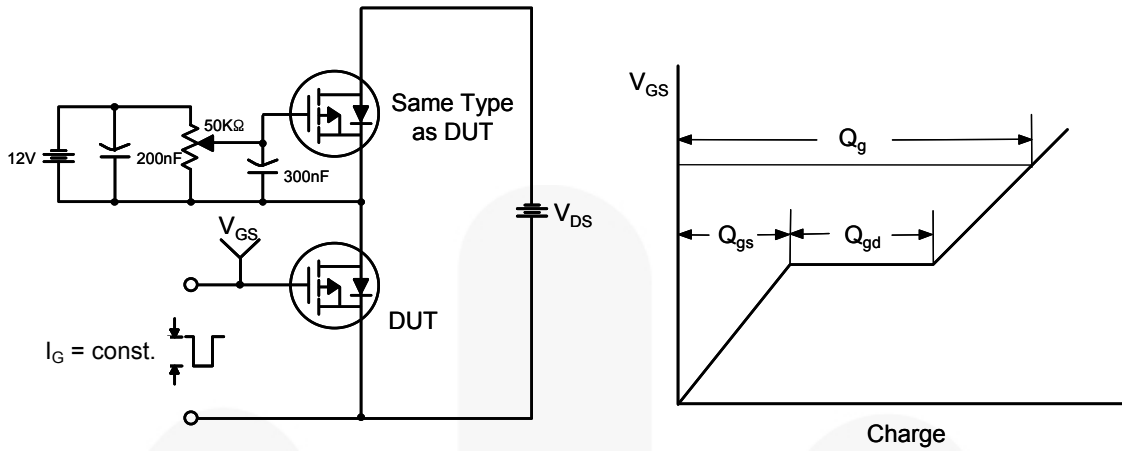


Figure 12. Gate Charge Test Circuit & Waveform

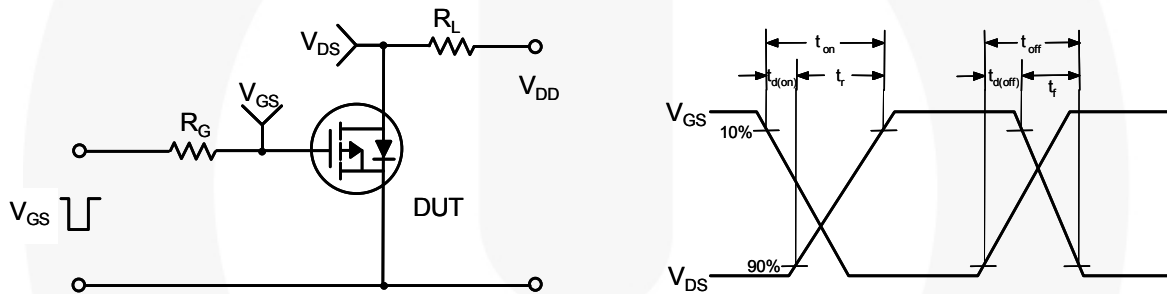


Figure 13. Resistive Switching Test Circuit & Waveforms

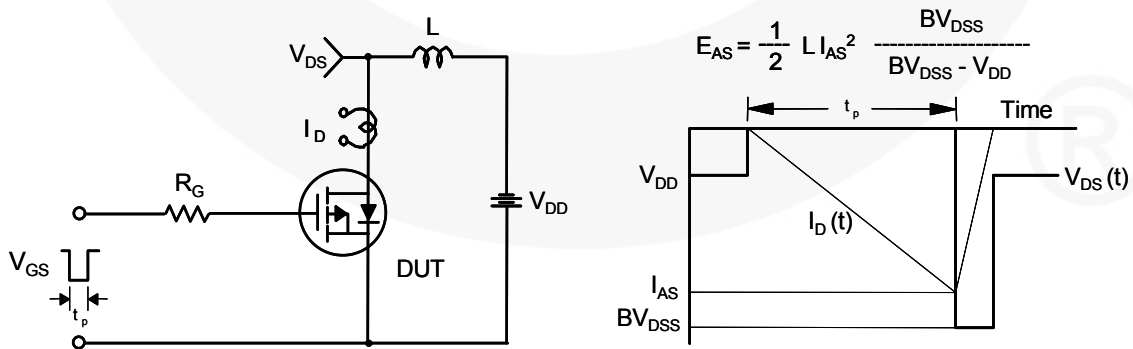


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

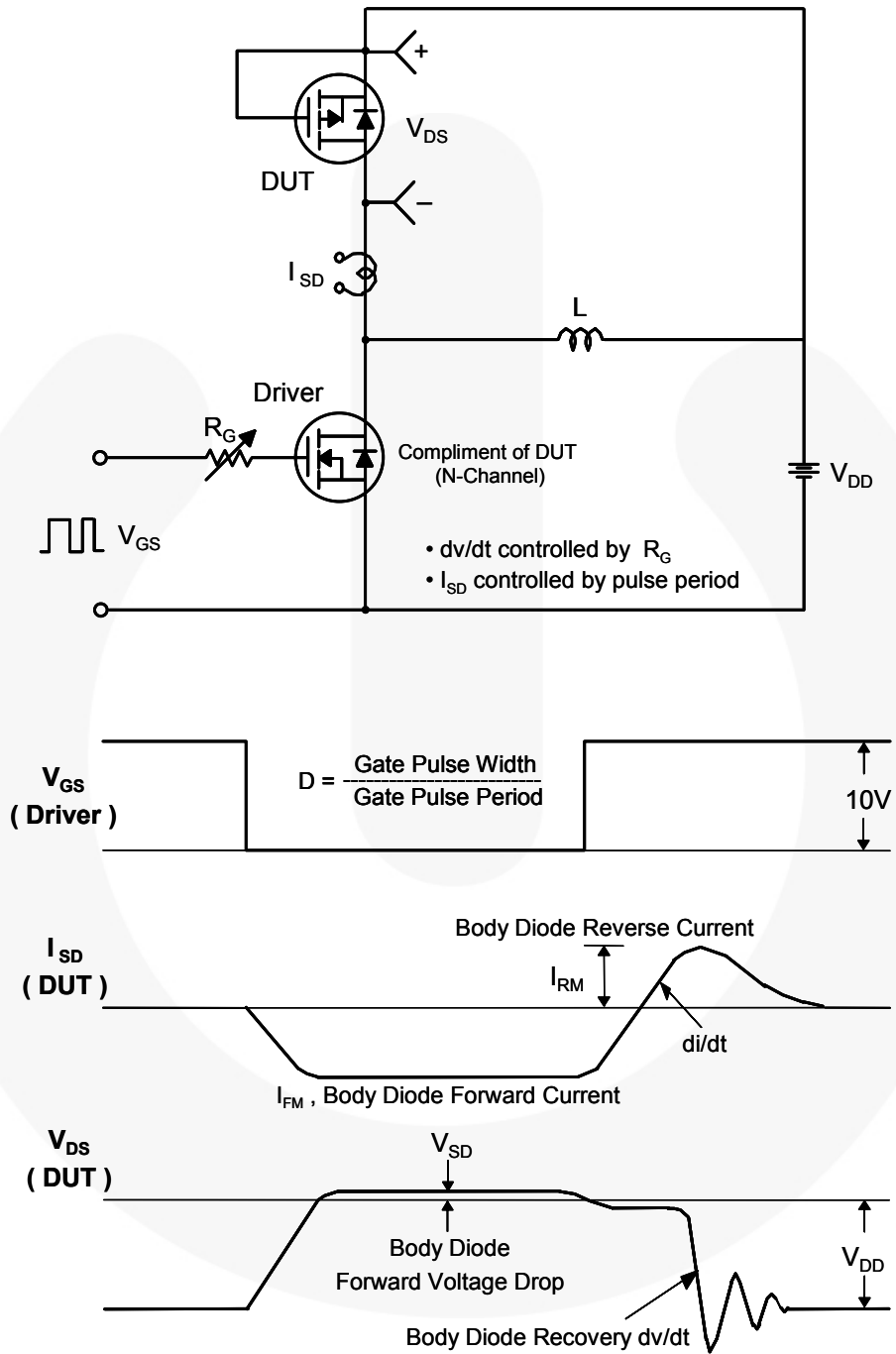
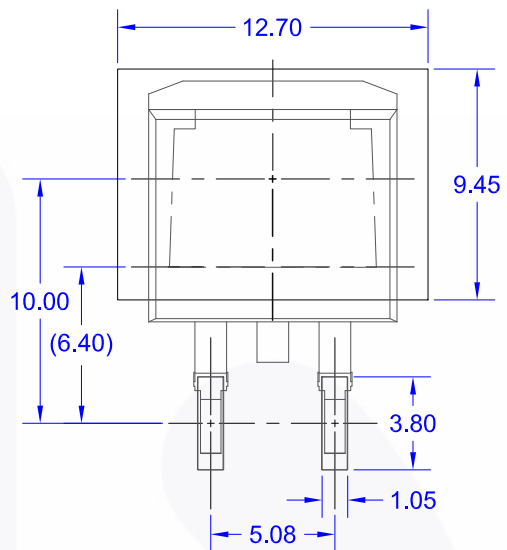
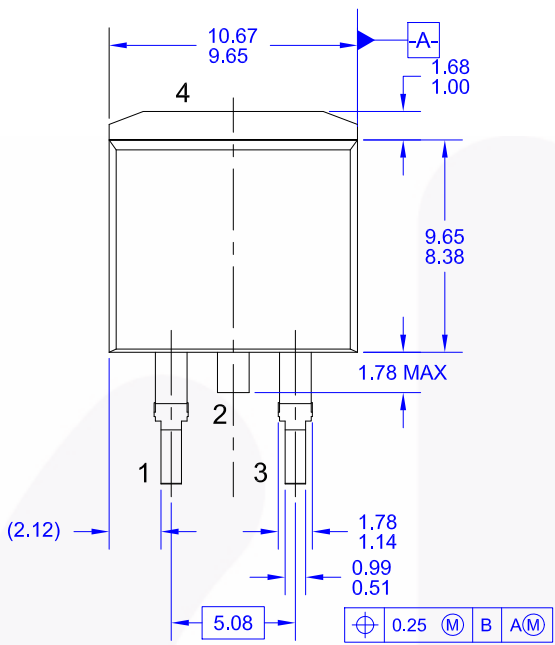


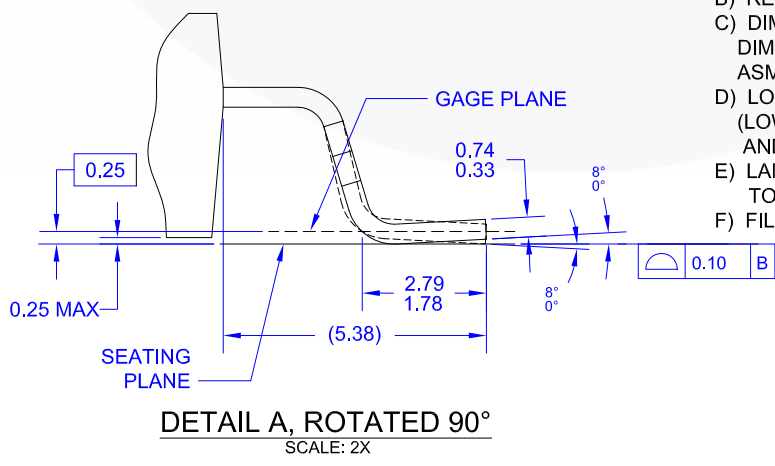
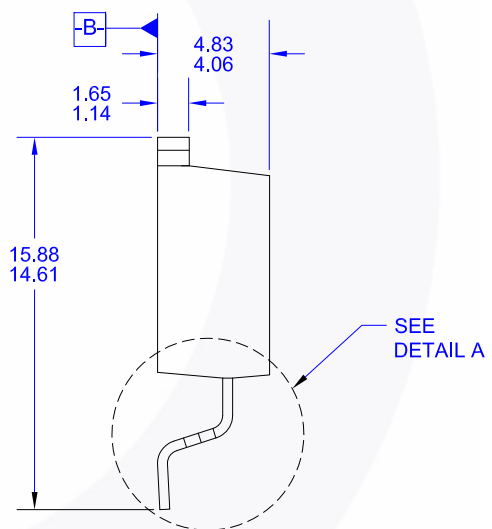
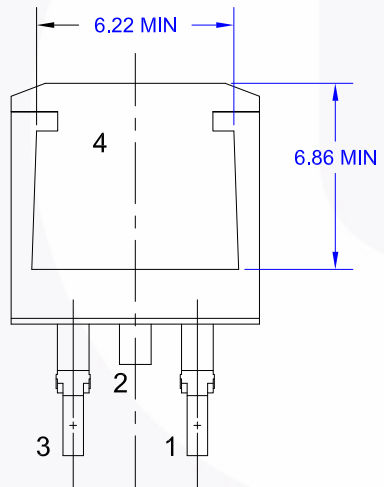
Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms



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LAND PATTERN RECOMMENDATION  
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- NOTES: UNLESS OTHERWISE SPECIFIED
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  - C) DIMENSIONING AND TOLERANCING PER DIMENSIONING AND TOLERANCING PER ASME Y14.5 - 2009.
  - D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE).
  - E) LANDPATTERN RECOMMENDATION PER IPC TO254P1524X482-3N
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