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May 2015

FQD3P50

P-Channel QFET® MOSFET

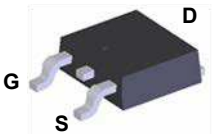
- 500 V, - 2.1 A, 4.9 Ω

Description

This P-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor®'s proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.

Features

- - 2.1 A, - 500 V, $R_{DS(on)}$ = 4.9 Ω (Max.) @ V_{GS} = - 10 V, ID = - 1.05 A
- Low Gate Charge (Typ. 18 nC)
- Low Crss (Typ. 9.5 pF)
- 100% Avalanche Tested



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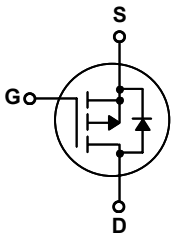


Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter		FQD3P50	Unit
V_{DSS}	Drain-Source Voltage		-500	V
I_D	Drain Current - Continuous (T_C = 25°C)		-2.1	A
	- Continuous (T_C = 100°C)		-1.33	A
I_{DM}	Drain Current - Pulsed	(Note 1)	-8.4	A
V_{GSS}	Gate-Source Voltage		± 30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	250	mJ
I_{AR}	Avalanche Current	(Note 1)	-2.1	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	5.0	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	-4.5	V/ns
P_D	Power Dissipation (T_A = 25°C) *		2.5	W
	Power Dissipation (T_C = 25°C)		50	W
	- Derate above 25°C		0.4	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	FQD3P50	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	2.5	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max. *	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	110	°C/W

* When mounted on the minimum pad size recommended (PCB Mount)

Elerical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 μA	-500	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = -250 μA, Referenced to 25°C	--	0.42	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -500 V, V_{GS} = 0 V	--	--	-1	μA
		V_{DS} = -400 V, T_C = 125°C	--	--	-10	μA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 μA	-3.0	--	-5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -1.05 A	--	3.9	4.9	Ω
g_{FS}	Forward Transconductance	V_{DS} = -50 V, I_D = -1.05 A	--	2.1	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -25 V, V_{GS} = 0 V, f = 1.0 MHz	--	510	660	pF
C_{oss}	Output Capacitance		--	70	90	pF
C_{rss}	Reverse Transfer Capacitance		--	9.5	12	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -250 V, I_D = -2.7 A, R_G = 25 Ω (Note 4)	--	12	35	ns
t_r	Turn-On Rise Time		--	56	120	ns
$t_{d(off)}$	Turn-Off Delay Time		--	35	80	ns
t_f	Turn-Off Fall Time		--	45	100	ns
Q_g	Total Gate Charge	V_{DS} = -400 V, I_D = -2.7 A, V_{GS} = -10 V (Note 4)	--	18	23	nC
Q_{gs}	Gate-Source Charge		--	3.6	--	nC
Q_{gd}	Gate-Drain Charge		--	9.2	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	-2.1	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	-8.4	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -2.1 A	--	--	-5.0	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = -2.7 A, dI_F / dt = 100 A/μs	--	270	--	ns
Q_{rr}	Reverse Recovery Charge		--	1.5	--	μC

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 102mH, I_{AS} = -2.1A, V_{DD} = -50V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ -2.7A, di/dt ≤ 200A/μs, V_{DD} ≤ BV_{DSS}, Starting T_J = 25°C
4. Essentially independent of operating temperature

Typical Characteristics

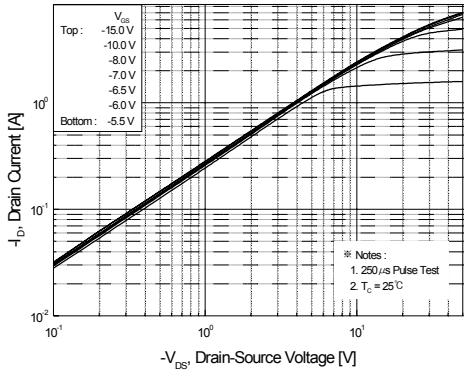


Figure 1. On-Region Characteristics

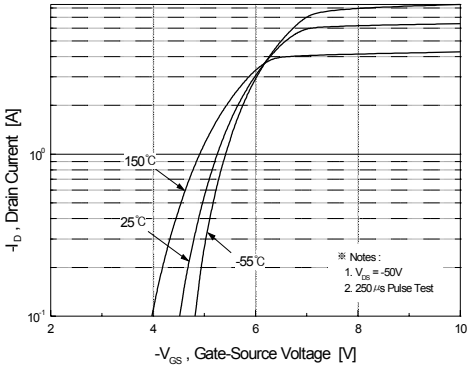


Figure 2. Transfer Characteristics

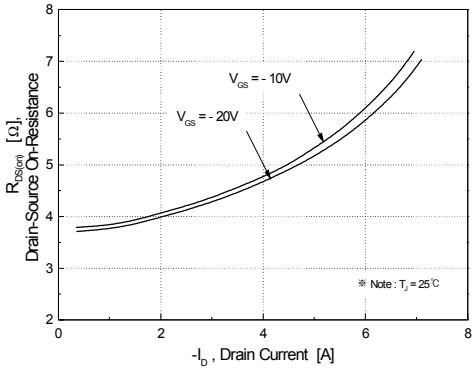


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

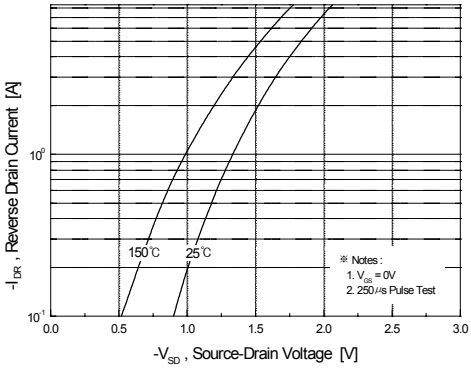


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

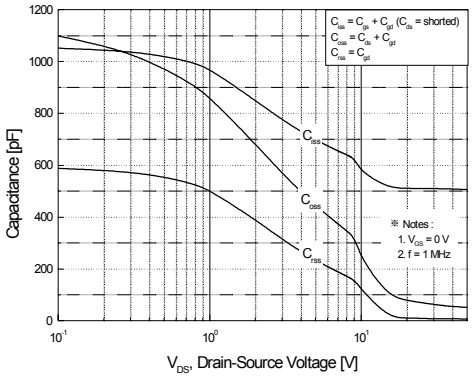


Figure 5. Capacitance Characteristics

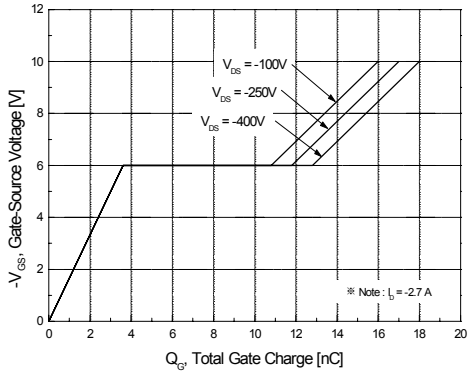


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

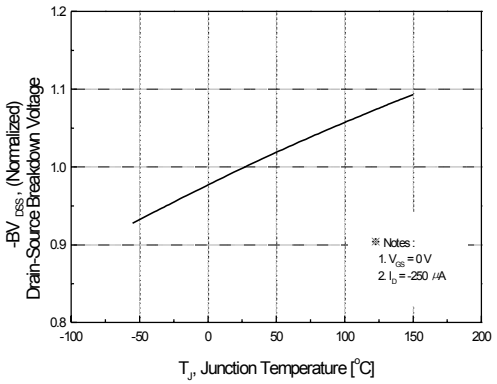


Figure 7. Breakdown Voltage Variation vs. Temperature

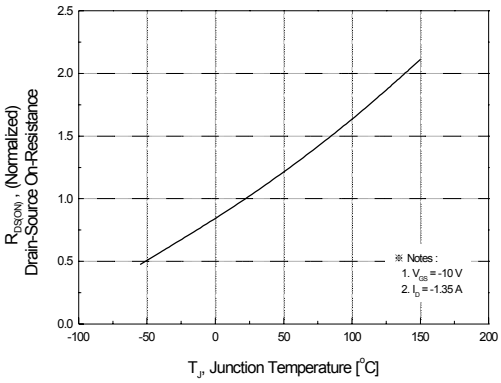


Figure 8. On-Resistance Variation vs. Temperature

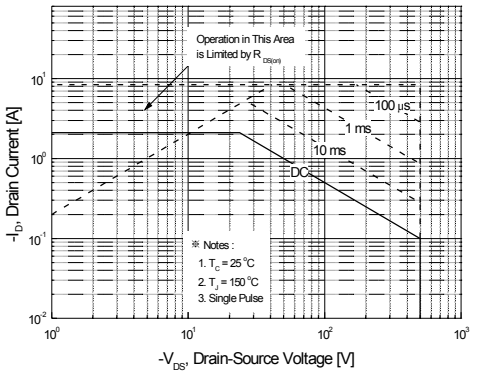


Figure 9. Maximum Safe Operating Area

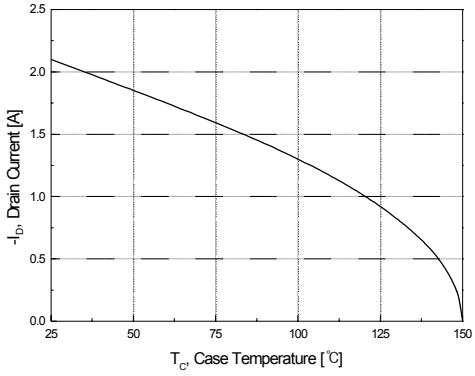


Figure 10. Maximum Drain Current vs. Case Temperature

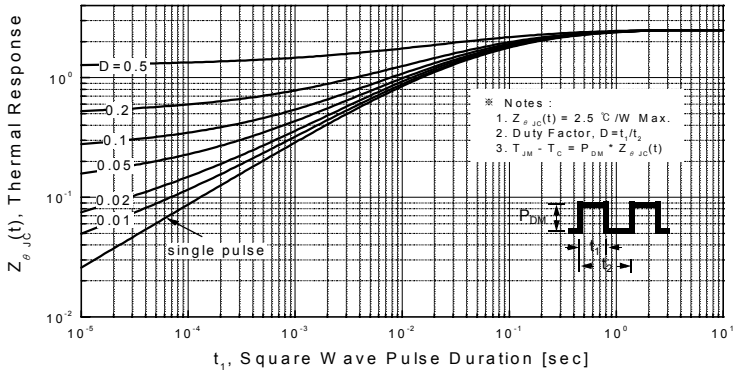
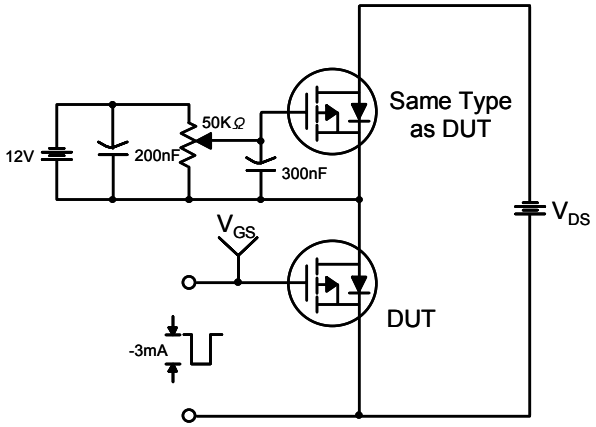
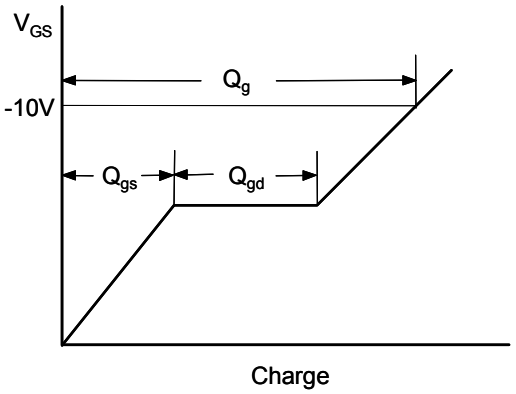


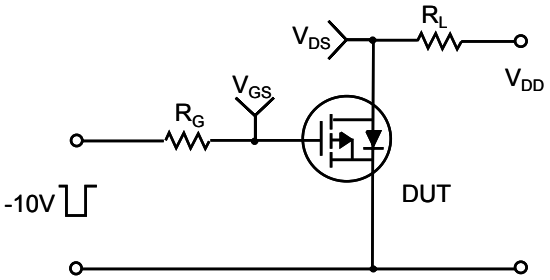
Figure 11. Transient Thermal Response Curve

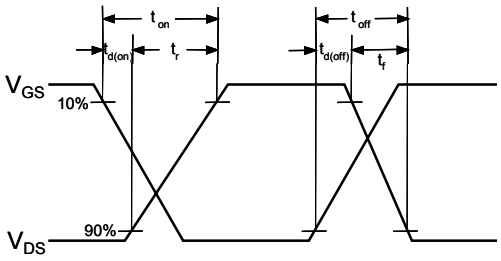
Gate Charge Test Circuit & Waveform



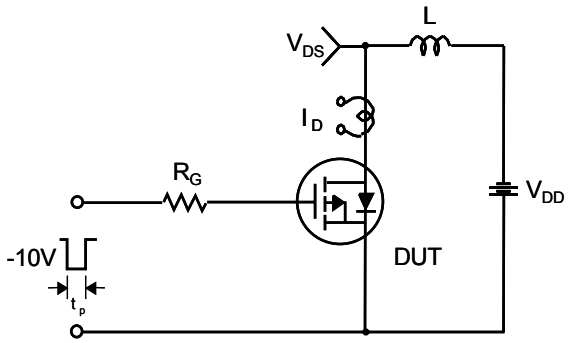


Resistive Switching Test Circuit & Waveforms

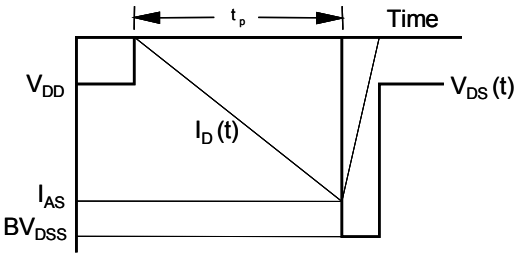




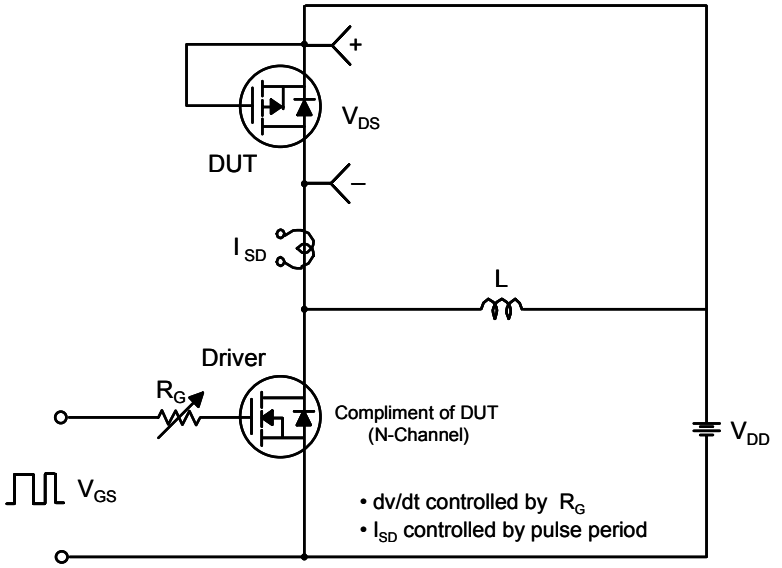
Unclamped Inductive Switching Test Circuit & Waveforms

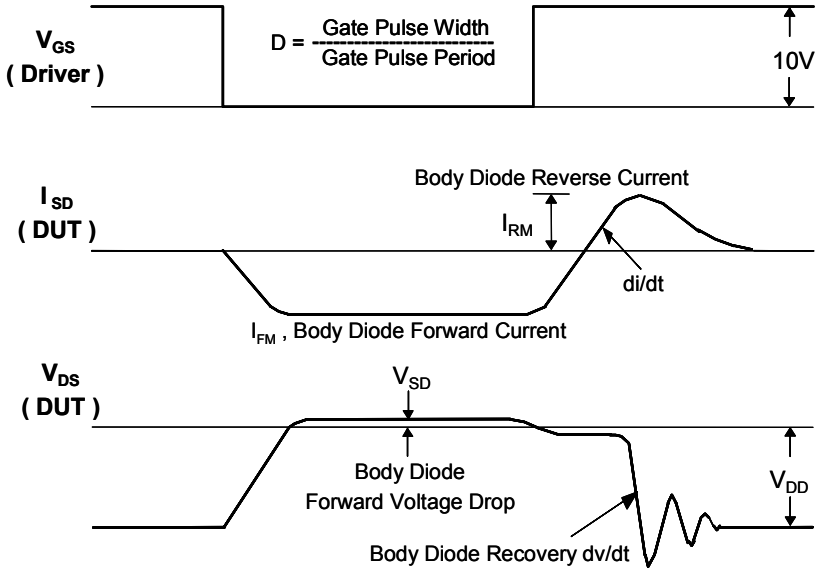


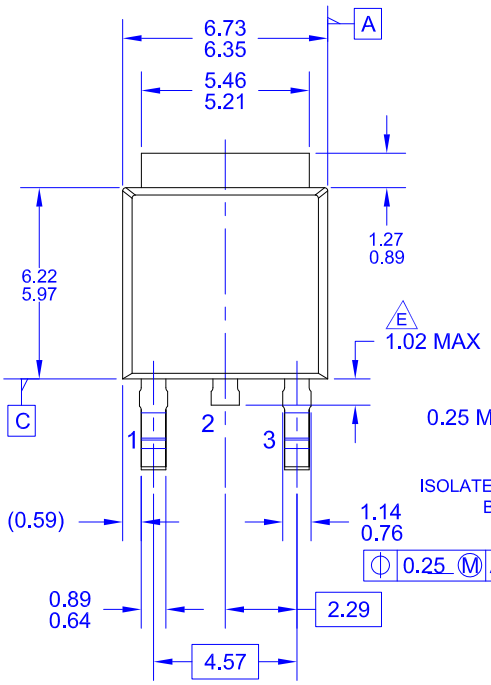
$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$



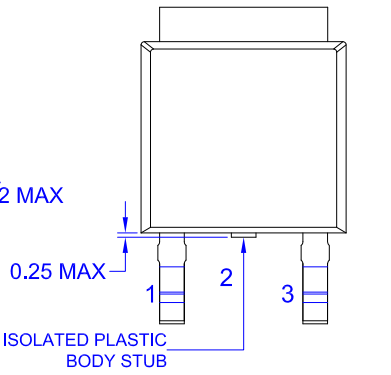
Peak Diode Recovery dv/dt Test Circuit & Waveforms



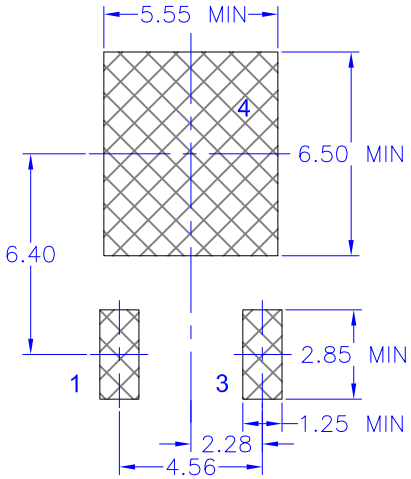




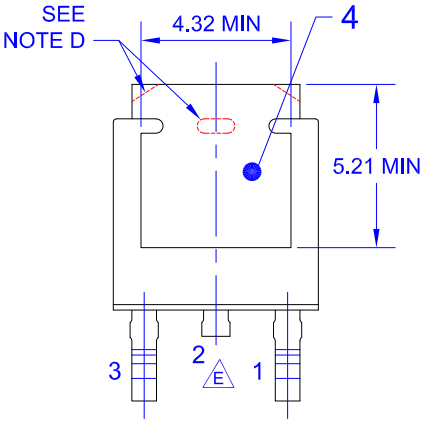
NON-DIODE PRODUCTS VERSION



DIODE PRODUCTS VERSION



LAND PATTERN RECOMMENDATION



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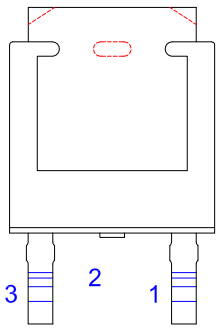

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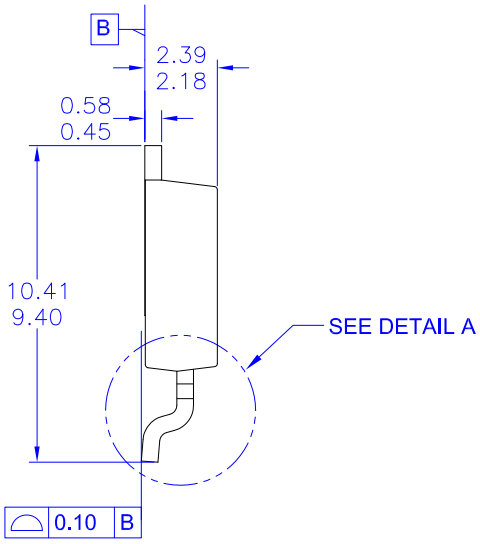

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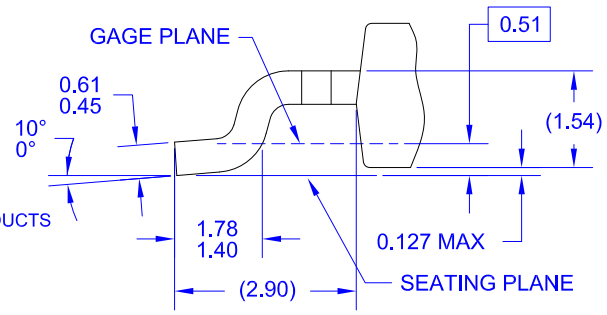
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.
E) TRIMMED METAL CENTER LEAD IS PRESENT ON FOR NON-DIODE PRODUCTS
F) DIMENSIONS ARE EXCLUSIVE OF BURS, MOLD FLASH AND TIE BAR EXTRUSIONS.
G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.
H) DRAWING NUMBER AND REVISION: MKT-TO252A03REV11



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