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November 2013

FQD6N50C

N-Channel QFET[®] MOSFET 500 V, 4.5 A, 1.2 Ω

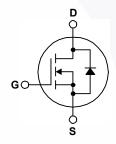
Features

- 4.5 A, 500 V, $R_{DS(on)}$ = 1.2 Ω (Max.) @V_{GS} = 10 V, I_D = 2.25 A
- Low Gate Charge (Typ. 19 nC)
- Low Crss (Typ.15 pF)
- · 100% avalanche tested

Description

This N-Channel enhancement mode power MOSFET is produced using Fairchild Semiconductor's proprietary planar stripe and DMOS technology. This advanced MOSFET technology has been especially tailored to reduce on-state resistance, and to provide superior switching performance and high avalanche energy strength. These devices are suitable for switched mode power supplies, active power factor correction (PFC), and electronic lamp ballasts.





Absolute Maximum Ratings T_C = 25°C unless otherwise noted.

Symbol	Parameter		FQD6N50CTM	Unit	
V_{DSS}	Drain-Source Voltage		500	V	
I _D	Drain Current - Continuous (T _C = 25°C)		4.5	Α	
	- Continuous (T _C = 100°C)		2.7	Α	
I _{DM}	Drain Current - Pulsed	(Note 1)	18	Α	
V _{GSS}	Gate-Source Voltage		± 30	V	
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		300	mJ	
I _{AR}	Avalanche Current	(Note 1)	4.5	Α	
E _{AR}	Repetitive Avalanche Energy (No		6.1	mJ	
dv/dt	Peak Diode Recovery dv/dt (Note 3)		4.5	V/ns	
	Power Dissipation (T _A = 25°C)*		2.5	W	
P_{D}	Power Dissipation (T _C = 25°C)		61	W	
	- Derate above 25°C		0.49	W/°C	
T _J , T _{STG}	Operating and Storage Temperature Range		-55 to +150	°C	
T _L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C	

Thermal Characteristics

Symbol	Parameter	FQD6N50CTM	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	2.05	
D	Thermal Resistance, Junction-to-Ambient (minimum pad of 2 oz copper), Max.	110	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (* 1 in ² pad of 2 oz copper), Max.	50	

Package Marking and Ordering Information

Device Marking Device		Package	Reel Size	Tape Width	Quantity
FQD6N50C	FQD6N50CTM	D-PAK	330 mm	16 mm	2500 units

Electrical Characteristics $T_C = 25^{\circ}C$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
Off Cha	racteristics					
BV _{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	500			V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 250 μA, Referenced to 25°C		0.8		V/°C
	Zero Gate Voltage Drain Current	V _{DS} = 500 V, V _{GS} = 0 V			1	μΑ
I _{DSS}		V _{DS} = 400 V, T _C = 125°C			10	μΑ
I _{GSSF}	Gate-Body Leakage Current, Forward	V _{GS} = 30 V, V _{DS} = 0 V			100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V _{GS} = -30 V, V _{DS} = 0 V			-100	nA
On Cha	racteristics					
V _{GS(th)}	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_{D} = 250 \mu\text{A}$	2.0		4.0	V
R _{DS(on)}	Static Drain-Source On-Resistance	V _{GS} = 10 V, I _D = 2.25A		1.0	1.2	Ω
g _{FS}	Forward Transconductance	$V_{DS} = 40 \text{ V}, I_{D} = 2.25 \text{A}$		4.5		S
C _{iss}	Input Capacitance Output Capacitance	V _{DS} = 25 V, V _{GS} = 0 V, f = 1.0 MHz		540 80	700 105	pF pF
C _{oss}	Output Capacitance	f = 1.0 MHz		80	105	pF
C _{rss}	Reverse Transfer Capacitance			15	20	pF
Switchi	ng Characteristics					
t _{d(on)}	Turn-On Delay Time	V _{DD} = 250 V, I _D = 4.5A,		10	30	ns
t _r	Turn-On Rise Time	$R_{G} = 25 \Omega$		35	80	ns
t _{d(off)}	Turn-Off Delay Time	11.G 20 32		55	120	ns
t _f	Turn-Off Fall Time	(Note 4)		45	100	ns
Qg	Total Gate Charge	V _{DS} = 400 V, I _D = 4.5A,	/	19	25	nC
Q _{gs}	Gate-Source Charge	V _{GS} = 10 V		2.8		nC
Q _{gd}	Gate-Drain Charge	(Note 4)		8.8		nC
Drain-S	ource Diode Characteristics a	nd Maximum Ratings				
I _S	Maximum Continuous Drain-Source Diode Forward Current				4.5	Α
I _{SM}	Maximum Pulsed Drain-Source Diode F	Forward Current			18	Α
V _{SD}	Drain-Source Diode Forward Voltage	V _{GS} = 0 V, I _S = 4.5 A			1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _S = 4.5 A,		260		ns
Q _{rr}	Reverse Recovery Charge	dI _F / dt = 100 A/μs		1.6		μС

NOTES:

 $^{{\}bf 1.}\ Repetitive\ Rating: Pulse\ width\ limited\ by\ maximum\ junction\ temperature.$

^{2.} L = 26.6 mH, I_{AS} = 4.5A, V_{DD} = 50V, R_{G} = 25 Ω , starting T_{J} = 25°C.

 $^{3.~}I_{SD} \leq~4.5 \text{A, di/dt} \leq 200 \text{A/}\mu\text{s, V}_{DD} \leq \text{BV}_{DSS,} \, \text{starting} \quad \text{T}_{J} = 25^{\circ}\text{C}.$

^{4.} Essentially independent of operating temperature.

Typical Characteristics

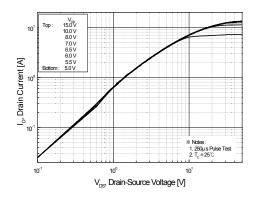


Figure 1. On-Region Characteristics

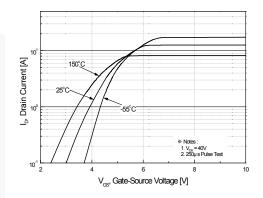


Figure 2. Transfer Characteristics

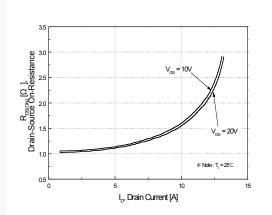


Figure 3. On-Resistance Variation vs Drain Current and Gate Voltage

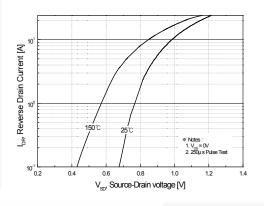


Figure 4. Body Diode Forward Voltage Variation with Source Current and Temperature

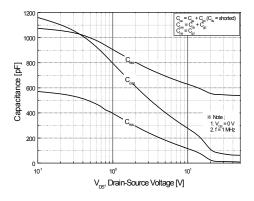


Figure 5. Capacitance Characteristics

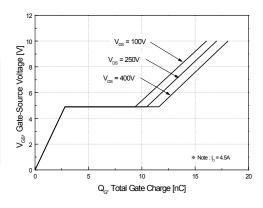


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

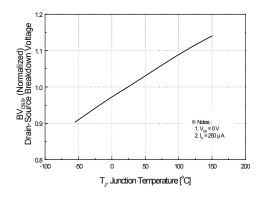


Figure 7. Breakdown Voltage Variation vs Temperature

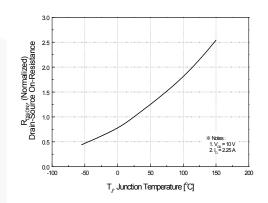


Figure 8. On-Resistance Variation vs Temperature

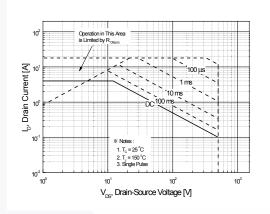


Figure 9. Maximum Safe Operating Area

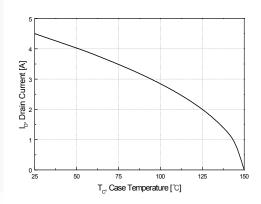


Figure 10. Maximum Drain Current vs Case Temperature

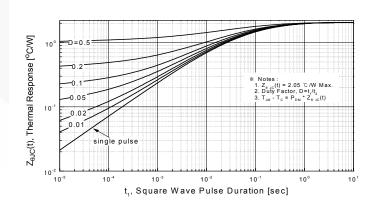


Figure 11. Transient Thermal Response Curve

Figure 12. Gate Charge Test Circuit & Waveform

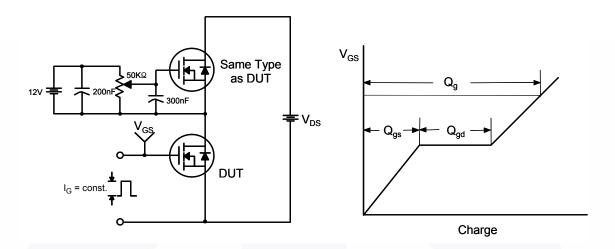


Figure 13. Resistive Switching Test Circuit & Waveforms

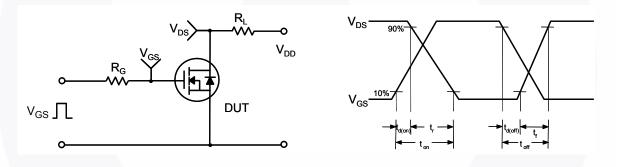
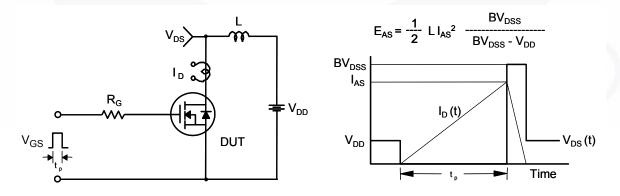


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms



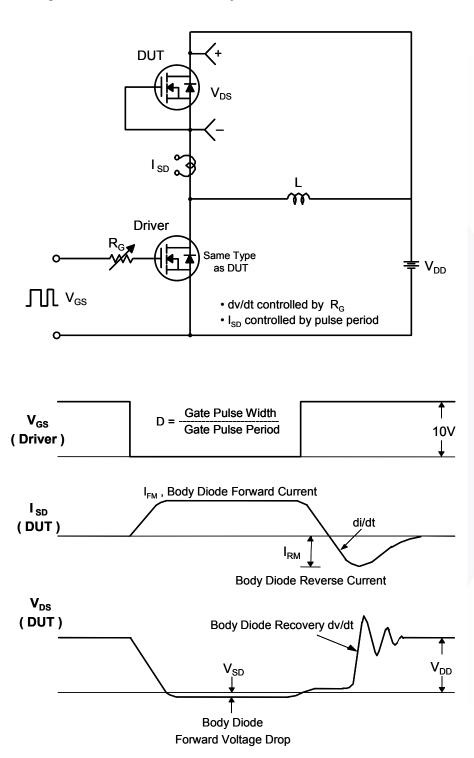


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

Mechanical Dimensions

TO-252 3L (DPAK)

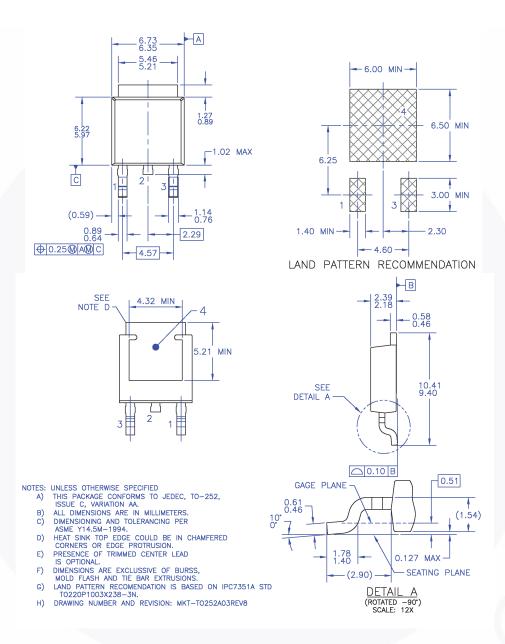


Figure 16. TO252 (D-PAK), Molded, 3 Lead, Option AA&AB

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Dimension in Millimeters





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