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FRDM-GD3000EVB evaluation board

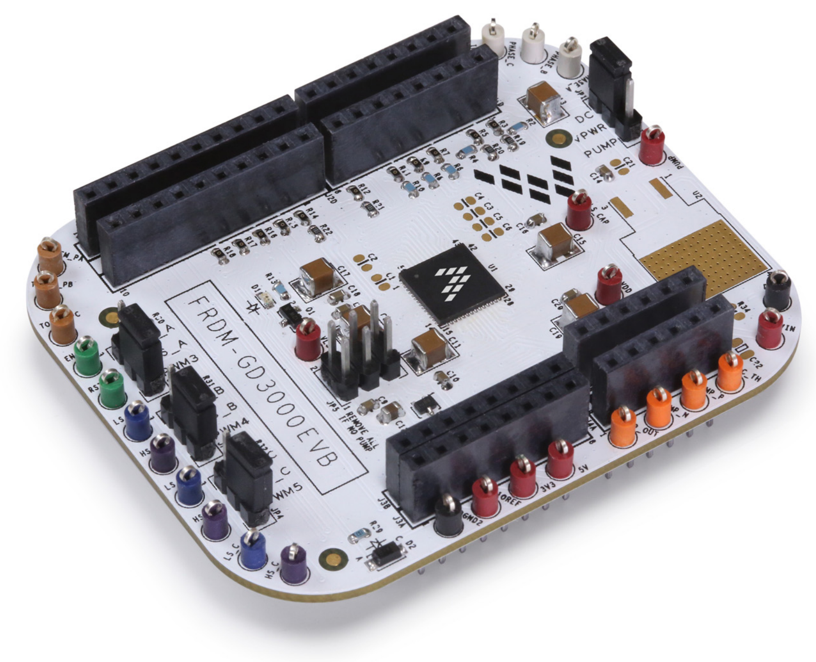

Figure 1. FRDM-GD3000EVB

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NXP provides the enclosed product(s) under the following conditions:

This evaluation kit is intended for use of ENGINEERING DEVELOPMENT OR EVALUATION PURPOSES ONLY. It is provided as a sample IC pre-soldered to a printed circuit board to make it easier to access inputs, outputs, and supply terminals. This evaluation board may be used with any development system or other source of I/O signals by simply connecting it to the host MCU or computer board via off-the-shelf cables. This evaluation board is not a Reference Design and is not intended to represent a final design recommendation for any particular application. Final device in an application will be heavily dependent on proper printed circuit board layout and heat sinking design as well as attention to supply filtering, transient suppression, and I/O signal quality.

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2 Getting started

2.1 Kit contents/packing list

The FRDM-GD3000EVB evaluation board contents include:

- Assembled and tested evaluation board/module in an anti-static bag
- Four Arduino™ female/male connectors (two each 2X8, one each 2X6, one each 2X10)
- Warranty card

2.2 Jump Start

NXP's analog product development boards help to easily evaluate NXP products. These tools support analog mixed signal and power solutions including monolithic ICs using proven high-volume SMARTMOS mixed signal technology, and system-in-package devices utilizing power, SMARTMOS and MCU dies. NXP products enable longer battery life, smaller form factor, component count reduction, ease of design, lower system cost and improved performance in powering state of the art systems.

- Go to www.nxp.com/FRDM-GD3000EVB
- Look for

  Jump Start Your Design

- Download documents, software, and other information

Once the files are downloaded, review the user guide in the bundle. The user guide includes setup instructions, BOM and schematics. Jump Start bundles are available on each tool summary page with the most relevant and current information. The information includes everything needed for design.

2.3 Required equipment and software

To use this kit, you need:

- DC Power supply: 5.0 V to 48 V with up to 10 A current handling capability, depending on motor requirements and MOSFET specifications.
- Typical loads (BLDC motor)
- Any compatible FRDM board (see Section 3.12 "Compatible FRDM boards", page 13)
- USB Standard A (male) to mini or micro (male) cable, depending on which FRDM board is used
- Soldering station
- A FRDM-PWRSTG evaluation board or any custom-designed, but compatible MOSFET board

2.4 System requirements

The kit requires the following:

- USB-enabled PC with Windows® XP or higher

3 Getting to know the hardware

3.1 Board overview

The evaluation board (EVB) provides a development platform exercising all the functions of the GD3000 3-Phase Brushless Motor Pre-Driver IC. The EVB is designed for use in conjunction with any compatible FRDM board. It may be used with the FRDM-KL25Z to enable control via the SPIGen GUI.

3.2 Board features

The board allows evaluation of NXP part MC33812 and all its functions. The board features the following:

- Compatibility with select NXP Freedom Development Platforms
- Test points to allow signal probing
- Optional built in voltage regulator to supply logic level circuitry
- LEDs to indicate the supply status

3.3 Block diagram

A simplified version of the hardware block diagram is shown in Figure 2. It shows only the major components and features of the evaluation board and the entire system. For specifics, refer to the schematic.

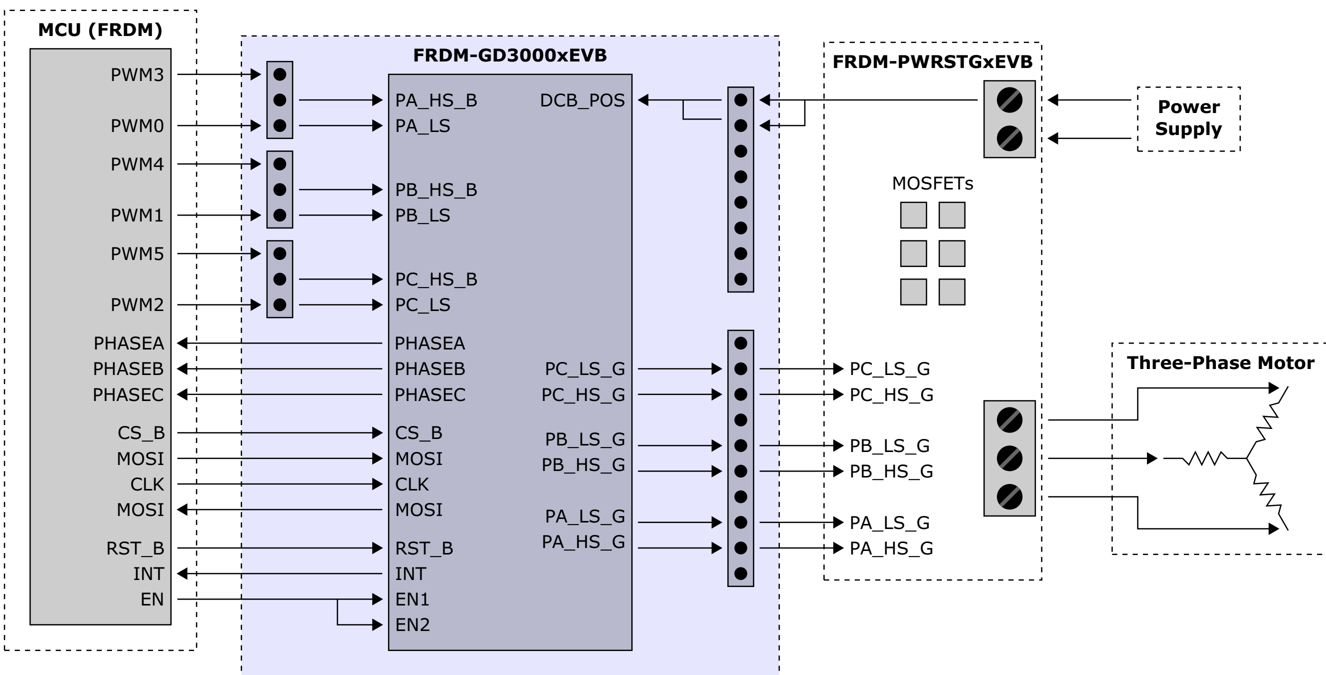

Figure 2. Block diagram

3.4 Device features

This evaluation board features the following NXP product:

Table 1. Device features

Device	Description	Features
MC33812	The GD3000 is a gate driver IC for three-phase motor drive applications providing three half-bridge drivers, each capable of driving two N-channel MOSFETs.	• Supports greater than 1.0 A peak current capability • Can operate off of a single power supply, with a wide range from 6.0 V to 58.0V with 75 V transient protection • Uses a bootstrap gate driver architecture with trickle charge circuitry to support 100% duty cycle • Uses programmable cross-talk protection when the high-side or low-side MOSFET is switching to prevent current flow • Integrated V_{DS} sensing of the high-side and low-side MOSFETs is used to protect the external power stage against overcurrent conditions • Includes a current shunt amplifier for accurate current measurement for phase error detection

3.5 Board description

Figure 3 describes the main blocks of the evaluation board.

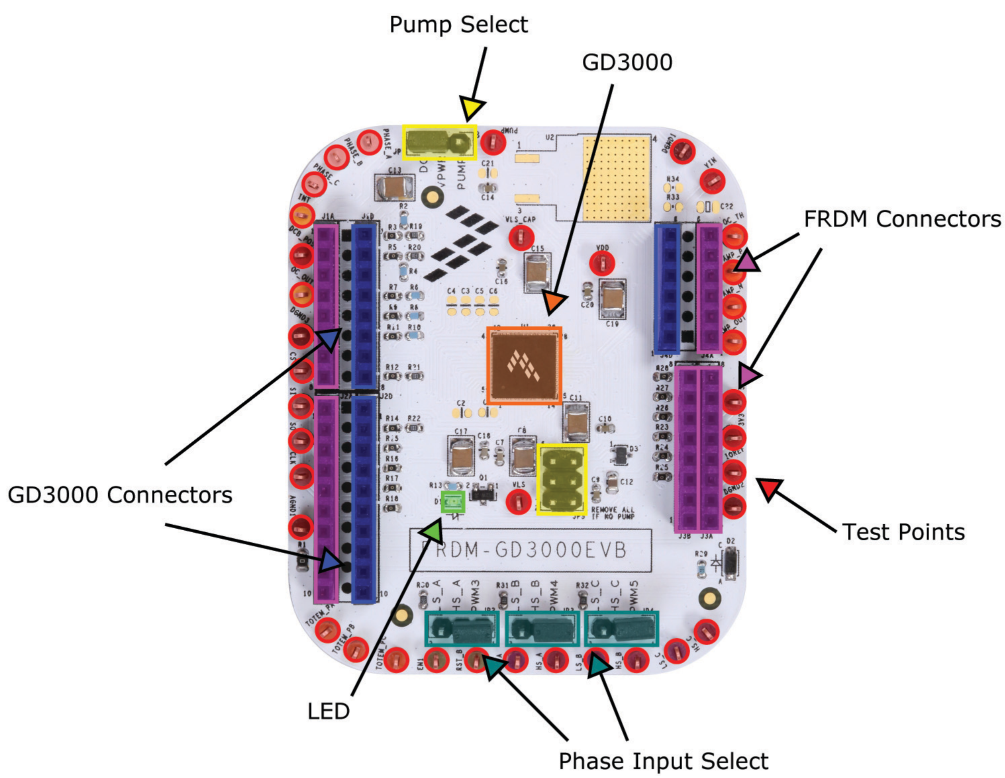

Figure 3. Board description

Table 2. Board description

Name	Description
FRDM Connectors	Connectors to attach to a compatible FRDM board
GD3000 Connectors	Connectors to attach to an FRDM-PWRSTG board
MC33812	Three Phase Field Effect Transistor Pre-driver
Jumpers	Jumpers for configuring the board for various modes of operation
Test points	Test points to probe various signals

3.6 LED display

The following LEDs are provided as visual output devices for the evaluation board:

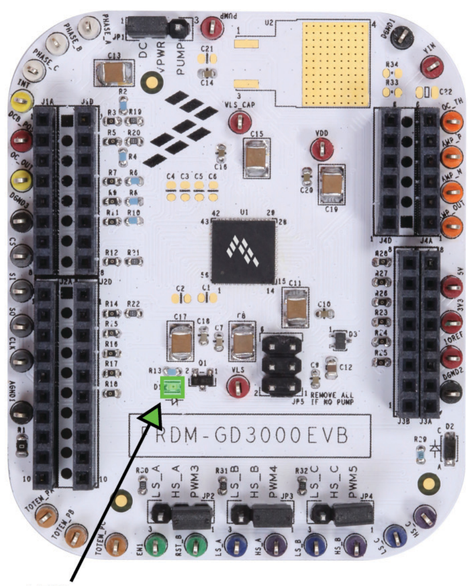

Figure 4. LED display

Table 3. LED display

Name	Description
D1	GREEN LED, indicates when V_{LS} is present (i.e. the device is on)

3.7 Jumper definitions

Figure 5 shows the jumper locations on the board.

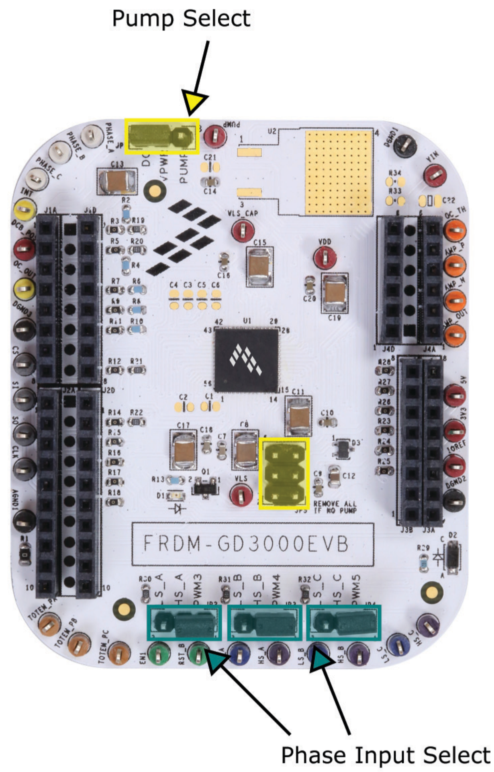

Figure 5. Board jumpers

The following table defines the evaluation board jumper positions and explains their functions. (The default settings are shown in blue.)

Table 4. Jumper definitions

Jumper	Description	Setting	Connection
JP1	VPWR Select	1-2	DCB_POS to VPWR
		2-3	PUMP to VPWR
JP2	Phase A Input Select	1-2	PA_HS_B to PWM3
		2-3	PA_HS_B to PA_LS
JP3	Phase B Input Select	1-2	PB_HS_B to PWM4
		2-3	PB_HS_B to PB_LS
JP4	Phase C Input Select	1-2	PC_HS_B to PWM5
		2-3	PC_HS_B to PC_LS
JP5	PUMP Select	1-2	PUMP in use (remove when PUMP is not used)
		3-4	PUMP in use (remove when PUMP is not used)
		5-6	PUMP in use (remove when PUMP is not used)

3.8 Input signal definition

The board has the following input signals used to drive the gate driver and relay feedback to the gate driver. Additional feedback signals may be present depending on which FRDM-PWRSTG board is used. Refer to the relevant FRDM-PWRSTG user guide.

Table 5. Input signals

Input Name	Description
EN	Logic signal input must be high to enable any gate drive output (from MCU)
RST_B	Reset input (from MCU)
CS	Chip Select input. It frames SPI commands and enables SPI port (from MCU)
MOSI	Input data for SPI port. Clocked on the falling edge of SCLK, MSB first (from MCU)
CLK	Clock for SPI port and typically is 3.0 MHz (from MCU)
OC_TH	Threshold of the overcurrent detector (from FRDM-PWRSTG)
AMP_P	Non-inverting input of the current-sensing amplifier (from FRDM-PWRSTG)
AMP_N	Inverting input of the current-sensing amplifier (from FRDM-PWRSTG)
PWM2	Active low input signal for PC_LS (or both PC_LS and PC_HS_B) (from MCU)
PWM1	Active low input signal for PB_LS (or both PB_LS and PB_HS_B) (from MCU)
PWM0	Active low input signal for PA_LS (or both PA_LS and PA_HS_B) (from MCU)
PWM3	Active low input signal for PA_HS_B (from MCU)
PWM4	Active low input signal for PB_HS_B (from MCU)
PWM5	Active low input signal for PC_HS_B (from MCU)
PA_HS_S	Source connection for Phase A high-side FET (from FRDM-PWRSTG)
PB_HS_S	Source connection for Phase B high-side FET (from FRDM-PWRSTG)
PC_HS_S	Source connection for Phase C high-side FET (from FRDM-PWRSTG)
PA_BOOT	Bootstrap capacitor for Phase A (from FRDM-PWRSTG)
PB_BOOT	Bootstrap capacitor for Phase B (from FRDM-PWRSTG)
PC_BOOT	Bootstrap capacitor for Phase C (from FRDM-PWRSTG)
PA_LS_S	Source connection for Phase A low-side FET (from FRDM-PWRSTG)
PB_LS_S	Source connection for Phase B low-side FET (from FRDM-PWRSTG)
PC_LS_S	Source connection for Phase C low-side FET (from FRDM-PWRSTG)

3.9 Output signal definition

The board has the following output signals which are used to communicate with an MCU board and a FRDM-PWRSTG accessory board which can drive a load, such as a brushless DC motor.

Table 6. Output signals

Output name	Description
INT	Interrupt pin output (to MCU)
OC_OUT	Totem pole digital output of the overcurrent comparator (to MCU)
TOTEM_PA	Totem pole output of Phase A comparator; this output is low when the voltage on PA_HS_S (source of high-side FET) is less than 50% of V_{SUP} (to MCU)
TOTEM_PB	Totem pole output of Phase B comparator; this output is low when the voltage on PB_HS_S (source of high-side FET) is less than 50% of V_{SUP} (to MCU)
TOTEM_PC	Totem pole output of Phase C comparator; this output is low when the voltage on PC_HS_S (source of high-side FET) is less than 50% of V_{SUP} (to MCU)
MISO	Output data for SPI port. Tri-state until CS becomes low (to MCU)
AMP_OUT	Output of the current-sensing amplifier (to FRDM-PWRSTG, then to MCU)
PC_LS_G	Gate drive for output Phase C low-side (to FRDM-PWRSTG)
PC_HS_G	Gate drive for output Phase C high-side (to FRDM-PWRSTG)
PB_LS_G	Gate drive for output Phase B low-side (to FRDM-PWRSTG)
PB_HS_G	Gate drive for output Phase B high-side (to FRDM-PWRSTG)
PA_LS_G	Gate drive for output Phase A low-side (to FRDM-PWRSTG)
PA_HS_G	Gate drive for output Phase A high-side (to FRDM-PWRSTG)

3.10 Test point definitions

The following test points, shown in Figure 6, provide access to various signals to and from the board.

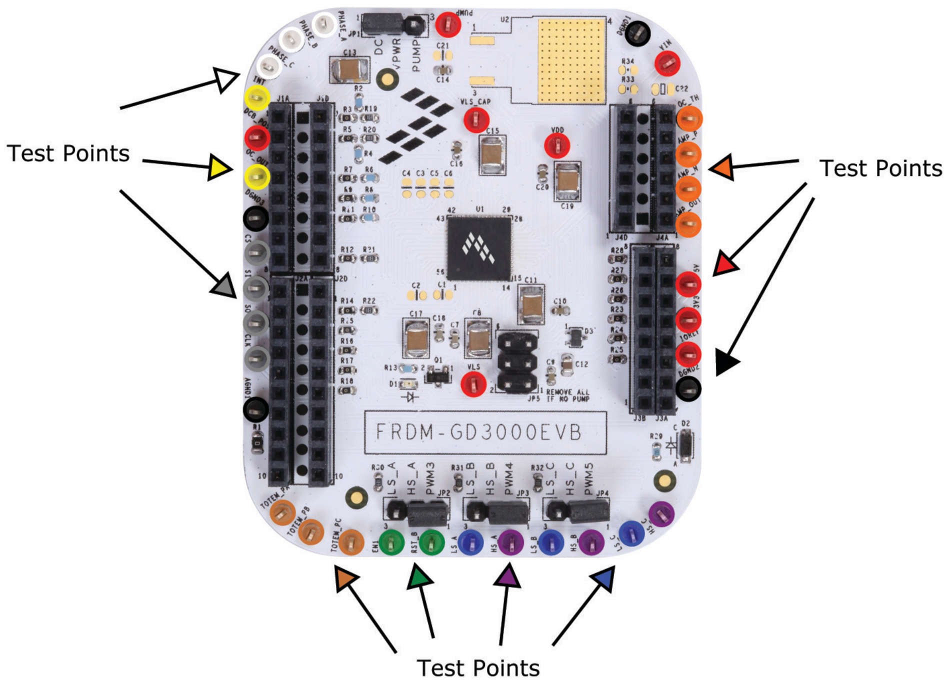

Figure 6. Test points

Table 7. Test point definitions

Test point name	Signal name	Description
VDD	VDD	VDD regulator output capacitor connection
VLS	VLS	VLS regulator output; power supply for the gate drives
VLS_CAP	VLS_CAP	VLS Regulator connection for additional output capacitor, providing low impedance supply source for low-side gate drive
IOREF	IOREF	IO reference from FRDM board
DCB_POS	DCB_POS	Power supply input for gate drives
PUMP	PUMP_VPWR	VPWR if external pump is used
VIN	VIN	Power supply for FRDM board
DGND1	GND	Ground
DGND2	GND	Ground
DGND3	GND	Ground

Table 7. Test point definitions (continued)

Test point name	Signal name	Description
AGND1	AGND	Analog ground from FRDM board
PHASE_A	PA_HS_S	Source connection for Phase A high-side FET (PHASE A output)
PHASE_B	PB_HS_S	Source connection for Phase B high-side FET (PHASE B output)
PHASE_C	PC_HS_S	Source connection for Phase C high-side FET (PHASE C output)
EN	EN	Logic signal input must be high (EN1 ANDed with EN2) to enable any gate drive output.
RST_B	RST_B	Reset input
INT	INT	Interrupt pin output
OC_OUT	OC_OUT	Totem pole digital output of the overcurrent comparator
OC_TH	OC_TH	Threshold of the overcurrent detector
CS	CS3_0	Chip Select input. It frames SPI commands and enables SPI port
SI	MOSI_0	Input data for SPI port. Clocked on the falling edge of SCLK, MSB first
SO	MISO_0	Output data for SPI port. Tri-state until CS becomes low
CLK	CLK_0	Clock for SPI port and typically is 3.0 MHz
TOTEM_PA	TOTEM_PA	Totem pole output of Phase A comparator; this output is low when the voltage on PA_HS_S (source of high-side FET) is less than 50% of VSUP
TOTEM_PB	TOTEM_PB	Totem pole output of Phase B comparator; this output is low when the voltage on PB_HS_S (source of high-side FET) is less than 50% of VSUP
TOTEM_PC	TOTEM_PC	Totem pole output of Phase C comparator; this output is low when the voltage on PC_HS_S (source of high-side FET) is less than 50% of VSUP
LS_A	PA_LS	Active high input logic signal enables the low-side driver for Phase A
LS_B	PB_LS	Active high input logic signal enables the low-side driver for Phase B
LS_C	PC_LS	Active high input logic signal enables the low-side driver for Phase C
HS_A	PA_HS_B	Active low input logic signal enables the high-side driver for Phase A
HS_B	PB_HS_B	Active low input logic signal enables the high-side driver for Phase B
HS_C	PC_HS_B	Active low input logic signal enables the high-side driver for Phase C
AMP_P	AMP_P	Non-inverting input of the current-sensing amplifier
AMP_N	AMP_N	Inverting input of the current-sensing amplifier
AMP_OUT	AMP_OUT	Output of the current-sensing amplifier

3.11 Screw terminal connections

The board does not have screw terminal connectors for the power supply and load. These connectors are found on the power stage board which must be stacked on top of this gate driver board. See related products for available power stage boards and their respective user guides.

3.12 Compatible FRDM boards

The following FRDM boards are guaranteed to be compatible with this evaluation board. If using a FRDM board not listed, check the pin assignments to make sure the FRDM board is compatible with this evaluation board.

Table 8. Compatible Freedom development boards

FRDM board name	Functionality
FRDM-K22F	Partial
FRDM-K64F	Partial
FRDM-K20D50M	Partial
FRDM-KE02Z	Partial
FRDM-KE02Z40M	Partial
FRDM-KE04Z	<none>
FRDM-KE06Z	Partial
FRDM-KL02Z	Partial
FRDM-KL03Z	Partial
FRDM-KL05Z	Partial
FRDM-KL25Z	Partial
FRDM-KL26Z	Partial
FRDM-KL27Z	Partial
FRDM-KL43Z	Partial
FRDM-KL46Z	Partial
FRDM-KV10Z	Full (1)
FRDM-KV31F	Full

Notes

1. On the FRDM-KV10Z, populate R64 with a 0 Ohm resister, replace R9 and R15 with 680 Ohm resistors, and set PTD1 high in software to disable the accelerometer.

3.13 Pin assignments

Table 9 provides information about the connectors and pin assignments of the FRDM-GD3000, FRDM-KL25Z, FRDM-KV10Z, and FRDM-KV31F. The FRDM-KL25Z is generally used as a Freedom SPI Dongle (FSD). It can also be used as a regular microcontroller, although with limited functionality. The FRDM-KV10Z and the FRDM-KV31F can be used as regular MCU boards and provide full functionality. On the FRDM-KV10Z, populate R64 with a 0 Ohm resister, replace R9 and R15 with 680 Ohm resistors, and set PTD1 high in software to disable the accelerometer.

Table 9. Arduino™ connector pin assignments (“A” suffix)

FRDM-GD3000			FRDM-KL25Z			FRDM-KV10Z			FRDM-KV31F		
Header	Pin	Name	Header	Pin	Port	Header	Pin	Port	Header	Pin	Port
J1A	1	INT	J1	2	PTA1	J1	2	PTD0	J1	2	PTE1
J1A	2	OC_OUT	J1	4	PTA2	J1	4	PTD1	J1	4	PTE0
J1A	3	<NC>	J1	6	PTD4	J1	6	–	J1	6	PTD5
J1A	4	TOTEM_PA	J1	8	PTA12	J1	8	PTE24	J1	8	PTE6
J1A	5	TOTEM_PB	J1	10	PTA4	J1	10	PTB0	J1	10	PTC13
J1A	6	TOTEM_PC	J1	12	PTA5	J1	12	PTE25	J1	12	PTA12
J1A	7	<NC>	J1	14	PTC8	J1	14	PTE29	J1	14	PTC3
J1A	8	EN	J1	16	PTC9	J1	16	PTC7	J1	16	PTC6

Table 9. Arduino™ connector pin assignments (“A” suffix) (continued)

FRDM-GD3000			FRDM-KL25Z			FRDM-KV10Z			FRDM-KV31F		
Header	Pin	Name	Header	Pin	Port	Header	Pin	Port	Header	Pin	Port
J2A	1	<reserved>	J2	2	PTA13	J2	2	PTD2	J2	2	PTA0
J2A	2	RST_B	J2	4	PTD5	J2	4	PTA4	J2	4	PTA1
J2A	3	CS	J2	6	PTD0	J2	6	PTD6	J2	6	PTC19
J2A	4	MOSI	J2	8	PTD2	J2	8	PTC6	J2	8	PTC18
J2A	5	MISO	J2	10	PTD3	J2	10	PTD3	J2	10	PTC17
J2A	6	CLK	J2	12	PTD1	J2	12	PTC5	J2	12	PTC16
J2A	7	GND	J2	14	GND	J2	14	GND	J2	14	GND
J2A	8	AREF	J2	16	VREFH	J2	16	AREF	J2	16	VREF
J2A	9	<reserved>	J2	18	PTE0	J2	18	PTB3	J2	18	PTC1
J2A	10	<reserved>	J2	20	PTE1	J2	20	PTB2	J2	20	PTC0
J3A	8	VIN	J3	16	P5-9V_VIN	J3	16	P5-9V_VIN	J3	16	P5-9V_VIN
J3A	7	GND	J3	14	GND	J3	14	GND	J3	14	GND
J3A	6	GND	J3	12	GND	J3	12	GND	J3	12	GND
J3A	5	5V	J3	10	P5V_USB	J3	10	P5V_USB	J3	10	P5V_USB
J3A	4	3V3	J3	8	P3V3	J3	8	P3V3	J3	8	P3V3
J3A	3	<NC>	J3	6	RESET/PTA20	J3	6	RST_TGTMCU_B	J3	6	RST_TGTMCU_B
J3A	2	IOREF	J3	4	P3V3	J3	4	P3V3	J3	4	P3V3
J3A	1	<NC>	J3	2	SDA_PTD5	J3	2	<NC>	J3	2	<NC>
J4A	6	<reserved>	J4	12	PTC1	J4	12	PTB2	J4	12	PTC10
J4A	5	<reserved>	J4	10	PTC2	J4	10	PTB3	J4	10	PTC11
J4A	4	<reserved>	J4	8	PTB3	J4	8	PTE21	J4	8	PTC0
J4A	3	<reserved>	J4	6	PTB2	J4	6	PTE20	J4	6	PTB11
J4A	2	<reserved>	J4	4	PTB1	J4	4	PTE16	J4	4	PTC9
J4A	1	<reserved>	J4	2	PTB0	J4	2	PTC0	J4	2	PTC8

Table 10. MCU connector pin assignments (“B” suffix)

FRDM-GD3000			FRDM-KL25Z			FRDM-KV10Z			FRDM-KV31F		
Header	Pin	Name	Header	Pin	Port	Header	Pin	Port	Header	Pin	Port
J1B	1	N/A	J1	1	PTC7	J1	1	PTE24	J1	1	PTC12
J1B	2	N/A	J1	3	PTC0	J1	3	PTD7	J1	3	PTA13
J1B	3	N/A	J1	5	PTC3	J1	5	PTE25	J1	5	PTC15
J1B	4	N/A	J1	7	PTC4	J1	7	PTD0	J1	7	PTC16
J1B	5	N/A	J1	9	PTC5	J1	9	PTD1	J1	9	PTC17
J1B	6	N/A	J1	11	PTC6	J1	11	PTB0	J1	11	PTE2
J1B	7	N/A	J1	13	PTC10	J1	13	PTE29	J1	13	PTE3
J2B	1	N/A	J2	1	PTC12	J2	1	PTE18	J2	1	<NC>
J2B	2	N/A	J2	3	PTC13	J2	3	PTB1	J2	3	<NC>
J2B	3	N/A	J2	5	PTC16	J2	5	PTE19	J2	5	<NC>
J2B	4	N/A	J2	7	PTC17	J2	7	PTE17	J2	7	<NC>
J2B	5	N/A	J2	9	PTA16	J2	9	PTE30	J2	9	<NC>
J2B	6	N/A	J2	11	PTA17	J2	11	PTB3	J2	11	<NC>
J2B	7	N/A	J2	13	PTE31	J2	13	PTC6	J2	13	<NC>

Table 10. MCU connector pin assignments (“B” suffix)

FRDM-GD3000			FRDM-KL25Z			FRDM-KV10Z			FRDM-KV31F		
Header	Pin	Name	Header	Pin	Port	Header	Pin	Port	Header	Pin	Port
J2B	8	N/A	J2	15	<NC>	J2	15	PTB0	J2	15	<NC>
J2B	9	N/A	J2	17	PTC6	J2	17	PTE29	J2	17	<NC>
J2B	10	N/A	J2	19	PTD7	J2	19	PTC7	J2	19	<NC>
J3B	8	PWM2	J3	15	PTE5	J3	15	PTC1	J3	15	PTC1
J3B	7	PWM1	J3	13	PTE4	J3	13	PTC2	J3	13	PTC2
J3B	6	PWM0	J3	11	PTE3	J3	11	PTC3	J3	11	PTC5
J3B	5	PWM3	J3	9	PTE2	J3	9	PTC4	J3	9	PTC4
J3B	4	PWM4	J3	7	PTB11	J3	7	PTD4	J3	7	PTD4
J3B	3	PWM5	J3	5	PTB10	J3	5	PTD5	J3	5	PTD5
J3B	2	N/A	J3	3	PTB9	J3	3	PTA1	J3	3	PTB18
J3B	1	N/A	J3	1	PTB8	J3	1	PTA2	J3	1	PTB19
J4B	6	N/A	J4	11	PTE30	J4	11	PTE30	J4	11	DAC0_OUT
J4B	5	N/A	J4	9	PTE29	J4	9	PTC5	J4	9	PTB21
J4B	4	N/A	J4	7	PTE23	J4	7	PTB2	J4	7	ADC1_DM0
J4B	3	N/A	J4	5	PTE22	J4	5	PTB3	J4	5	ADC0_DM0
J4B	2	N/A	J4	3	PTE21	J4	3	PTE21	J4	3	ADC0_DM1
J4B	1	N/A	J4	1	PTE20	J4	1	PTE20	J4	1	ADC0_DP1

Table 11. Gate drive connector pin assignments (“D” suffix)

FRDM-GD3000			FRDM-KL25Z			FRDM-KV10Z			FRDM-KV31F		
Header	**Pin**	**Name**	**Header**	**Pin**	**Port**	**Header**	**Pin**	**Port**	**Header**	**Pin**	**Port**
J1D	1	DCB_POS	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
J1D	2	DCB_POS	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
J1D	3	PA_HS_S	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
J1D	4	PB_HS_S	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
J1D	5	PC_HS_S	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
J1D	6	PA_BOOT	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
J1D	7	PB_BOOT	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
J1D	8	PC_BOOT	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
J2D	1	PC_LS_S	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
J2D	2	PC_LS_G	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
J2D	3	PC_HS_G	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
J2D	4	PB_LS_S	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
J2D	5	PB_LS_G	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
J2D	6	PB_HS_G	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
J2D	7	PA_LS_S	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
J2D	8	PA_LS_G	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
J2D	9	PA_HS_G	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
J2D	10	<NC>	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
J3D	8	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
J3D	7	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
J3D	6	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
J3D	5	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
J3D	4	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
J3D	3	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
J3D	2	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
J3D	1	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
J4D	6	OC_TH	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
J4D	5	AMP_P	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
J4D	4	AMP_N	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
J4D	3	AMP_OUT	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
J4D	2	<reserved>	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
J4D	1	<reserved>	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

4 Installing the software and setting up the hardware

4.1 General hardware setup

Figure 7 shows the typical setup of the FRDM-GD3000EVB system. The FRDM-GD3000EVB connects to the top of any compatible FRDM board. Any FRDM-PWRSTG (a power stage board specifically designed for use with the GD3000 evaluation board) attaches to the top of the evaluation board. A power supply (typically 12 V to 48 V) connects to the screw terminal J5 on the power stage board. The FRDM board connects to the PC via a USB cable. A BLDC load is connected to J6 on the power stage board.

The following procedure describes how to set up the hardware:

1. Solder the female headers into the top of the Freedom MCU board. If SPIGen is to be used, the FRDM-KL25Z must be used.
2. Connect the FRDM-GD3000EVB to the top of the Freedom MCU board.
3. Connect the FRDM-PWRSTG to the top of the FRDM-GD3000EVB.
4. Attach a load to the phase outputs (J6).
5. With the power supply OFF, attach it to the power input terminals (J5).
6. Connect the Freedom MCU board to the PC via the USB cable. To use SPIGen, the USB cable must be connected to the USBKL25Z port on the FRDM-KL25Z. Otherwise, in order to program the Freedom MCU board, the SDA port must be used.

Note: The Freedom MCU board must first be configured as a FSD or regular MCU board. See the following sections for setup details.

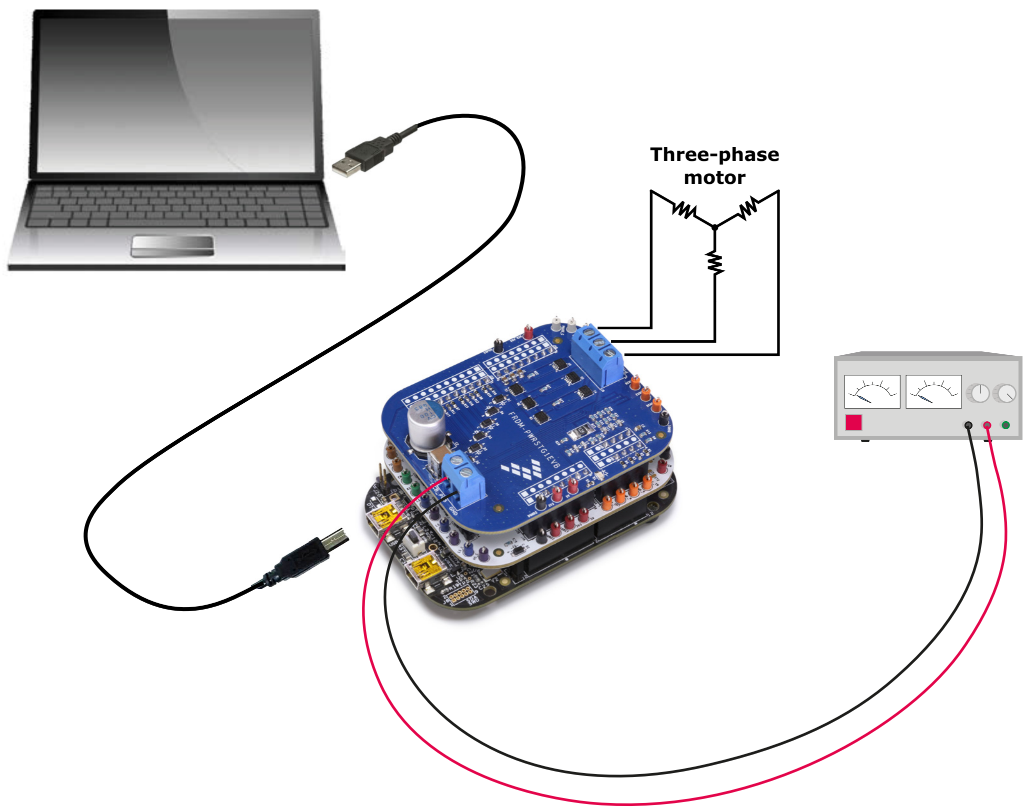

Figure 7. Hardware Configuration

4.2 Using the FSD

The FRDM-KL25Z provides an ideal support platform for the FRDM-GD3000EVB kit. In this configuration, the FRDM-KL25Z connects to a PC and allows the user—via the GUI—to control the inputs to the GD3000. However, SPIGen can only provide limited functionality. For more advanced evaluations, microcontroller code must be used. See Section 4.4 "Using MCU code", page 21.

4.2.1 Installing SPIGen

The latest version of SPIGen is designed to run on any Windows 8, Windows 7, Vista or XP-based operating system. To install the software:

1. Go to www.nxp.com/SPIGen and download the latest version of SPIGen.
2. Run the install program from the desktop. The Installation Wizard guides the user through the rest of the process.
3. Go to www.nxp.com/FRDM-GD3000EVB and download the SPIGen configuration file.

For additional information on using SPIGen, see the SPIGen 7 User Guide available at www.nxp.com/SPIGen

4.3 Preparing the FRDM-KL25Z for use as an FSD (Freedom SPI Dongle)

Because the FRDM-KL25Z board has access to the KL25Z microcontroller’s USB, SPI, and parallel ports, it can be configured to serve as an FSD for the FRDM-GD3000EVB evaluation board. The main function of the FRDM-KL25Z in this configuration is to provide the evaluation board with a parallel port to communicate via a USB port with the SPIGen GUI on a PC.

NOTE:

If using SPIGen with the FRDM-GD3000EVB evaluation board, configure the FRDM-KL25Z as an FSD.

A generic FRDM-KL25Z board does not have firmware installed to support the FRDM-GD3000EVB evaluation board. Prior to connecting the KL25Z to the evaluation board:

- Install the FRDM-KL25Z board driver onto the PC. This causes the board to appear on the PC as a mass storage device (MSD) and enables installing microcode by dragging and dropping to the MSD icon.
- Download the OpenSDA firmware onto the KL25Z. This enables OpenSDA functionality supporting firmware downloading and debugging.
- Install the FRDM-GD3000EVB evaluation board firmware onto the KL25Z. This provides the communication interface between SPIGen and the MCU on the evaluation board.

4.3.1 Installing the FRDM-KL25Z board driver

1. Connect the Standard A end of the USB cable to the PC. The board draws power through the USB port. While holding down the FRDM-KL25Z's Reset button, attach the Mini-B end of the USB cable to the board's OpenSDA USB port (labelled **SDA** on the board). The small LED above the OpenSDA port flashes green when the board is properly connected.
2. When properly connected through the OpenSDA port, the FRDM-KL25Z automatically loads the board driver. Subsequently, a Mass Storage Device (MSD) icon named "BOOTLOADER" appears as a device on the PC.

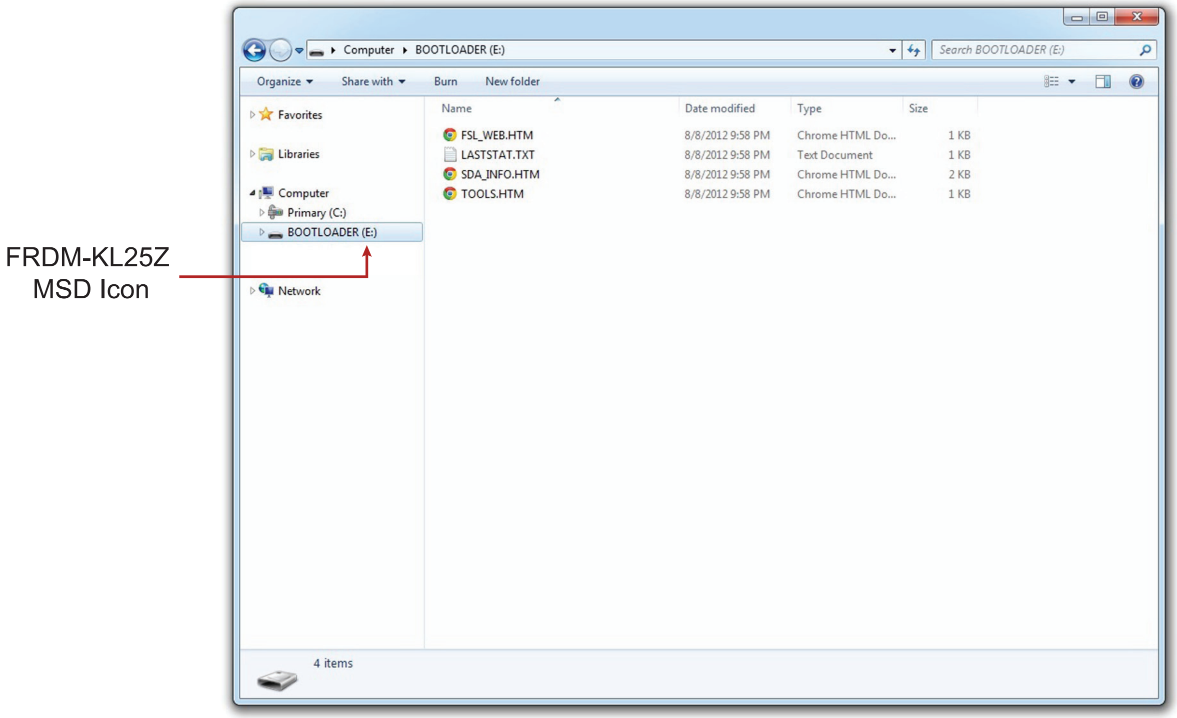

Figure 8. FRDM-KL25Z board driver installed

4.3.2 Downloading the OpenSDA firmware

1. Go to the P&E Microcomputer Systems website at http://www.pemicro.com/opensda.
2. Login to the P&E Micro user account. If no account, create a new one to access the firmware.
3. Search for the **OpenSDA Firmware** panel, then click to download the P&E Micro zip file.
4. Open the zip file and locate the OpenSDA firmware file named **MSD-DEBUG-FRDM-KL25Z_Pemico_vxxx.SDA**. Unzip this file to the PC.
5. Verify the USB cable is connected to the OpenSDA USB port on the KL25Z.
6. Drag and drop **MSD-DEBUG-FRDM-KL25Z_Pemicro_vxxx.SDA** to the KL25Z BOOTLOADER icon on the PC.
7. Unplug the USB mini-plug, then re-insert the plug into the OpenSDA port. The green OpenSDA LED remains on and an MSD device named FRDM-KL25Z appears on the PC.

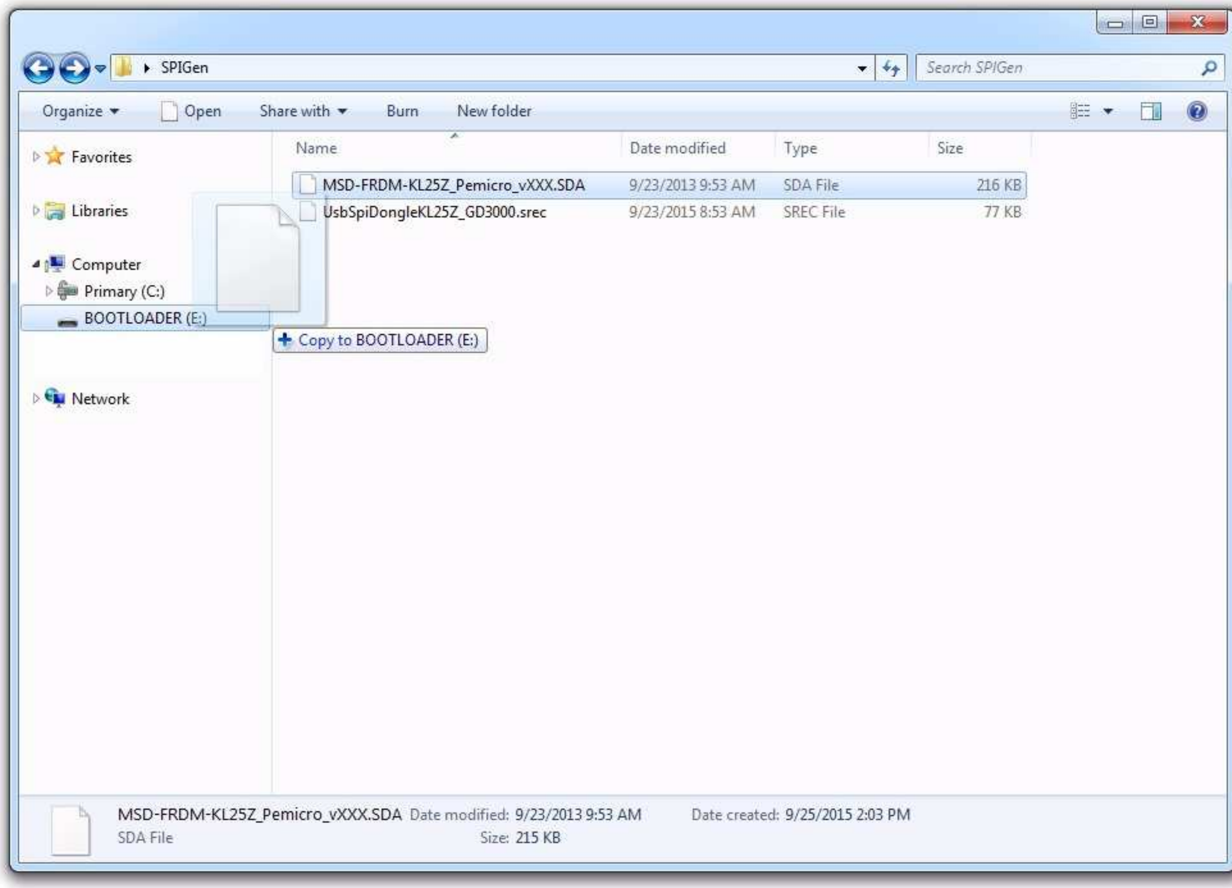

Figure 9. Downloading OpenSDA firmware

4.3.3 Installing the FRDM-GD3000EVB evaluation board Firmware

1. Go to evaluation board tool summary page at www.nxp.com/FRDM-GD3000EVB. Click on **Jump Start Your Design**. Download the .srec file **UsbSpiDongleKL25Z_GD3000**.
2. Assure that the USB cable is connected to the OpenSDA USB port on the KL25Z.
3. Drag and drop the .srec file onto the FRDM-KL25Z icon that appears on your PC as a Mass Storage Device named **FRDM-KL25Z**. The microcode automatically installs on the FRDM-KL25Z board's embedded flash memory The flashing green LED above the OpenSDA port indicates that the download is in process. When the firmware has been successfully installed, the green LED stops flashing and remains on.
4. To begin communicating with SPIGen, move the USB mini-plug from the KL25Z's OpenSDA port to the KL25Z USB port.

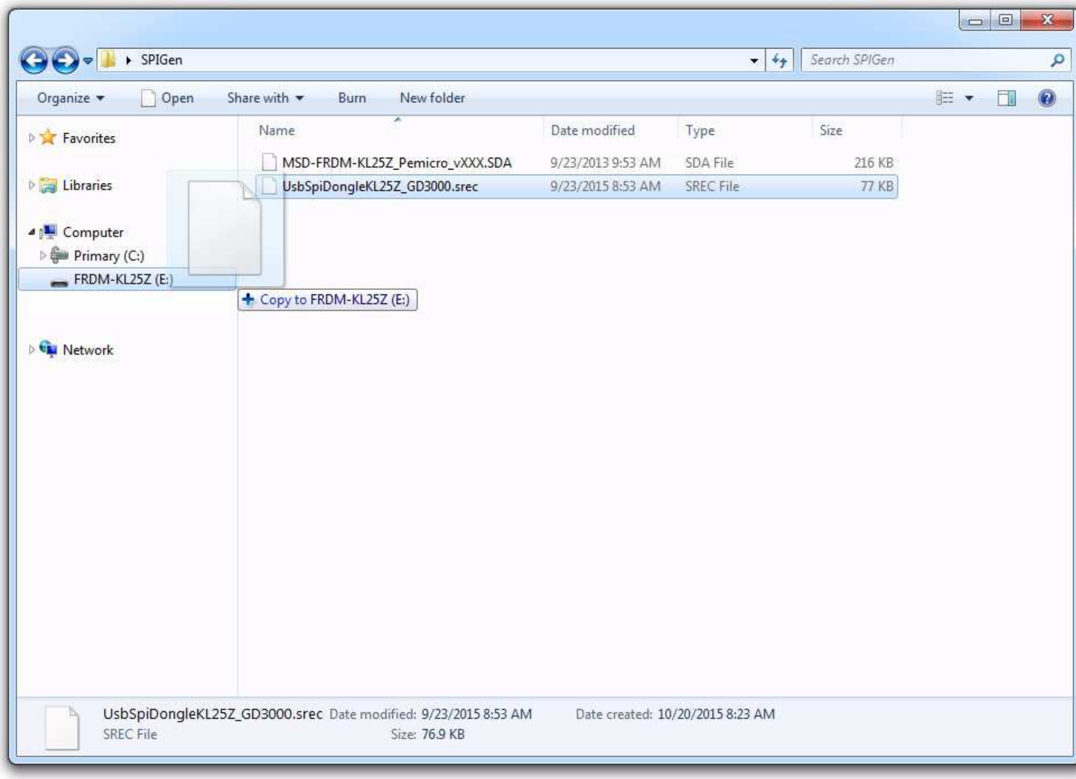

Figure 10. Download the FRDM-GD3000EVB evaluation board .srec File

4.4 Using MCU code

4.4.1 Installing the IDE

Install the preferred IDE (e.g. Codewarrior, Kinetis Design Studio, etc.) on the PC or use a web-based compiler (e.g. mbed). Use the compiler to program the MCU.

4.4.2 Configuring the FRDM-KL25Z as an MCU board

1. Connect the Standard A end of the USB cable to the PC. The board draws power through the USB port. While holding down the FRDM-KL25Z’s Reset button, attach the Mini-B end of the USB cable to the board’s OpenSDA USB port (labelled **SDA** on the board). The small LED above the OpenSDA port flashes green when the board is properly connected.
2. When properly connected through the OpenSDA port, the FRDM-KL25Z automatically loads the board driver. Subsequently, a Mass Storage Device (MSD) icon named “BOOTLOADER” appears as a device on the PC.

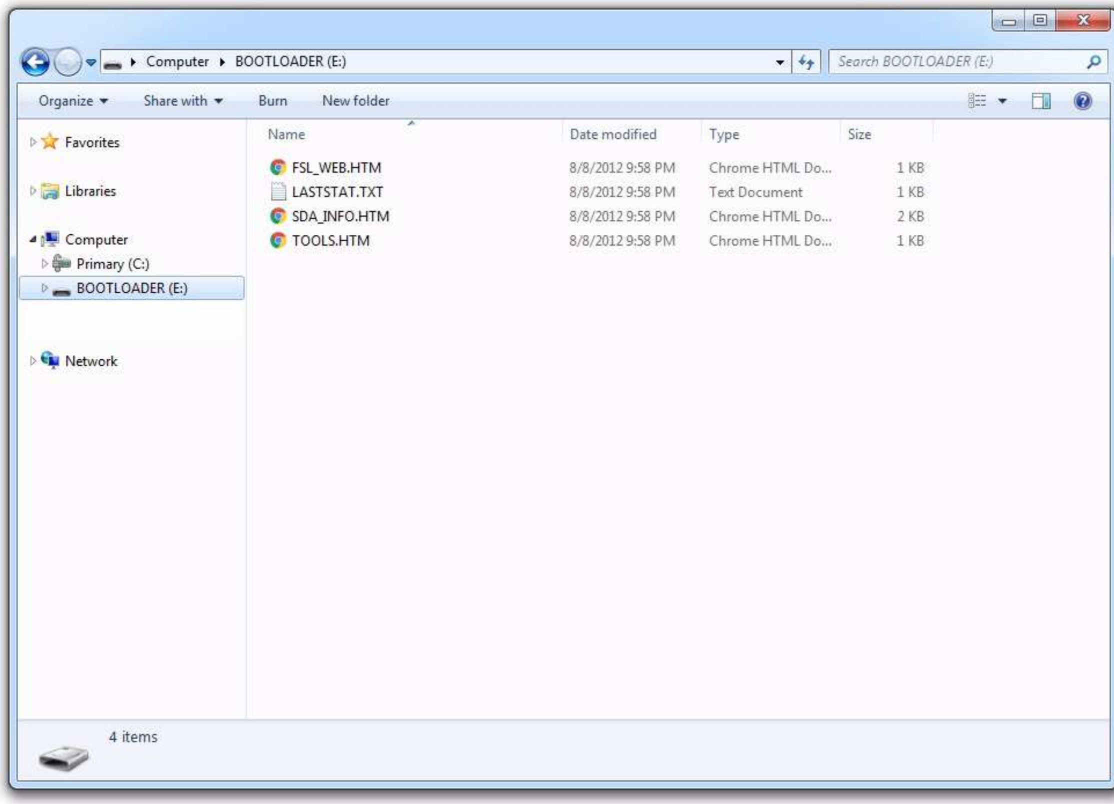

Figure 11. FRDM-KL25Z board driver installed

1. Go to the P&E Microcomputer Systems website at http://www.pemicro.com/opensda.
2. Login to the P&E Micro user account. When there is no account, create one to access the firmware.
3. Search for the **OpenSDA Firmware** panel, then click to download the P&E Micro zip file.
4. Open the zip file and locate the OpenSDA firmware file named **MSD-DEBUG-FRDM-KL25Z_Pemico_vxxx.SDA**. Unzip this file to the PC.
5. Assure the USB cable is connected to the OpenSDA USB port on the KL25Z.
6. Drag and drop **MSD-DEBUG-FRDM-KL25Z_Pemicro_vxxx.SDA** to the KL25Z BOOTLOADER icon on the PC.
7. Unplug the USB mini-plug, then re-insert the plug into the OpenSDA port. The green OpenSDA LED remains on and an MSD device named FRDM-KL25Z appears on the PC.

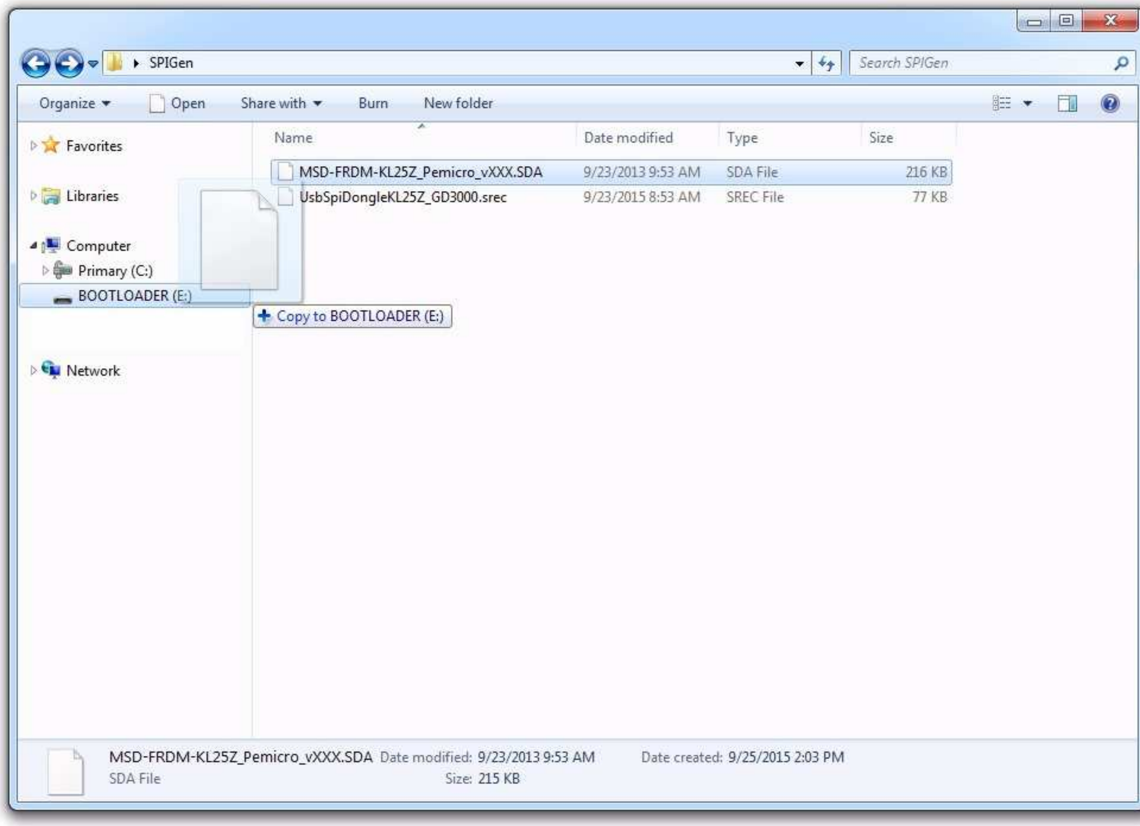

Figure 12. Downloading OpenSDA firmware

5 Evaluation board examples

The evaluation board is designed to work in conjunction with many of NXP's FRDM boards and allows several different ways of controlling the inputs to the evaluation board. The setup for these enablement boards is described in Section 4.1 "General hardware setup", page 17. The following section provides a simple example using SPIGen.

5.1 SPIGen example

The example is NOT tuned for a motor. It simply introduces the user to a limited set of functions of the GD3000. While other loads may be used for this example, it is specifically designed to be used with an LED configuration, as shown in Figure 13. The LEDs indicate which direction the current flows.

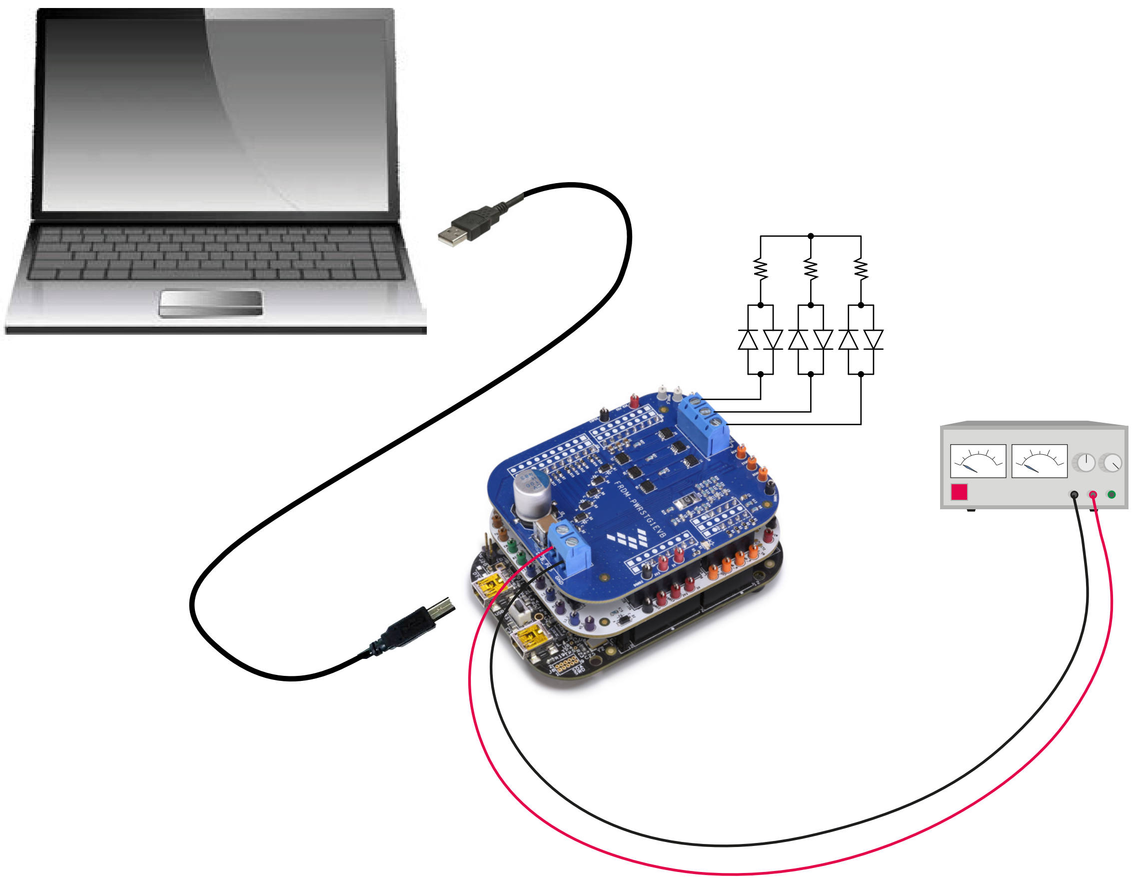

Figure 13. Example configuration

5.2 Setting up SPIGen to use with the GD3000

To use SPIGen with the GD3000, follow these instructions:

1. Plug the USB mini-plug into the USBKL25Z port on the FRDM-KL25Z.
2. Run the SPIGen program, previously installed. SPIGen opens to the page shown in Figure 14.

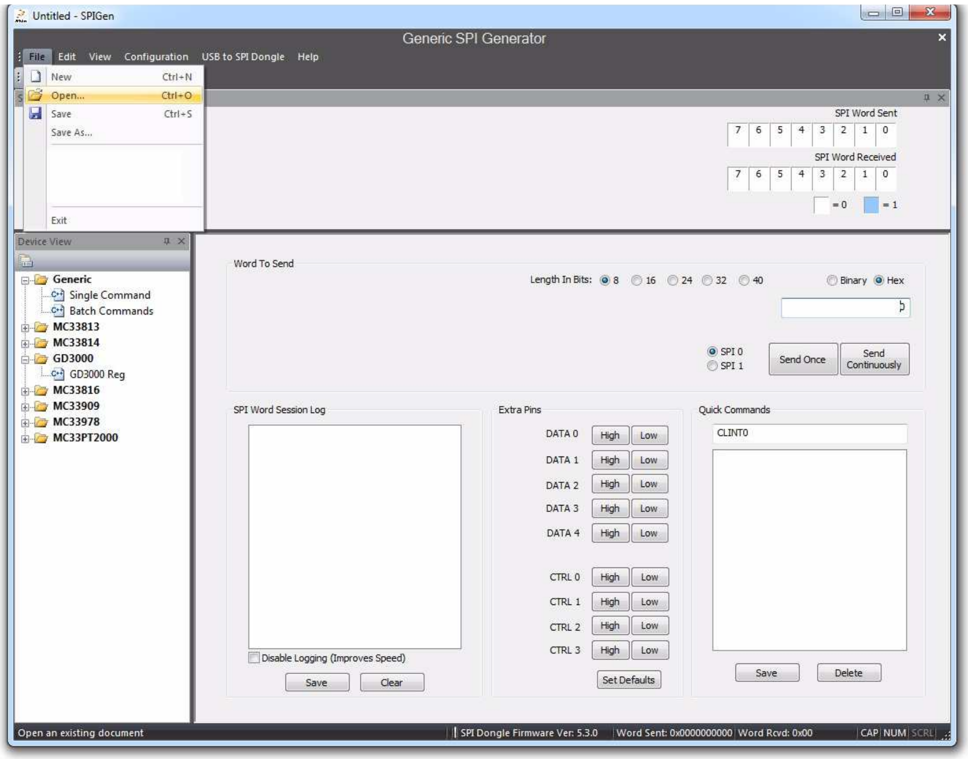

Figure 14. Generic SPIGen Tab

3. Click **File** -> **Open** and open the **FRDM-GD3000EVB.spi** file.