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FXOS8700CQ

6-axis sensor with integrated linear accelerometer and magnetometer

Rev. 7.0 - 22 March 2016 **Data sheet: Technical data**

1. General description

FXOS8700CQ is a small, low-power, 3-axis, linear accelerometer and 3-axis, magnetometer combined into a single package. The device features a selectable I²C or *point-to-point* SPI serial interface with 14-bit accelerometer and 16-bit magnetometer ADC resolution along with smart-embedded functions. FXOS8700CQ has dynamically selectable acceleration full-scale ranges of ±2 *g*/±4 *g*/±8 *g* and a fixed magnetic measurement range of ±1200 µT. Output data rates (ODR) from 1.563 Hz to 800 Hz are selectable by the user for each sensor. Interleaved magnetic and acceleration data is available at ODR rates of up to 400 Hz. FXOS8700CQ is available in a plastic QFN package and it is guaranteed to operate over the extended temperature range of –40 °C to +85 °C.

2. Features and benefits

- Complete 6-axis, e-compass hardware solution
- 1.95 V to 3.6 V VDD supply voltage, 1.62 V to 3.6 V VDDIO voltage
- ±2 *g*/±4 *g*/±8 *g* dynamically selectable acceleration full-scale range
- ±1200 µT magnetic sensor full-scale range
- Output data rates (ODR) from 1.563 Hz to 800 Hz for each sensor, and up to 400 Hz when operated in hybrid mode with both sensors active
- Low noise: < 126 µg/√Hz acceleration noise density at 200-Hz bandwidth, < 100 nT/√Hz magnetic noise density at 100-Hz bandwidth
- 14-bit ADC resolution for acceleration measurements
- 16-bit ADC resolution for magnetic measurements
- Low power: 240 µA current consumption at 100 Hz, and 80 µA at 25 Hz with both sensors active
- Embedded programmable acceleration event functions
  - Freefall and motion detection
  - Transient detection
  - Vector-magnitude change detection
  - Pulse and tap detection (single and double)
  - Orientation detection (portrait/landscape)
- Embedded programmable magnetic event functions
  - Threshold detection
  - Vector-magnitude change detection
  - Autonomous magnetic min/max detection
  - Autonomous hard-iron calibration

- Programmable automatic ODR change using auto-wake and return-to-sleep functions to save power. This function works with both magnetic and acceleration event interrupt sources.
- 32-sample FIFO for acceleration data only
- Integrated accelerometer self-test function

3. Applications

- Security: motion detection, door opening, smart home applications, robotics, and unmanned aerial vehicles (UAVs) with electronic compass (e-compass) function.
- Medical applications: patient monitoring, fall detection, and rehabilitation
- E-compass in mobile devices, tablets, and personal navigation devices
- User interface (menu scrolling by orientation change, tap detection for button replacement)
- Orientation detection (portrait/landscape: up/down, left/right, back/front orientation identification)
- Augmented reality (AR), gaming, and real-time activity analysis (pedometry, freefall, and drop detection for hard disk drives and other devices)
- Power management for mobile devices using inertial and magnetic event detection
- Wearable devices: motion detection, activity monitoring, sports monitoring, context awareness, and shock and vibration monitoring (mechatronic compensation, shipping, and warranty usage logging)

4. Ordering information

Table 1. Ordering information

Part number	Temperature range	Package description	Shipping
FXOS8700CQR1	–40 °C to +85 °C	QFN	Tape and reel

5. Block diagram

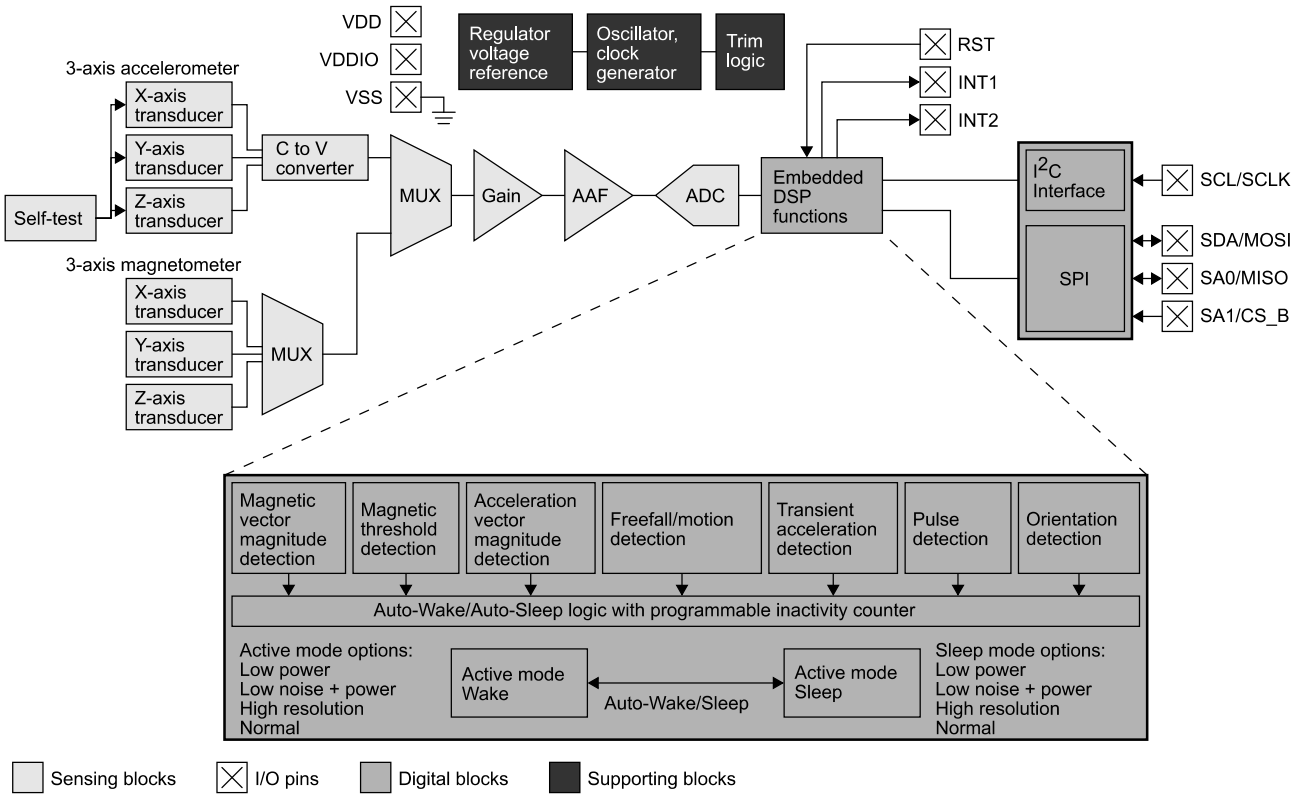


Fig 1. Block diagram

6. Pinning information

6.1 Pinning

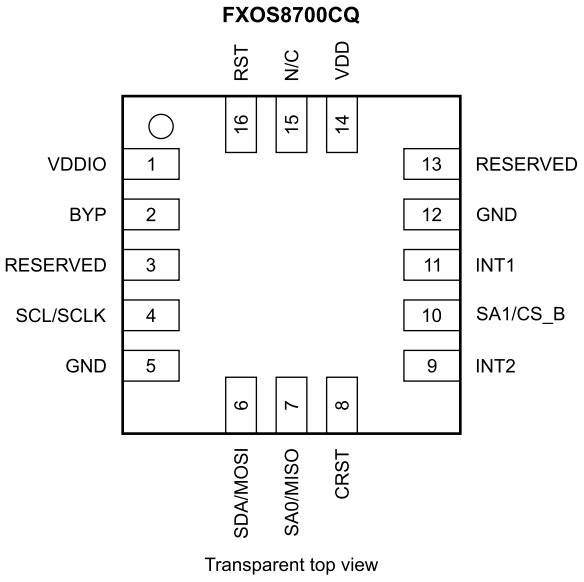


Fig 2. Pin configuration

6.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
VDDIO	1	Interface supply voltage
BYP	2	Internal regulator output bypass capacitor connection
Reserved	3	Test reserved, connect to GND
SCL/SCLK	4	I^2C serial clock/SPI clock[1]
GND	5	Ground
SDA/MOSI	6	I^2C serial data/SPI master out, slave in[1][2]
SA0/MISO	7	I^2C address selection bit 0/SPI master in, slave out[1][2][3]
Crst	8	Magnetic reset capacitor
INT2	9	Interrupt 2
SA1/CS_B	10	I^2C address selection bit 1/SPI chip select (active low)[2][3]
INT1	11	Interrupt 1
GND	12	Ground
Reserved	13	Test reserved, connect to GND
VDD	14	Sensor supply voltage
N/C	15	Not connected internally
RST[2]	16	Reset input, active high. Connect to GND if unused

[1] Refer to Section 10.2.1 regarding point-to-point SPI operation.

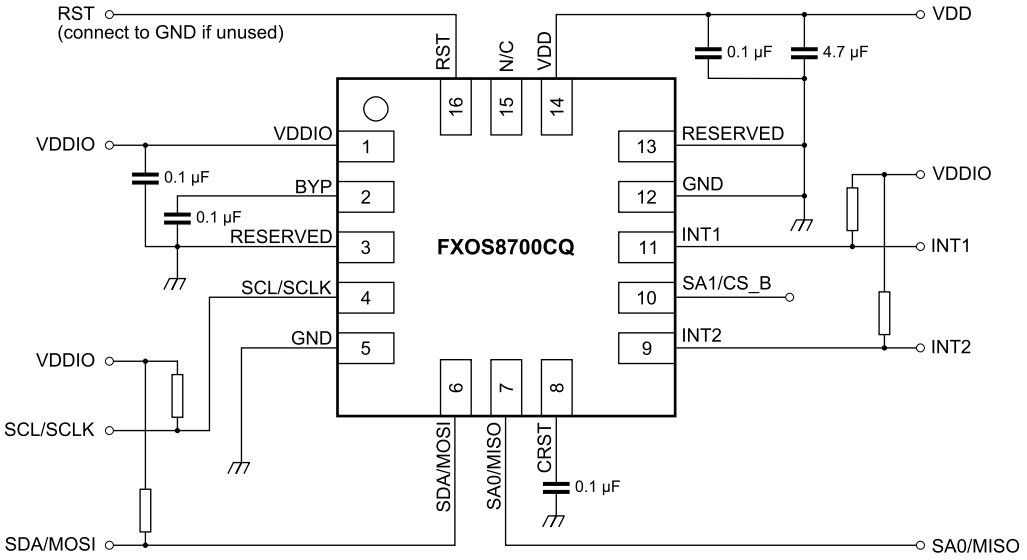
[2] Refer to Section 10.2.3 regarding SPI bus requirements during 1 ms period following a reset

[3] Refer to Table 11 for I^2C address options selectable using the SA0 and SA1 pins.

7. Electrical connections

Device power is supplied through the VDD pin. Power supply decoupling capacitors (100 nF ceramic plus 4.7 μF bulk) should be placed as close as possible to pin 14 of the device. The digital interface supply voltage (VDDIO) should be decoupled with a 100 nF ceramic capacitor placed as close as possible to pin 1 of the device.

The digital control signals SCL, SDA, SA0, SA1, and RST are not tolerant of voltages exceeding VDDIO + 0.3 V. If VDDIO is removed, these pins will clamp any logic signals through their internal ESD protection diodes. The function and timing of the two interrupt pins (INT1 and INT2) are user programmable through the I^2C/SPI interface. The SDA and SCL I^2C connections are open drain and therefore require a pullup resistor as shown in the application diagram in Figure 3. The INT1 and INT2 pins may also be configured for open-drain operation. If they are configured for open drain, external pullup resistors are required.



(1) Pullup resistors on SCL/SCLK and SDA/MOSI are not required if the device is operated in SPI Interface mode.

(2) Pullup resistors on INT1 and INT2 are not required if these pins are configured for push-pull (default) operation.

Fig 3. Electrical connection

7.1 Orientation

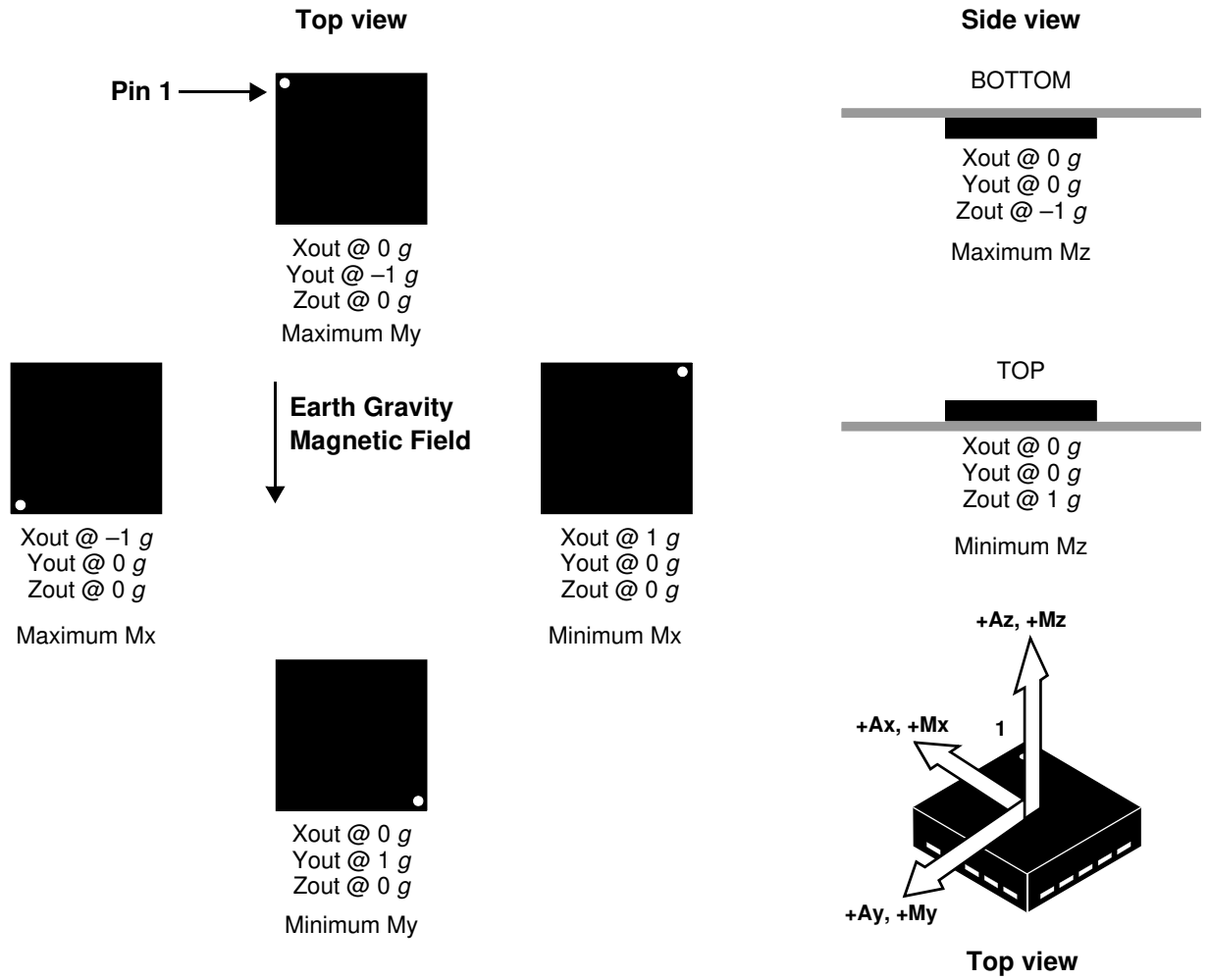


Fig 4. Product orientation and axis orientation

8. Terminology

8.1 Sensitivity

Sensitivity is represented in mg/LSB for the accelerometer and µT/LSB for the magnetometer. The magnetometer sensitivity is fixed at 0.1 µT/LSB. The accelerometer sensitivity changes with the full-scale range selected by the user. Accelerometer sensitivity is 0.244 mg/LSB in 2 *g* mode, 0.488 mg/LSB in 4 *g* mode, and 0.976 mg/LSB in 8 *g* mode.

8.2 Zero-*g* and zero-flux offset

For the accelerometer, zero-*g* offset describes the deviation of the output values from the ideal values when the sensor is stationary. With an accelerometer stationary on a level horizontal surface, the ideal output is 0 *g* for the X and Y axes, and 1 *g* for the Z-axis. The

deviation of each output from the ideal value is called zero-*g* offset. Offset is to some extent a result of stress on the sensor, and therefore, can slightly change after mounting the sensor onto a printed circuit board or exposing it to extensive mechanical stress. For the magnetometer, zero-flux offset describes the deviation of the output signals from zero when the device is shielded from external magnetic field sources (that is, inside a zero-Gauss chamber).

8.3 Self-test

Self-test can be used to verify the transducer and signal chain functionality without the need to apply an acceleration stimulus. When the accelerometer self-test is activated, an electrostatic actuation force is applied to the sensor, simulating a small acceleration. In this case the sensor X, Y, and Z outputs will exhibit a change in DC levels related to the selected full-scale range (sensitivity). When self-test is activated, the device output level is given by the algebraic sum of the signals produced by the acceleration acting on the sensor and by the electrostatic self-test force.

9. Device characteristics

9.1 Accelerometer mechanical characteristics

Table 3. Accelerometer mechanical characteristics @ VDD = 2.5 V, VDDIO = 1.8 V T = 25 °C unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
FS_{ACC}	Measurement range	±2 *g* mode	[1]	-	±2	-	g
		±4 *g* mode		-	±4	-	
		±8 *g* mode		-	±8	-	
SEN_{ACC}	Sensitivity	±2 *g* mode		-	4096	-	LSB/*g*
				-	0.244	-	mg/LSB
		±4 *g* mode		-	2048	-	LSB/*g*
				-	0.488	-	mg/LSB
		±8 *g* mode		-	1024	-	LSB/*g*
				-	0.976	-	mg/LSB
TCS_{ACC}	Sensitivity change with temperature	±2 *g*, ±4 *g*, ±8 *g* modes	[1]	-	±0.01	-	%/°C
$SEN\text{-}TOL_{ACC}$	Sensitivity accuracy			-	±2.5	-	$\%SEN_{ACC}$
OFF_{ACC}	Zero-*g* level offset accuracy	±2 *g*, ±4 *g*, ±8 *g* modes	[2]	-	±20	-	mg
$OFF_{ACC\text{-}PBM}$	Zero-*g* level offset accuracy post-board mount	±2 *g*, ±4 *g*, ±8 *g* modes	[4]	-	±30	-	mg
TCO_{ACC}	Zero-*g* level change versus temperature	–40 °C to 85 °C	[1]	-	±0.2	-	mg/°C
NL_{ACC}	Nonlinearity (deviation from straight line)	Over ±1 *g* range normal mode	[5][6]	-	±0.5	-	$\%FS_{ACC}$
$STOC_{ACC}$	Self-test output change		[7]				LSB
		±2 *g* mode, X-axis		+192	-	-	
		±2 *g* mode, Y-axis		+270	-	-	
		±2 *g* mode, Z-axis		+1275	-	-	

Table 3. Accelerometer mechanical characteristics @ VDD = 2.5 V, VDDIO = 1.8 V T = 25 °C unless otherwise noted. - *¶continued*

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
ND_{ACC}	Output noise density, normal mode	ODR = 400 Hz, normal mode	[4][7]	-	126	-	µg/√Hz
		ODR = 400 Hz, low-noise mode	[1]	-	99	-	µg/√Hz
T_{OP}	Operating temperature range			–40	-	+85	°C

[1] Dynamic range is limited to ±4 *g* when in the low-noise mode.

[2] Before board mount.

[3] Post-board mount offset specifications are based on a 2-layer PCB design.

[4] Evaluation only.

[5] After post-board mount corrections for sensitivity, cross axis and offset. Refer to NXP application note AN4399 for more information.

[6] Self-test is only exercised along one direction for each sensitive axis.

[7] Measured using earth's gravitational field (1 *g*) with the device oriented horizontally (+Z axis up) and stationary.

9.2 Magnetometer magnetic characteristics

Table 4. Magnetometer magnetic characteristics @ VDD = 2.5 V, VDDIO = 1.8 V T = 25 °C unless otherwise noted.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
FS_{MAG}	Measurement range	-		±1200	-	-	µT
SEN_{MAG}	Sensitivity	-		-	0.1	-	µT/LSB
TCS_{MAG}	Sensitivity change versus temperature	-		-	±0.1	-	%/°C
OFF_{MAG}	Zero-flux offset accuracy	-	[1]	-	±10	-	µT
TCO_{MAG}	Zero-flux offset change with temperature	-		-	±0.8	-	µT/°C
$HYST_{MAG}$	Hysteresis	-	[2][3]	-	±0.5	-	$\%FS_{MAG}$
NL_{MAG}	Nonlinearity		[3]				
	Deviation from best-fit straight line	-		-	±1	-	$\%FS_{MAG}$
-	Temperature sensor sensitivity	-		-	0.96	-	°C/LSB
$Noise_{MAG}$	Magnetometer output noise	ODR = 800 Hz, OSR = 2		-	1.5	-	µT-rms
		ODR = 400 Hz, OSR = 4		-	1.2	-	
		ODR = 200 Hz, OSR = 8		-	0.85	-	
		ODR = 100 Hz, OSR = 16		-	0.6	-	
		ODR = 50 Hz, OSR = 32		-	0.5	-	
		ODR = 12.5 Hz, OSR = 128		-	0.35	-	
		ODR = 6.25 Hz, OSR = 256		-	0.3	-	
		ODR = 1.56 Hz, OSR = 1024		-	0.3	-	
T_{OP}	Operating temperature range	-		–40	-	+85	°C

[1] After m-cell has been factory trimmed.

[2] Hysteresis is measured by sweeping the applied magnetic field from –1000 µT to 1000 µT and then back to –1000 µT. The difference in the two readings at –1000 µT divided by the swept field range is the hysteresis figure, expressed in % of the full-scale range (FS_{MAG}).

[3] Tested over a ±1000 µT measurement range.

9.3 Hybrid characteristics

Table 5. Hybrid characteristics @ VDD = 2.5 V, VDDIO = 1.8 V T = 25 °C unless otherwise noted.

Symbol	Rating	Value	Unit	Symbol	Rating
ODR_{max}	Maximum output data rate in hybrid mode	-	400	-	Hz
T_{OP}	Operating temperature range	–40	-	+85	°C
BW	Output data bandwidth	-	ODR/2	-	Hz

9.4 Electrical characteristics

Table 6. Electrical characteristics @ VDD = 2.5 V, VDDIO = 1.8 V T = 25 °C unless otherwise noted.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VDD	Supply voltage	-	1.95	2.5	3.6	V
VDDIO	Interface supply voltage	-	1.62	1.8	3.6	V
$IDD_{ACC-LPM}$	Supply current	Low-power acceleration mode				µA
		ODR = 12.5 Hz	-	8	-	
		ODR = 100 Hz	-	35	-	
		ODR = 400 Hz	-	130	-	
IDD_{ACC-NM}	Supply current	Normal acceleration mode				µA
		ODR = 50 Hz	-	35	-	
		ODR = 200 Hz	-	130	-	
		ODR = 800 Hz	-	240	-	
$IDD_{ACC+MAG}$	Supply current	Hybrid mode				µA
		ODR = 200 Hz Accelerometer OSR = 4 Magnetometer OSR = 2	-	440	-	
		ODR = 100 Hz Accelerometer OSR = 4 Magnetometer OSR = 2	-	240	-	
		ODR = 25 Hz Accelerometer OSR = 4 Magnetometer OSR = 2	-	80	-	
IDD_{MAG}	Supply current	Magnetic mode				µA
		ODR = 400 Hz, OSR = 2	-	575	-	
		ODR = 12.5 Hz, OSR = 2	-	40	-	
IDD_{BOOT}	Supply current during boot sequence	0.9 ms max duration using recommended regulator bypass capacitor, VDD = 2.5 V	-	-	-	3
C_{BYP}, C_{RST}	Value of capacitors on BYP and magnetic reset pins	–40 °C to 85 °C	75	100	470	nF
IDD_{STBY}	Supply current	Standby mode @ 25 °C	-	2	-	µA
IDD_{STBY}	Supply current	Over-temperature range, standby mode	-	-	10	µA

Table 6. Electrical characteristics @ VDD = 2.5 V, VDDIO = 1.8 V T = 25 °C unless otherwise noted. *- ¶continued -*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VIH_{RST}	Digital high-level input voltage, RST pin	-	1.04	-	-	V
VIL_{RST}	Digital low-level input voltage, RST pin	-	-	-	0.68	V
VIH	Digital high-level input voltage, SCL, SDA, SA0, and SA1 pins	-	0.75*VDDIO	-	-	V
VIL	Digital low-level input voltage, SCL, SDA, SA0, and SA1 pins	-	-	-	0.3*VDDIO	V
VOH	High-level output voltage, INT and INT2 pins	I_O = 500 µA	0.9*VDDIO	-	-	V
VOL	Low-level output voltage, INT1 and INT2 pins	I_O = 500 µA	-	-	0.1*VDDIO	V
VOL_{SDA}	Low-level output voltage, SDA pin	I_O = 500 µA	-	-	0.1*VDDIO	V
	SCL and SDA pin leakage	25 °C	-	1.0	-	nA
		–40 °C to 85 °C	-	4.0	-	
	SCL and SDA pin capacitance	-	-	3	-	pf
	VDD rise time	-	0.001	-	1000	ms
T_{BOOT}	Boot time	- [1]	-	-	1000	µs
$T_{POR \rightarrow ACT}$	Turn-on time 1	- [2]	-	2/ODR + 2	-	ms
$T_{STBY \rightarrow ACT}$	Turn-on time 2	- [3]	-	2/ODR + 1	-	ms
T_{OP}	Operating temperature range	-	–40	-	+85	°C

[1] Time from VDDIO on and VDD > VDD min until I^2C/SPI interface ready for operation.

[2] Time to obtain valid data from power-down mode to active mode.

[3] Time to obtain valid data from standby mode to active mode.

Table 7. IDD (µA) table versus operating modes (VDD + VDDIO), VDD = VDDIO = 2.4 V[1]

Legend: NM = Accelerometer OSR Normal Mode (CTRL_REG2[mods] = 0b00);
LP = Accelerometer OSR Low Power (CTRL_REG2[mods] = 0b11);
OS0 = Magnetometer OSR set to 0 (M_CTRL_REG1[m_os] = 0b000);
OS7 = Magnetometer OSR set to 7 (M_CTRL_REG1[m_os] = 0b111).

Mode	Acc only		Mag only		Hybrid		
ODR	NM	LP	OS0	OS7	NM/OS0	LP/OS0	NM/OS7
800	239	239	1072	1072			
400	239	121	552	1002	648	647	648
200	121	62	289	966	412	339	607
100	68	33	156	947	220	183	512
50	33	18	90	939	123	105	465
25					74	66	442
12.5	33	7	37	932			

Table 7. IDD (µA) table versus operating modes (VDD + VDDIO), VDD = VDDIO = 2.4 V[1] - *¶continued*

Legend: NM = Accelerometer OSR Normal Mode (CTRL_REG2[mods] = 0b00);
LP = Accelerometer OSR Low Power (CTRL_REG2[mods] = 0b11);
OS0 = Magnetometer OSR set to 0 (M_CTRL_REG1[m_os] = 0b000);
OS7 = Magnetometer OSR set to 7 (M_CTRL_REG1[m_os] = 0b111).

Mode	Acc only		Mag only		Hybrid		
ODR	NM	LP	OS0	OS7	NM/OS0	LP/OS0	NM/OS7
6.25	33	7	37	931	51	35	437
3.125					51	35	437
1.5625	33	7	36	931			
0.78125					51	35	436
stby				2			

[1] Values are based on limited number of samples and are for reference only. Output data rates do not exist for the shaded cells.

9.5 Absolute maximum ratings

Stresses above those listed as “absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

NXP recommends that customers using magnetic sensor components adopt industry standard safe handling practices and procedures for magnetic products. To avoid potential damage to the magnetic transducer contained within this product, it is recommended to only handle the device with non-magnetic tools and fixtures.

Table 8. Maximum ratings

Symbol	Rating		Value	Unit
g_{max}	Maximum acceleration (all axes, 100 µs)		10 000	*g*
VDD_{max}	Supply voltage, interface supply voltage		–0.3 to +3.6	V
$VDDIO_{max}$	Supply voltage, IO voltage		–0.3 to +3.6	V
VIN_{max}	Input voltage on any control pin (SA0/MISO, SA1/CS_B, SCL/SCLK, SDA/MOSI, RST)		–0.3 to VDDIO + 0.3	V
D_{drop}	Drop-test height		1.8	m
-	Maximum exposed magnetic field without perming	[1]	3000	µT
-	Maximum exposed field without permanent damage		0.1	T
T_{STG}	Storage temperature range		–40 to +125	°C

[1] Sensor characteristics can be restored on a “permed” device by means of briefly applying an external uniform magnetic field on the order of 100 Gauss or greater, along the X-axis.

Table 9. ESD and latchup protection characteristics

Symbol	Rating	Value	Unit
HBM	Human body model	±2000	V
MM	Machine model	±200	V

Table 9. ESD and latchup protection characteristics - *¶continued*

Symbol	Rating	Value	Unit
CDM	Charge device model	±500	V
I_{LU}	Latchup current at T = 85 °C	±100	mA

This device is sensitive to mechanical shock. Improper handling can cause permanent damage to the part or cause the part to otherwise fail.

This device is sensitive to ESD, improper handling can cause permanent damage to the part.

10. Digital interfaces

10.1 I²C interface characteristics

Table 10. I²C slave timing values[1]

Symbol	Parameter		I²C fast mode		Unit
			Min	Max	
f_{SCL}	SCL clock frequency		0	400	kHz
t_{BUF}	Bus free time between stop and start condition		1.3	-	µs
$t_{HD;STA}$	(Repeated) start hold time		0.6	-	µs
$t_{SU;STA}$	(Repeated) start setup time		0.6	-	µs
$t_{SU;STO}$	STOP condition setup time		0.6	-	µs
$t_{HD;DAT}$	SDA data hold time	[2]	0.05	0.9	µs
$t_{VD;DAT}$	SDA valid time	[2][3]	-	0.9	µs
$t_{VD;ACK}$	SDA valid acknowledge time	[2][4]	-	0.9	µs
$t_{SU;DAT}$	SDA setup time		100	-	ns
t_{LOW}	SCL clock low time		1.3	-	µs
t_{HIGH}	SCL clock high time		0.6	-	µs
t_r	SDA and SCL rise time	[5]	20 + 0.1 C_b	300	ns
t_f	SDA and SCL fall time	[5]	20 + 0.1 C_b	300	ns
t_{SP}	Pulse width of spikes on SDA and SCL that must be suppressed by internal input filter		0	50	ns

[1] All values referred to VIH (min) and VIL (max) levels

[2] This device does not stretch the low period (t_{LOW}) of the SCL signal.

[3] $t_{VD;DAT}$ = time for data signal from SCL low to SDA output.

[4] $t_{VD;ACK}$ = time for acknowledgement signal from SCL low to SDA output (high or low, depending on which one is worse)

[5] C_b = total capacitance of one bus line in pF.

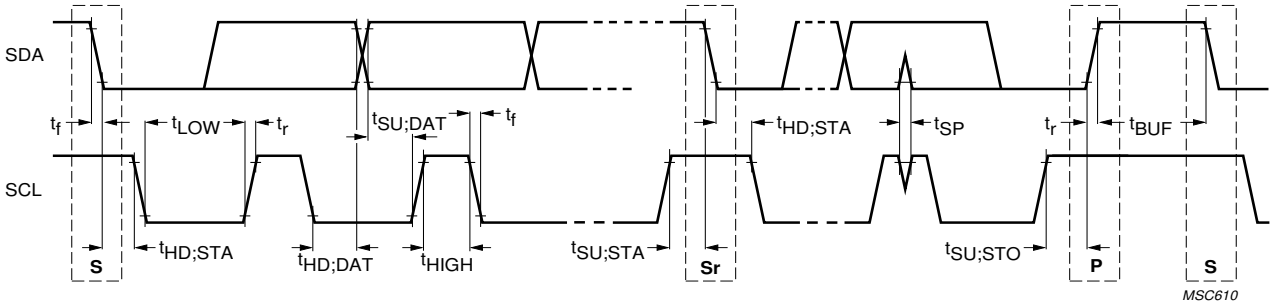


Fig 5. I^2C slave timing diagram

10.1.1 General I^2C operation

There are two signals associated with the I^2C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. External pullup resistors connected to VDDIO are required for SDA and SCL. When the bus is free both the lines are high. The I^2C interface is compliant with fast mode (400 kHz), and normal mode (100 kHz) I^2C standards. Operation at frequencies higher than 400 kHz is possible, but depends on several factors including the pullup resistor values, and total bus capacitance (trace + device capacitance).
See Table 11 for more information.

A transaction on the bus is started through a start condition (ST) signal, which is defined as a high-to-low transition on the data line while the SCL line is held high. After the ST signal has been transmitted by the master, the bus is considered busy. The next byte of data transmitted contains the slave address in the first seven bits, and the eighth bit, the read/write bit, indicates whether the master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after the ST condition with its own address. If they match, the device considers itself addressed by the master. The ninth clock pulse, following the slave address byte (and each subsequent byte) is the acknowledge (ACK). The transmitter must release the SDA line during the ACK period. The receiver must then pull the data line low so that it remains stable low during the high period of the acknowledge clock period.

The number of bytes per transfer is unlimited. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL low to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. This delay action is called clock stretching. Not all receiver devices support clock stretching. Not all master devices recognize clock stretching. This part does not use clock stretching.

A low to high transition on the SDA line while the SCL line is high is defined as a stop condition (SP) signal. A write or burst write is always terminated by the master issuing the SP signal. A master should properly terminate a read by not acknowledging a byte at the appropriate time in the protocol. A master may also issue a repeated start signal (SR) during a transfer

The slave addresses that may be assigned to the FXOS8700CQ part are 0x1C, 0x1D, 0x1E, or 0x1F. The selection is made through the logic level of the SA1 and SA0 inputs.

Table 11. I²C slave address

SA1	SA0	Slave address
0	0	0x1E
0	1	0x1D
1	0	0x1C
1	1	0x1F

10.1.2 I²C read/write operations

Single-byte read

The master (or MCU) transmits a start condition (ST) to the FXOS8700CQ, followed by the slave address, with the R/W bit set to “0” for a write, and the FXOS8700CQ sends an acknowledgement. Then the master (or MCU) transmits the address of the register to read and the FXOS8700CQ sends an acknowledgement. The master (or MCU) transmits a repeated start condition (SR), followed by the slave address with the R/W bit set to “1” for a read from the previously selected register. The FXOS8700CQ then acknowledges and transmits the data from the requested register. The master does not acknowledge (NAK) the transmitted data, but transmits a stop condition to end the data transfer.

When performing a multi-byte or “burst” read, the FXOS8700CQ automatically increments the register address read pointer after a read command is received. Therefore, after following the steps of a single-byte read, multiple bytes of data can be read from sequential registers after each FXOS8700CQ acknowledgment (AK) is received until a no acknowledge (NAK) occurs from the master followed by a stop condition (SP) signaling an end of transmission.

Single-byte write

To start a write command, the master transmits a start condition (ST) to the FXOS8700CQ, followed by the slave address with the R/W bit set to “0” for a write, and the FXOS8700CQ sends an acknowledgement. Then the master (or MCU) transmits the address of the register to write to, and the FXOS8700CQ sends an acknowledgement. Then the master (or MCU) transmits the 8-bit data to write to the designated register and the FXOS8700CQ sends an acknowledgement that it has received the data. Since this transmission is complete, the master transmits a stop condition (SP) to end the data transfer. The data sent to the FXOS8700CQ is now stored in the appropriate register.

Multiple-byte write

The FXOS8700CQ automatically increments the register address write pointer after a write command is received. Therefore, after following the steps of a single-byte write, multiple bytes of data can be written to sequential registers after each FXOS8700CQ acknowledgment (ACK) is received.

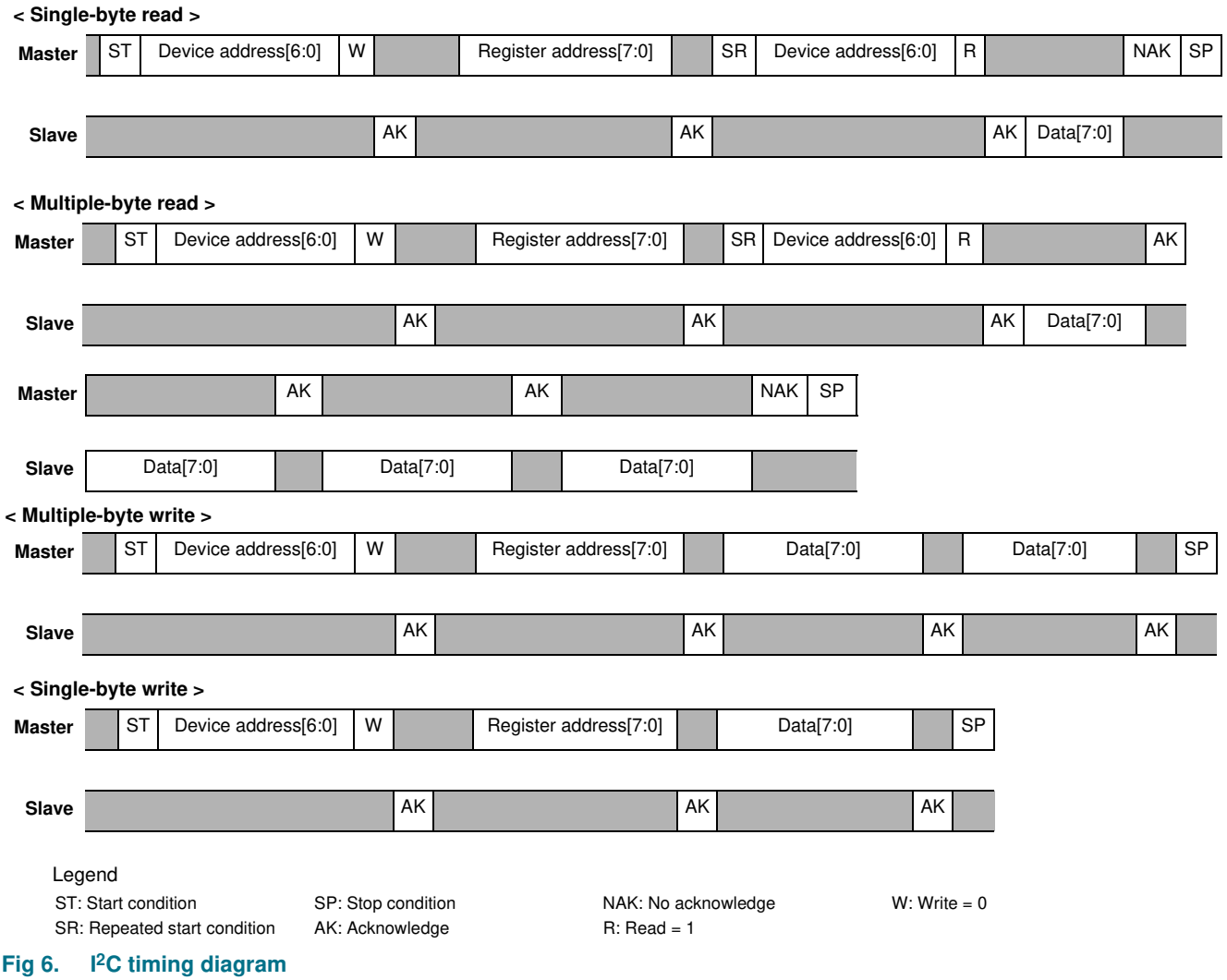


Fig 6. I²C timing diagram

10.2 SPI interface characteristics

SPI interface is a classical master/slave serial port. The FXOS8700CQ is always considered as the slave and thus is never initiating the communication.

Table 12 and Figure 7 describe the timing requirements for the SPI system.

Table 12. SPI timing

Function	Symbol	Min	Max	Unit
Operating frequency	O*f*	-	1	MHz
SCLK period	tSCLK	1000	-	ns
SCLK high time	tCLKH	500	-	ns
SCLK low time	tCLKL	500	-	ns
CS_B lead time	tSCS	65	-	ns
CS_B lag time	tHCS	65	-	ns
MOSI data setup time	tSET	25	-	ns

Table 12. SPI timing

Function	Symbol	Min	Max	Unit
MOSI data hold time	tHOLD	75	-	ns
MISO data valid (after SCLK low edge)	tDDLY	-	500	ns
Width CS high	tWCS	100	-	ns

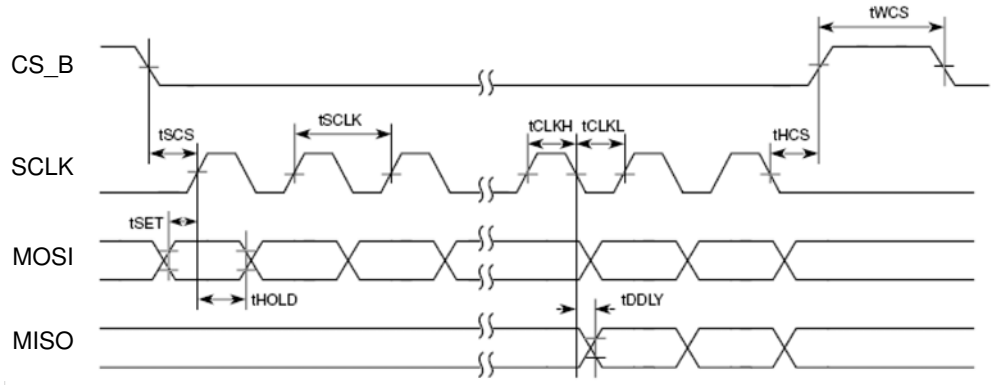


Fig 7. SPI timing diagram

10.2.1 General SPI operation

NOTE

FXOS8700CQ only supports a point-to-point SPI protocol, with only one master (MCU) and one slave device (FXOS8700CQ) present on the bus. FXOS8700CQ does not tri-state the MISO pin when the CS_B pin is deasserted (logic high), which can lead to a bus conflict if multiple slave devices are present on the bus.

Do not connect more than one master and one slave device on the SPI bus.

The CS_B pin is driven low at the start of a SPI transaction, held low for the duration of the transaction, and driven high after the transaction is complete. During a transaction the master toggles the SPI clock (SCLK) and transmits data on the MOSI pin.

A write operation is initiated by transmitting a 1 for the R/W bit. Then the 8-bit register address, ADDR[7:0] is encoded in the first and second serialized bytes. Data to be written starts in the third serialized byte. The order of the bits is as follows:

Byte 0: R/W,ADDR[6],ADDR[5],ADDR[4],ADDR[3],ADDR[2],ADDR[1],ADDR[0],

Byte 1: ADDR[7],X,X,X,X,X,X,X,

Byte 2: DATA[7],DATA[6],DATA[5],DATA[4],DATA[3],DATA[2],DATA[1],DATA[0].

Multiple bytes of DATA may be transmitted. The X indicates a bit that is ignored by the part. The register address is auto-incremented so that the next clock edges will latch the data for the next register. When desired, the rising edge on CS_B stops the SPI communication.

The FXOS8700CQ SPI configuration is as follows:

- Polarity: rising/falling
- Phase: sample/setup
- Order: MSB first

Data is sampled during the rising edge of SCLK and set up during the falling edge of SCLK.

10.2.2 SPI read/write operations

A read operation is initiated by transmitting a 0 for the R/W bit. Then the 8-bit register address, ADDR[7:0] is encoded in the first and second serialized bytes. Subsequent bits are ignored by the part. The read data is deserialized from the MISO pin.

Similarly a write operation is initiated by transmitting a 1 for the R/W bit. After the first and second serialized bytes multiple-data bytes can be transmitted into consecutive registers, starting from the indicated register address in ADDR[7:0].

An SPI transaction is started by asserting the CS_B pin (high-to-low transition), and ended by deasserting the CS_B pin (low-to-high transition).

R/W bit followed by ADDR [6:0]	ADDR[7] followed by 7 “don’t care” bits	Data0	Data1	-	Datan

(1) Data bytes must be transmitted to the slave (FXOS8700CQ) using the MOSI pin by the master when R/W = 1. Data bytes will be transmitted by the slave (FXOS8700CQ) to the master using the MISO pin when R/W = 0. The first two bytes are always transmitted by the master using the MOSI pin. That is, a transaction is always initiated by master.

Fig 8. SPI single-burst read/write transaction diagram

The registers embedded inside FXOS8700CQ are accessed through either an I^2C, or a SPI serial interface. To enable either interface the VDDIO line must be connected to the interface supply voltage. If VDD is not present and VDDIO is present FXOS8700CQ is in shutdown mode and communications on the interface are ignored. If VDDIO is held high, VDD can be powered off and the communications pins will be in a high impedance state. This will allow communications to continue on the bus with other devices.

Table 13. Serial interface pin descriptions

Pin name	Pin description
VDDIO	Digital interface power
SA1/CS_B	I^2C second least significant bit of device address/SPI chip select
SCL/SCLK	I^2C/SPI serial clock
SDA/MOSI	I^2C serial data/SPI master serial data out slave serial data in
SA0/MISO	I^2C least significant bit of the device address/SPI master serial data in slave out

10.2.3 I²C/SPI auto detection

Table 14. I²C/SPI auto detection

SA0	Slave address
GND	I²C
VDDIO	I²C
Floating	SPI

FXOS8700CQ employs an interface mode, auto-detection circuit that will select either I²C or SPI interface mode based on the state of the SA0 pin during power up or when exiting reset. Once set for I²C or SPI operation, the device will remain in I²C or SPI mode until the device is reset or powered down and the auto-detection process is repeated. Please note that when SPI interface mode is desired, care must be taken to ensure that no other slave device drives the common SA0/MISO pin during the 1 ms period after a hard or soft reset or powerup event.

10.2.4 Power supply sequencing and I²C/SPI mode auto-detection

FXOS8700CQ does not have any specific power supply sequencing requirements between VDD and VDDIO voltage supplies to ensure normal operation. To ensure correct operation of the I²C/SPI auto-detection function, VDDIO should be applied before or at the same time as VDD. If this order cannot be maintained, the user should either toggle the RST line or power cycle the VDD rail in order to force the auto-detect function to restart and correctly identify the desired interface. FXOS8700CQ will indicate completion of the reset sequence by toggling the INT1 pin from logic high to low to high over a 500 ns period. If the INT1 pin was already low prior to the reset event, it will only go high.

11. Modes of operation

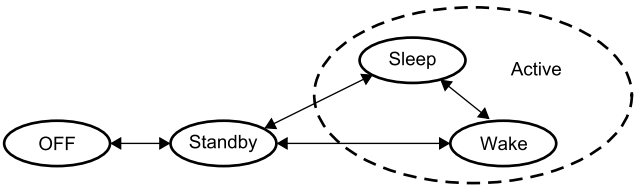


Fig 9. FXOS8700CQ power mode transition diagram

Table 15. Mode of operation description

Mode	I²C/SPI bus state	VDD	VDDIO	Function description
OFF	Powered down	<1.8 V	VDDIO can be > VDD	The device is powered off. All analog and digital blocks are shutdown. I²C bus inhibited.
Standby	I²C/SPI communication with FXOS8700CQ is possible	ON	VDDIO = High VDD = High Active bit is cleared	Only digital blocks are enabled. Analog subsystem is disabled. Internal clocks disabled.
Active (wake/sleep)	I²C/SPI communication with FXOS8700CQ is possible	ON	VDDIO = High VDD = High Active bit is set	All blocks are enabled (digital and analog).

All register contents are preserved when transitioning from active-to-standby mode, but some registers are reset when transitioning from standby-to-active. These registers are noted in Table16. The sleep and wake modes are active modes. For more information on how to use the sleep and wake modes and configuring the device to transition between them, please refer to Section 12 or NXP application note AN4074.

12. Embedded functionality

FXOS8700CQ is a low-power, digital output, 6-axis sensor with both I^2C and SPI interfaces. Extensive embedded functionality is provided to detect inertial and magnetic events at low power, with the ability to notify the host processor of an event using either of the two programmable interrupt pins. The embedded functionality includes:

- 8-bit or 14-bit accelerometer data which includes high-pass filtered data, and 8-bit or 16-bit magnetometer data
- Four different oversampling options for the accelerometer output data, and eight for the magnetometer. The oversampling settings allow the end user to optimize the resolution versus power trade-off in a given application.
- A low-noise accelerometer mode that functions independently of the oversampling modes for even higher resolution
- Low-power, auto-wake/sleep function for conserving power in portable battery powered applications
- Accelerometer pulse-detection circuit which can be used to detect directional single and double taps
- Accelerometer directional motion- and freefall-event detection with programmable threshold and debounce time
- Acceleration transient detection with programmable threshold and debounce time. Transient detection can employ either a high-pass filter or use the difference between reference and current sample values.
- Orientation detection with programmable hysteresis for smooth transitions between portrait/landscape orientations
- Accelerometer vector-magnitude change event detection with programmable reference, threshold, and debounce time values
- Magnetic threshold event detection with programmable reference, threshold, and debounce time
- Magnetometer vector-magnitude change event detection with programmable reference, threshold and debounce time values
- Magnetic min/max detection circuit which can also be used for autonomous calibration of magnetic hard-iron offset

Many different configurations of the above functions are possible to suit the needs of the end application. Separate application notes are available to further explain the different configuration settings and potential use cases.

12.1 Factory calibration

FXOS8700CQ's integrated accelerometer and magnetometer sensors are factory calibrated for sensitivity and offset on each axis. The trim values are stored in non-volatile memory (NVM). On power-up, the trim parameters are read from NVM and applied to the internal compensation circuitry. After mounting the device to the PCB, the user may

further adjust the accelerometer and magnetometer offsets through the OFF_X/Y/Z and M_OFF_X/Y/Z registers, respectively. For more information on device calibration, refer to NXP application note, AN4399.

12.2 8-bit or 14-bit accelerometer data

The measured acceleration data is stored in the OUT_X_MSB, OUT_X_LSB, OUT_Y_MSB, OUT_Y_LSB, OUT_Z_MSB, and OUT_Z_LSB registers as 2's complement 14-bit numbers. The most significant 8-bits of each axis are stored in the OUT_X/Y/Z_MSB registers, so applications needing only 8-bit results simply read these three registers and ignore the OUT_X/Y/Z_LSB registers. To do this, the f_read mode bit in CTRL_REG1 must be set.

When the full-scale range is set to 2 *g*, the measurement range is –2 *g* to +1.999 *g*, and each count corresponds to 0.244 mg at ±14-bits resolution. When the full-scale is set to 8 *g*, the measurement range is –8 *g* to +7.996 *g*, and each count corresponds to 0.976 mg. The resolution is reduced by a factor of 64 if only the 8-bit results are used (CTRL_REG1[f_read] = 1). For further information on the different data formats and modes, please refer to NXP application note AN4076.

12.3 Accelerometer low-power modes versus high-resolution modes

FXOS8700CQ can be optimized for lower power or higher resolution of the accelerometer output data. High resolution is achieved by setting the lnoise bit in register 0x2A. This improves the resolution (by lowering the noise), but be aware that the full-scale range setting is restricted to ±2 *g* or ±4 *g* when this bit is set. This will affect all internal embedded functions (scaling of thresholds, etc.) and reduce noise. Another method for improving the resolution of the data is through oversampling. One of the oversampling schemes of the output data can be activated when CTRL_REG2[mods] = 0b10 which will improve the resolution of the output data without affecting the internal embedded functions or fixing the dynamic range.

There is a trade-off between low power and high resolution. Low power can be achieved when the oversampling rate is reduced. When CTRL_REG2[mods] = 0b10, the lowest power is achieved, at the expense of higher noise. In general, the lower the selected ODR and OSR, the lower the power consumption. For more information on how to configure the device in low-power or high-resolution modes and understand the benefits and trade-offs, please refer to NXP application note AN4075.

12.4 Auto-wake/sleep mode

FXOS8700CQ can be configured to transition between sample rates (with their respective current consumptions) based on the status of the embedded interrupt event generators in the device. The advantage of using the auto-wake/sleep is that the system can automatically transition to a higher sample rate (higher current consumption) when needed but spends the majority of the time in the sleep mode (lower current) when the device does not require higher sampling rates. Auto-wake refers to the device being triggered by one of the interrupt event functions to transition to a higher sample rate. This may also interrupt the processor to transition from a sleep mode to a higher power mode.

Sleep mode occurs when none of the enabled interrupt event functions has detected an interrupt within the user-defined, time-out period. The device will then transition to the specified lower sample rate. It may also alert the processor to go into a lower power mode to save power during this period of inactivity. Refer to AN4074 for more detailed information on configuring the auto-wake/sleep function.

12.5 Hybrid mode

FXOS8700CQ uses a single common analog-to-digital converter (ADC) for both the accelerometer and magnetometer. When operating in hybrid mode (M_CTRL_REG1[m_hms] = 0b11), both the accelerometer and magnetometer sensors are actively measured by the ADC at an ODR equal to one half of the setting made in CTRL_REG1[dr] when operating in accelerometer-only mode (M_CTRL_REG1[m_hms] = 0b00 (default)) or magnetometer-only mode (M_CTRL_REG1[m_hms] = 0b01). While the ODR is common to both sensors when operating in hybrid mode, the OSR settings for each sensor are independent and may be set using the CTRL_REG2[mods] for the accelerometer and M_CTRL_REG1[m_os] for the magnetometer, respectively.

12.6 Accelerometer freefall and motion event detection

FXOS8700CQ integrates a programmable threshold based acceleration detection function capable of detecting either motion or freefall events depending upon the configuration. For further details and examples on using the embedded freefall and motion detection functions, refer to NXP application note AN4070.

12.6.1 Freefall detection

The detection of “Freefall” involves the monitoring of the X, Y, and Z axes for the condition where the acceleration magnitude is *below* a user-specified threshold for a user-definable amount of time. Typically, the usable threshold ranges are between ±100 mg and ±500 mg.

12.6.2 Motion detection

Motion detection is often used to alert the main processor that the device is currently in use. When the acceleration exceeds a set threshold for a set amount of time, the motion interrupt is asserted. A motion can be a fast moving shake or a slow moving tilt. This will depend on the threshold and timing values configured for the event. The motion detection function can analyze static acceleration changes or faster jolts. The timing value is set by a configurable debounce counter. The debounce counter acts like a filter to indicate whether the condition exists for longer than a set amount of time (that is, 100 ms or longer). There is also directional data available in the source register to detect the direction of the motion that generated the interrupt. This is useful for applications such as directional shake or flick detection, and can also assist gesture detection algorithms by indicating that a motion gesture has started.

12.7 Transient detection

FXOS8700CQ integrates an acceleration transient detection function that incorporates a high-pass filter. Acceleration data goes through the high-pass filter, eliminating the DC tilt offset and low frequency acceleration changes. The high-pass filter cutoff can be set by the user to four different frequencies which are dependent on the selected output data

rate (ODR). A higher cutoff frequency ensures that DC and slowly changing acceleration data will be filtered out, allowing only the higher frequencies to pass. The transient detection feature can be used in the same manner as the motion detection by bypassing the high-pass filter. There is an option in the configuration register to do this. This adds more flexibility to cover the various customer use cases.

Many applications use the accelerometer's static acceleration readings (that is, tilt) which measure the change in acceleration due to gravity only. These functions benefit from acceleration data being filtered with a low-pass filter where high-frequency data is considered noise. However, there are many functions where the accelerometer must analyze dynamic acceleration. Functions such as tap, flick, shake and step counting are based on the analysis of the change in the dynamic acceleration. The transient detection function can be routed to either interrupt pin through bit 5 in CTRL_REG5 register (0x2E). Registers 0x1D – 0x20 are used for configuring the transient detection function. The source register contains directional data to determine the direction of the transient acceleration, either positive or negative. For further information of the embedded transient detection function along with specific application examples and recommended configuration settings, refer to NXP application note AN4461.

12.8 Pulse detection

FXOS8700CQ has embedded single/double and directional pulse detection. This function employs several timers for programming the pulse width time and the latency between pulses. The detection thresholds are independently programmable for each axis. The acceleration data input to the pulse detection circuit can be put through both high and low-pass filters, allowing for greater flexibility in discriminating between pulse and tap events. The PULSE_SRC register provides information on the axis, direction (polarity), and single/double event status for the detected pulse or tap. For more information on how to configure the device for pulse detection, please refer to NXP application note AN4072.

12.9 Orientation detection

FXOS8700CQ has an embedded orientation detection algorithm with the ability to detect all six orientations. The transition angles and hysteresis are programmable, allowing for a smooth transition between portrait and landscape orientations.

The angle at which the device no longer detects the orientation change is referred to as the "Z-lockout angle". The device operates down to 29° from the flat position. All angles are accurate to ±2°.

For further information on the orientation detection function refer to NXP application note, AN4068.

12.10 Acceleration vector-magnitude detection

FXOS8700CQ incorporates an acceleration vector-magnitude change detection block that can be configured to generate an interrupt when the acceleration magnitude exceeds a preset threshold for a programmed debounce time. The function can be configured to operate in absolute or relative modes, and can also act as a wake-to-sleep/sleep-to-wake source. This function is useful for detecting acceleration transients when operated in absolute mode, or for detecting changes in orientation when operated in relative mode, refer to NXP application note AN4692.

12.11 Magnetic vector-magnitude detection

FXOS8700CQ incorporates a magnetic vector-magnitude change detection block that can be configured to generate an interrupt when the magnetic field magnitude exceeds a preset threshold for a programmed debounce time. The function can be configured to operate in absolute or relative modes, and can also act as a wake-to-sleep/sleep-to-wake source. For more information, refer to NXP application note AN4458.

12.12 Magnetic threshold detection

FXOS8700CQ incorporates a magnetic threshold event detection block that can be configured to generate an interrupt when the magnetic field on the enabled axes is above or below a programmed threshold.

Two logic combinations are possible for the detection: all of the enabled axes below their respective thresholds (AND condition), or any of the enabled axes above their respective thresholds (OR condition). Even detection may be filtered using a dedicated debounce counter to avoid spurious event detection. The thresholds for each axis are individually programmable and the function can also act as a wake-to-sleep/sleep-to-wake source.

12.13 Magnetic min/max detection (autonomous calibration)

FXOS8700CQ incorporates a magnetic min/max detection circuit that can be used to automatically track the minimum and maximum field values measured on each of the X, Y, and Z axes. The stored minimum and maximum values may optionally be used to determine the magnetic hard-iron compensation and load the offset registers with the appropriate correction values. For more information, refer to NXP application note AN4459.

13. Example FXOS8700CQ driver code

13.1 Introduction

It is very straightforward to configure the FXOS8700CQ and start receiving data from the three accelerometer and three magnetometer channels. Unfortunately, since every hardware platform will be different, it is not possible to provide completely portable software drivers. This section therefore provides real FXOS8700CQ driver code for a Kinetis uC board running under the MQX operating system. The I2C functions s_i2c_read_regs and s_i2c_write_regs are not provided here and should be replaced with the corresponding low level I2C driver code on the development platform.

13.2 FXOS8700CQ addresses

This section lists the I2C address of the FXOS8700CQ. The I2C address depends on the logic level of FXOS8700CQ's SA0 and SA1 address selection pins, so the actual I2C address may be 0x1C, 0x1D, 0x1E or 0x1F.

Please see Table 11, "I2C slave address," on page 15 for the available I2C addresses and SA1/SA0 settings.

Example 1.

```
// FXOS8700CQ I2C address
#define FXOS8700CQ_SLAVE_ADDR     0x1E   // with pins SA0=0, SA1=0
```

Some of the key FXOS8700CQ internal register addresses are listed below.

Example 2.

```
// FXOS8700CQ internal register addresses
#define FXOS8700CQ_STATUS         0x00
#define FXOS8700CQ_WHOAMI         0x0D
#define FXOS8700CQ_XYZ_DATA_CFG   0x0E
#define FXOS8700CQ_CTRL_REG1      0x2A
#define FXOS8700CQ_M_CTRL_REG1    0x5B
#define FXOS8700CQ_M_CTRL_REG2    0x5C
#define FXOS8700CQ_WHOAMI_VAL     0xC7
```

The reference driver code shown in this example does a block read of the FXOS8700CQ status byte and three 16-bit accelerometer channels plus three 16-bit magnetometer channels for a total of 13 bytes in a single I2C read operation.

Example 3.

```
// number of bytes to be read from the FXOS8700CQ
#define FXOS8700CQ_READ_LEN    13     // status plus 6 channels =
13 bytes
```