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FS4500/FS6500 evaluation boards

KTFRDMFS4500-FS6500EVMUG

Rev. 4.0 — 12 June 2017 **User guide**

1 FRDMFS4503CAEVM, FRDMFS6523CAEVM and FRDMFS6522LAEVM evaluation boards

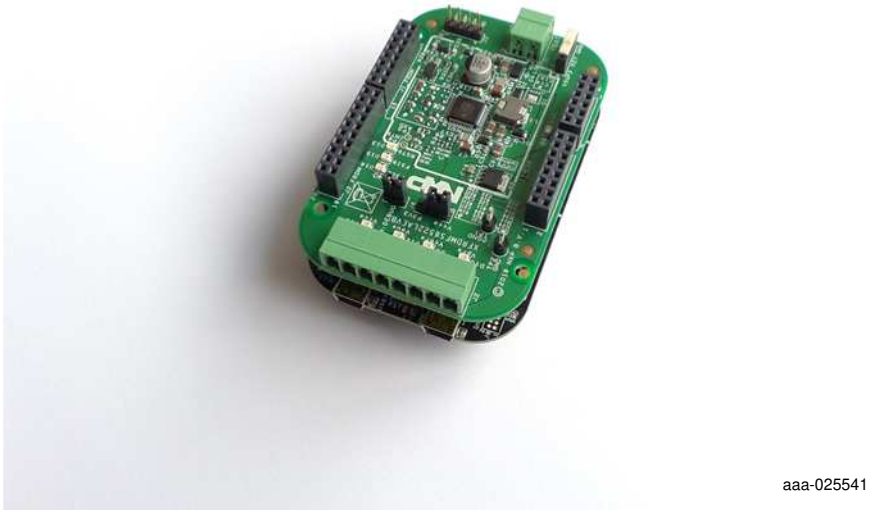

Figure 1. FRDMFS6523CAEVM

2 Important notice

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3 Getting started

3.1 Jump start

NXP's analog product development boards provide an easy-to-use platform for evaluating NXP products. The boards support a range of analog, mixed-signal and power solutions. They incorporate monolithic ICs and system-in-package devices that use proven high-volume SMARTMOS technology. NXP products offer longer battery life, a smaller form factor, reduced component counts, lower cost and improved performance in powering state of the art systems.

1. Go to the relevant Tool Summary Page:
   http://www.nxp.com/FRDMFS6522LAEVM
   http://www.nxp.com/FRDMFS6523CAEVM
   http://www.nxp.com/FRDMFS4503CAEVM
2. Review your Tools Summary Page.
3. Locate and click:

4. Download the documents, software and other information.

Once the files are downloaded, review the user guide in the bundle. The user guide includes setup instructions, BOM and schematics. Jump start bundles are available on each tool summary page with the most relevant and current information. The information includes everything needed for design.

3.2 Kit contents/packing list

The FRDMFS6522LAEVM, FRDMFS6523CAEVM and FRDMFS4503CAEVM contents include:

- Assembled and tested FRDMFS65xx board
- Assembled and test FRDM-KL25Z board
- 3.0 ft. USB-STD A to USB-B-mini cable
- Connector, terminal block plug, 2 pos., str. 3.81 mm
- Connector, terminal block plug, 8 pos., str. 3.81 mm

3.3 Required equipment

The EVM requires the following items:

- Power supply with a range of 8.0 V to 40 V and a current limit set initially to 1.0 A
  Standard A plug to Mini-B plug USB cable M/M
  FlexGUI graphical user interface
  FlexGUI register definition XML file

3.4 EVM overview

The EVM contains two boards:

- **FRDMFS4503CAEVB or FRDMFS6523CAEVB or FRDMFS6522LAEVB:** These are the evaluation boards available for the FS6500 / FS4500 SBC. The hardware is described in Section 4.5 "Getting to know the hardware". This document refers to these boards as EVBs.
- **FRDM-KL25Z:** This board contains the KL25Z MCU. It is plugged into the EVB by means of the Arduino™ connectors on both boards. The FRDM-KL25Z manages communication between the EVB and a host PC, allowing users to access the EVB's on-board device features and registers. For more information on the FRDM-KL25Z see Section 11 "References"

4 Board description

4.1 Board overview

The FRDMFS4503CAEVB, FRDMFS6523CAEVB and FRDMFS6522LAEVB are hardware evaluation tools supporting system designs based on NXP's FS4500 and FS6500 product families. The EVM allow testing the devices as an integral part of the overall system being developed. They provide access to all FS45xx and FS65xx functions (SPI, IOs) and support functional modes such as debug, normal, buck and boost.

Table 1. EVMs supporting the FS45xx/FS65xx family

EVM name	Supported silicon	Options
FRDMFS6522LAEVM	MC33FS6522LAE	CAN, LIN, No FS1b, V_{CORE} DC/DC 2.2 A [1]
FRDMFS6523CAEVM	MC33FS6523CAE	CAN, FS1b, No LIN, V_{CORE} DC/DC 2.2 A [1]
FRDMFS4503CAEVM	MC33FS4503CAE	CAN, FS1b, No LIN, V_{CORE} LDO 500 mA

[1] The FRDM board is limited to 1.5 A

4.2 Board features

The main features of the FRDMFS6522LAEVB, FRDMFS6523CAEVB and FRDMFS4503CAEVB evaluation boards are:

- VBAT power supply connector
- VCORE configuration:1.3 V
- VCCA configuration: 3.3 V, using internal PMOS
- VAUX configuration: 5.0 V
- Buck or boost setting
- DFS configuration
- Ignition key switch
- CAN bus
- LIN bus (FRDMFS6522LAEVM only)
- FS0B
- FS1B (FRDMFS6523CAEVM or FRDMFS4503CAEVM only)
- IO connector (IO_0 to IO_5)
- Connectivity to KL25Z Freedom board (Access to SPI bus, IOs, LIN digital, RSTB, FS0B, INTB, Debug, MUX_OUT, Regulators)
- LEDs that indicate signal or regulator status

4.3 Block diagram

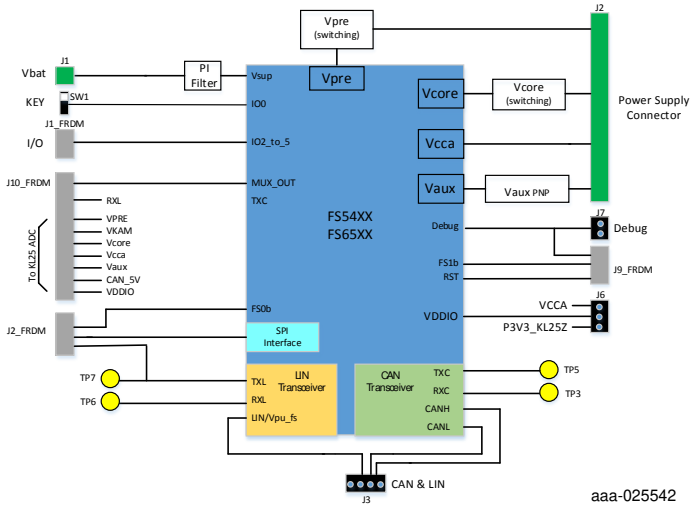


Figure 2. FRDMFS65/FRDMFS45 block diagram

4.4 Device features

TheFS65xx/FS45xx are multi-output power-regulating SMARTMOS devices aimed at the automotive market. They include CAN flexible data (FD) and/or LIN transceivers.

Multiple switching and linear voltage regulators—including low-power mode (32 µA) — provide a variety of wake-up capabilities. An advanced power management scheme maintains high efficiency over a wide range of input voltages (down to 2.7 V) and output current ranges (up to 2.2 A).

The FS45xx/FS65xx family includes enhanced safety features with multiple fail-safe outputs. The devices are capable of fully supporting safety-oriented system partitioning with a high integrity safety level (up to ASIL D).

The built-in CAN FD (flexible data-rate) interface meets all ISO11898-2 and -5 standards. The LIN interface is compliant with LIN protocol specifications 2.0, 2.1, 2.2, and SAEJ2602-2.

Table 2. FS45xx/FS65xxfeatures

Device	Description	Features
FS4500/ FS6500	Automotive control devices	• Battery voltage sensing and MUX output pin • Highly flexible SMPS pre-regulator, allowing two topologies: non-inverting buck-boost and standard buck • Switching mode power supply (SMPS) dedicated to MCU core supply, from 1.0 V to 5.0 V, delivering up to 2.2 A • Switching mode power supply (SMPS) dedicated to MCU core supply, from 1.0 V to 5.0 V, delivering up to 2.2 A • Linear voltage regulator dedicated to auxiliary functions, or to sensor supply (VCCA tracker or independent), 5.0 V or 3.3 V • Linear voltage regulator dedicated to MCU A/D reference voltage or I/Os supply (VCCA), 5.0 V or 3.3 V • 3.3 V keep alive memory supply available in low-power mode • Long duration timer available in low-power mode (1.0 s resolution) • Multiple wake-up sources in low-power mode: CAN, LIN, IOs, LDT • Five configurable I/Os

4.5 Getting to know the hardware

The primary component of the evaluation boards is the SBC. The boards include an FS45xx or FS65xx and provide full access to all the device's features.

This EVB can either be used alone, or connected to the FRDM-KL25Z board included with this EVM. This provides access to all the features and I/Os of FS45xx/FS65xx through a USB connection.

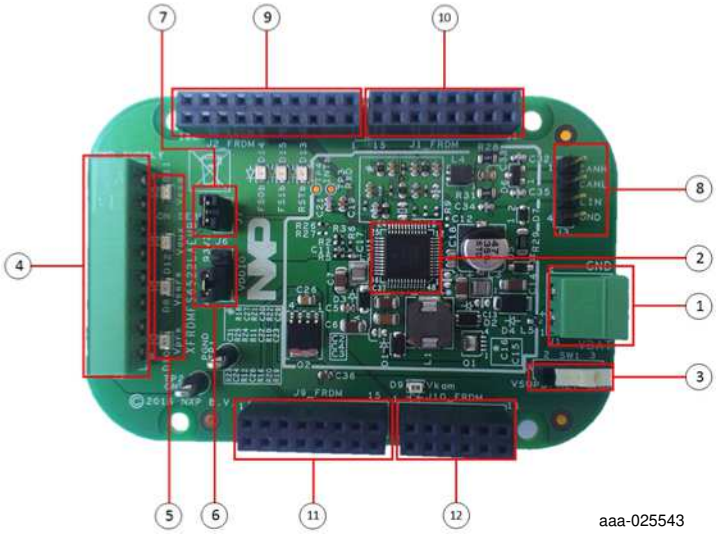


Figure 3. Evaluation board description

Table 3. Board description

Number	Description
1	V_{BAT} connector - Use Phoenix connector to supply board
2	FS45xx / FS65xx
3	Ignition key - Ignition key from car
4	Power supplies - Connector for power supplies (V_{PRE}/V_{CORE}/V_{CCA}/V_{AUX})
5	Power supplies LED - Visualizes regulator state (on or off).
6	V_{DDIO} selection - Selects either V_{CCA} or P3V3_KL25Z (3.3V supply from FRDM-KL25Z board)
7	Enable DBG mode
8	Can & LIN connector - Could be used for debug purpose (CANH, CANL, LIN)
9	I/Os - Input and Output from FS45XX/FS65XX (SPI, V_{PRE}, FS0b, TX LIN)
10	I/Os - Input and Output from FS45XX/FS65XX (IO2, IO3, IO4, IO5, Ignition)
11	I/Os - Input and Output from FS45XX/FS65XX (RSTb, FS1b, DBG, GND, P3V3_KL25Z)
12	I/Os - Input and Output from FS45XX/FS65XX (TX CAN, RX LIN, CAN_5V, V_{CORE}, V_{CCA}, V_{AUX}, V_{KAM}, V_{DDIO})

4.5.1 LED display

The board contains the following LEDs:

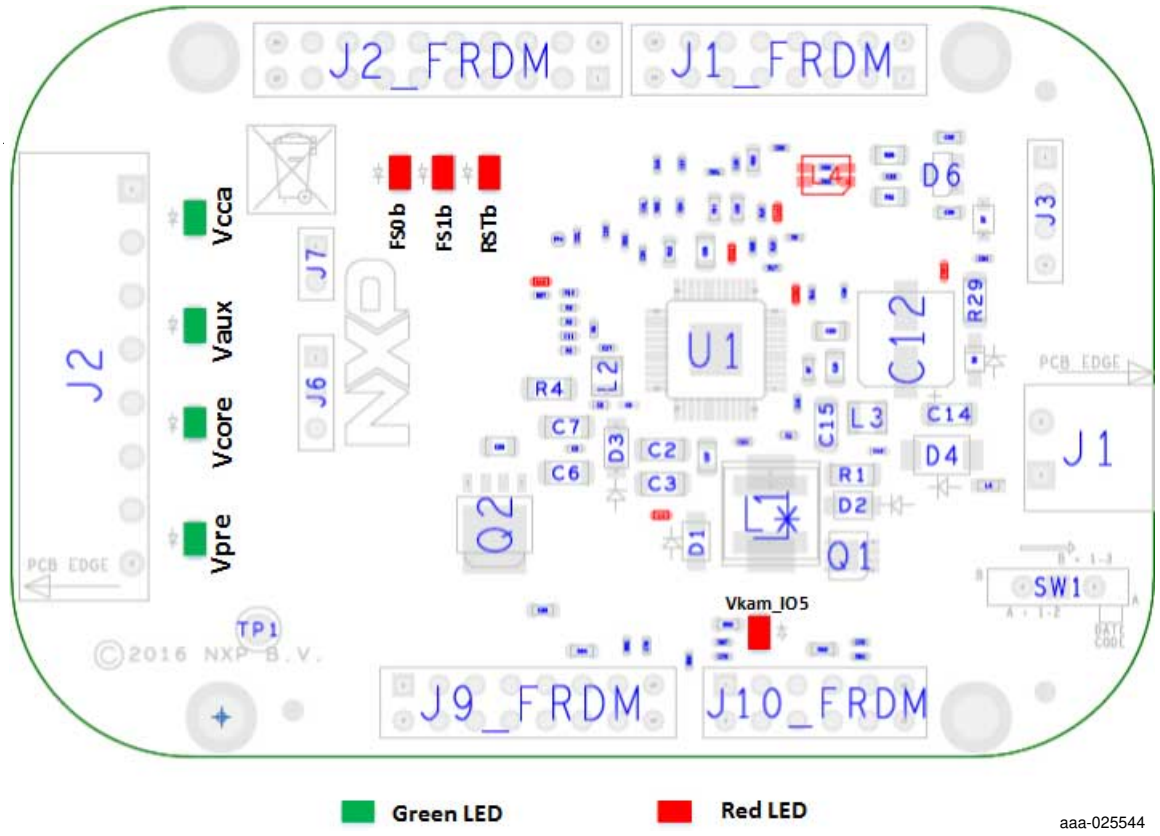


Figure 4. LEDs

Table 4. LEDs

Schematic label	Name	Color	Description
D8	V_{CORE}	Green	V_{CORE} on
D9	Vkam_IO5	Green	Vkam_IO5 on
D10	V_{PRE}	Green	V_{PRE} on
D11	V_{CCA}	Green	V_{CCA} on
D12	V_{AUX}	Green	V_{AUX} on
D13	RSTb	Red	Enabled when RSTB asserted (logic level = 0)
D14	FS0b	Red	Enabled when FS0b asserted (logic level = 0)
D15	FS1b	Red	Enabled when FS1b asserted (logic level = 0)

4.5.2 Jumper definitions

Figure 5 shows the location of jumpers on the evaluation board.

Table 5 describes the function and settings for each jumper. Default jumper settings are shown in bold text.

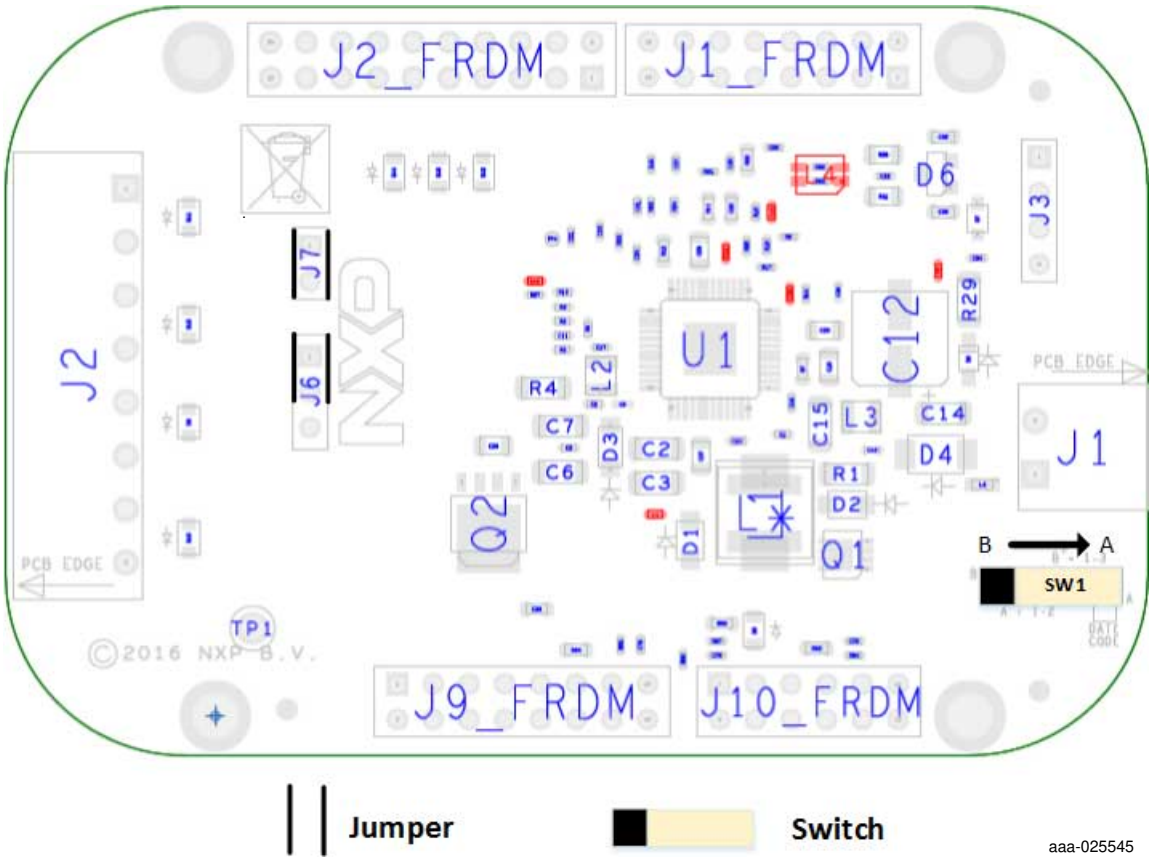


Figure 5. Jumpers

Table 5. Jumper definitions

Jumper	Description	Setting	Connection/Result
J6	VDDIO selection	**[1–2]**	VDDIO referenced to V_{CORE} or P3V3_KL25Z
		[2–3]	VDDIO referenced to V_{CCA}
J7	Debug mode	[1–2]	ON:Debug mode OFF: normal mode

4.5.3 Test point definitions

The following test points provide access to various signals to and from the board.

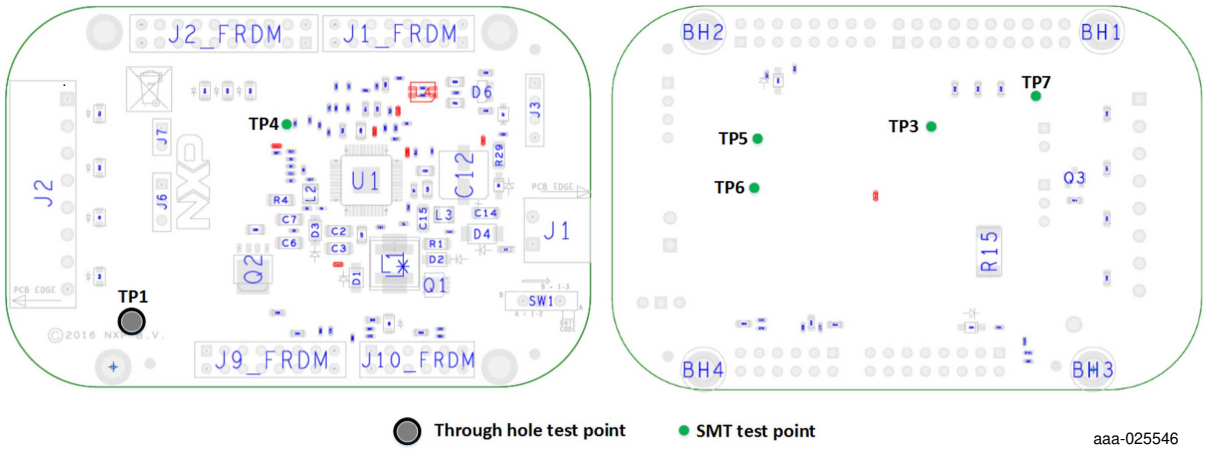


Figure 6. Test points

Table 6. Test point definitions

Test point name	Signal name	Description
TP1	GND	Ground
TP3	RXC	CAN receiver data. Logic level
TP4	INTB	INTB asserted (logic level = 0)
TP5	TXC	CAN transmit data. Logic Level
TP6	RXL	LIN receiver data. Logic level.
TP7	TXL	LIN transmit data. Logic Level

4.5.4 Connectors

Figure 7 shows the location of connectors on the board. The tables below list the pin-outs for each connector.

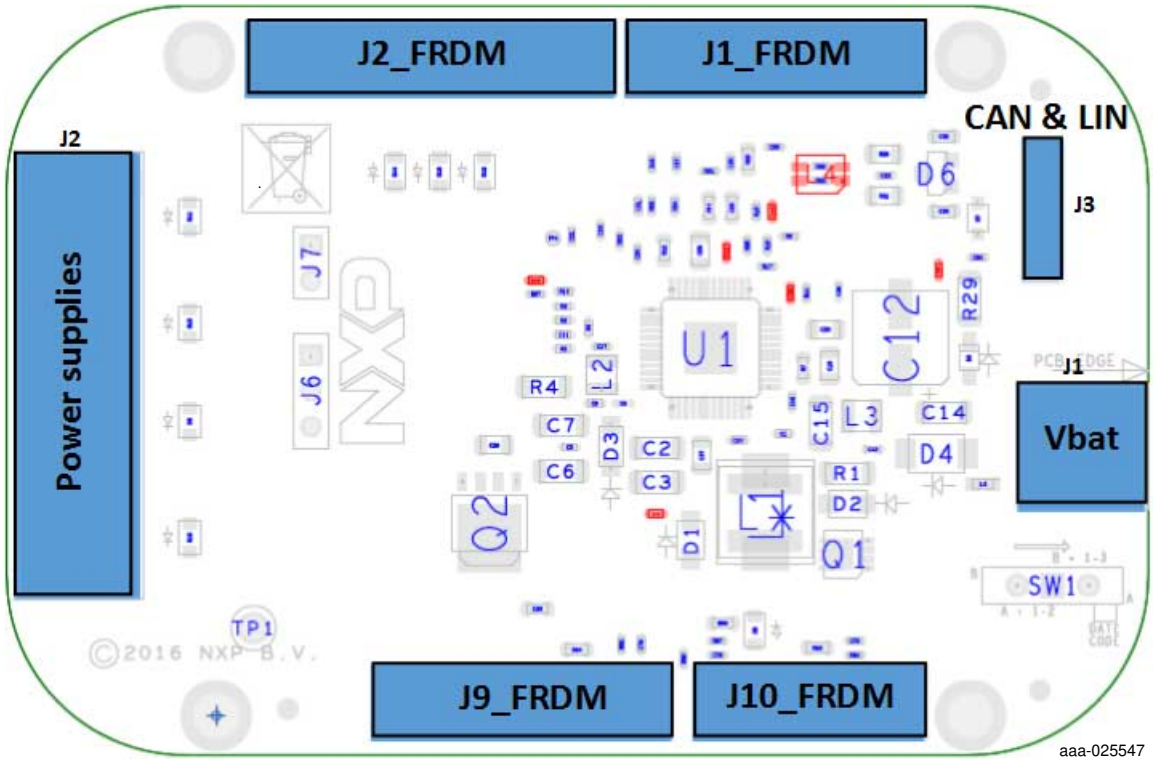


Figure 7. Connectors

4.5.4.1 V_{BAT} connector (J1)

V_{BAT} connects to the board through Phoenix connector (J1).

Table 7. V_{BAT} Phoenix connector (J1)

Pin number	Connection	Description
1	V_{BAT}	Connects to V_{BAT}
2	Ground	Connects to ground

4.5.4.2 SPI connector (J2_FRDM)

The Debug connector(J2_FRDM) gives access to the FS65xx main signal for debug or experimentation purposes.

Table 8. SPI connector (J2_FRDM)

Pin number	Connection	Description
1	Not Connected	
2	Not Connected	
3	Not Connected	
4	Not Connected	
5	Not Connected	
6	CSB	SPI chip select, active low

Pin number	Connection	Description
7	FS0B	Fail-safe 0.
8	MOSI	SPI Master Output Slave Input
9	Not Connected	
10	MISO	SPI Master Input Slave Output
11	Not Connected	
12	SCLK	SPI serial clock
13	Not Connected	
14	GND	Ground
15	Not Connected	
16	Not Connected	
17	Not Connected	
18	Not Connected	
19	TXL	LIN transmit data. Logic level.
20	Not Connected	

4.5.4.3 CAN and LIN connector (J3)

The CAN and LIN connector is mounted on all three boards, but LIN is supported only on the FRDMFS6522LAEVB.

Table 9. CAN & LINconnector (J3)

Pin number	Connection	Description
1	CANH	Connects to the CANH bus line
2	CANL	Connects to CANL bus line
3	LIN	Connects to the LIN bus
4	GND	Connects to ground

4.5.4.4 Debug connector (J9_FRDM)

The debug connector provides access to DBG as well as FS1b and reset.

Table 10. USB connector (J33)

Pin number	Connection	Description
1	Not Connected	
2	Not Connected	
3	FS1b	Fail-safe 1
4	P3V3_KL25Z	3.3V KL25Z supply
5	Not Connected	
6	Not Connected	
7	Not Connected	
8	P3V3_KL25Z	3.3V KL25Z supply

Pin number	Connection	Description
9	Not Connected	
10	Not Connected	
11	Not Connected	
12	GND	Connects to ground
13	DBG	Debug pin selection
14	GND	Connects to ground
15	RSTB	Reset, active low
16	Not Connected	

4.5.4.5 I/O connector (J1_FRDM)

The I/O connector accesses the device under test (DUT) IO and V_{KAM} signals.

Table 11. I/O connector (J1_FRDM)

Pin number	Connection	Description
1	Vkam_IO5	Keep alive memory voltage
2	Not Connected	
3	Not Connected	
4	Not Connected	
5	Key	Ignition signal
6	Not Connected	
7	IO_2	Input/Output 2
8	Not Connected	
9	IO_3	Input/Output 3
10	Not Connected	
11	IO_4	Input/Output 4
12	Not Connected	
13	Not Connected	
14	Not Connected	
15	Not Connected	
16	Not Connected	

4.5.4.6 Power supply connector (J2)

The power supply connector (J2) connects any of the SBC regulators to an external load or board for evaluation purposes.

Table 12. Power supply connector (J2)

Pin number	Connection	Description
1	V_{CCA}	V_{CCA} output voltage
2	GND	Ground

Pin number	Connection	Description
3	V_{AUX}	V_{AUX} auxiliary voltage regulator
4	GND	Ground
5	V_{CORE}	V_{CORE} voltage output
6	GND	Ground
7	V_{PRE}	V_{PRE} regulator output regulator
8	GND	Ground

4.5.4.7 KL25Z ADC inputs (J10_FRDM)

The KL25Z ADCconnector (J10_FRDM) connects the FS6500 regulator outputs to the ADCs on the KL25Z. The regulator values can then be measured and displayed in FlexGUI.

Table 13. KL25Z Analog regulator inputs (J10_FRDM)

Pin number	FRDM Signal	Description
1	Vkam_IO5	Keep alive memory voltage, connected to KL25 ADC0_SE0
2	V_{CORE}	V_{CORE} voltage output, connected to KL25 ADC0_SE8
3	RXL	LIN receiver data. Logic level.
4	V_{AUX}	V_{AUX} auxiliary voltage regulator, connected to KL25 ADC0_SE9
5	VDDIO	Reference voltage for IOs, connected to KL25 ADC0_SE3
6	V_{CCA}	V_{CCA} output voltage, connected to KL25 ADC0_SE12
7	Not connected	
8	CAN_5V	CAN voltage regulator, connected to KL25 ADC0_SE13
9	Not connected	
10	MUX_OUT	Multiplexer output
11	TXC	CAN transmit data. Logic level.
12	Not connected	

4.5.5 Switches

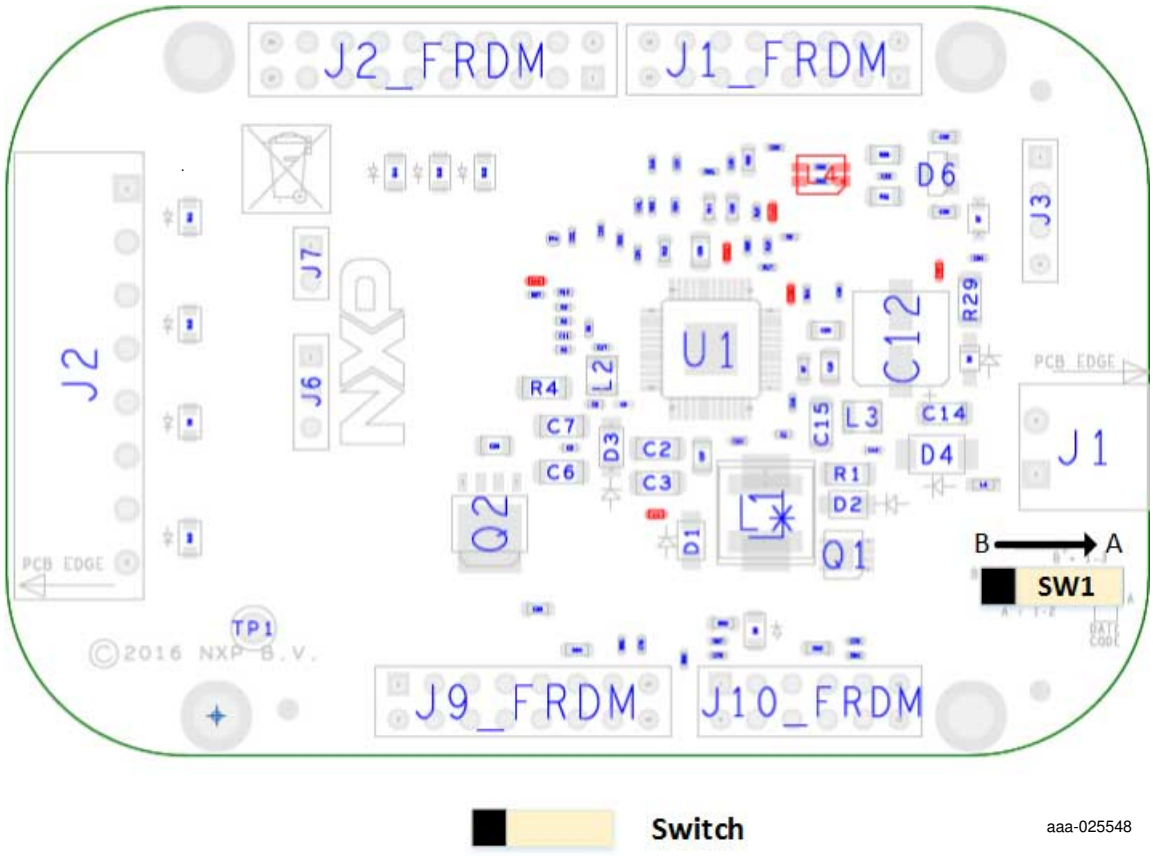


Figure 8. Switches

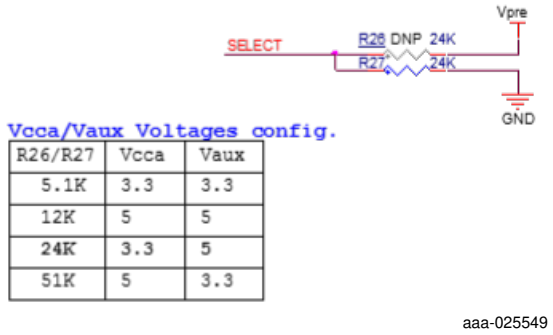
Table 14. SW1

Position	Function	Description
A	GND	Connection between Key input and ground
B	Vsup3	Connection between Key input and Vsup3

5 Board default settings

5.1 V_{CCA} and V_{AUX} setting

V_{CCA} and V_{AUX} are set by default, respectively to 3.3 V and 5.0 V. It's possible to change that by modifying R26 or R27 (whichever is populated) according to Figure 9.



R26/R27	Vcca	Vaux
5.1K	3.3	3.3
12K	5	5
24K	3.3	5
51K	5	3.3

Figure 9. V_{CCA} and V_{AUX} voltage settings

The V_{AUX} regulator is always tied to the external PNP transistor

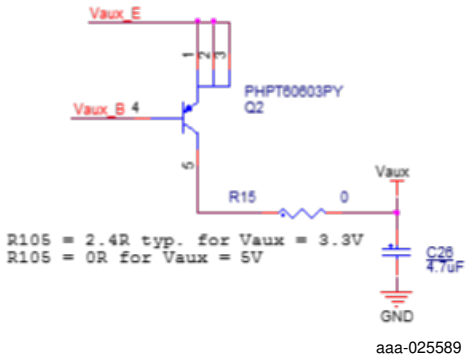


Figure 10. V_{AUX} regulator

5.2 V_{CORE} settings and related configurations

5.2.1 V_{CORE} and F45xx versus FS65xx

The FS45xx family of devices only support V_{CORE} LDO (low dropout) voltage regulators. The FS65xx family only supports V_{CORE} DC/DC voltage regulators. The evaluation board circuitry accommodates this discrepancy by implementing a variation of the BOM for each of the two device families. Populating or not populating resistors with some components depends on which device family is in use and determines which network is enabled.

For the FS45xx family, the following assembly options must be implemented:

- R42: DNP
- C8/C9/R4/D3/L2/C5/C7/R2/C11/R5/C17: populated

For the FS65xx family, it is the opposite:

- R42: populated
- C8/C9/R4/D3/L2/C5/C7/R2/C11/R5/C17: DNP

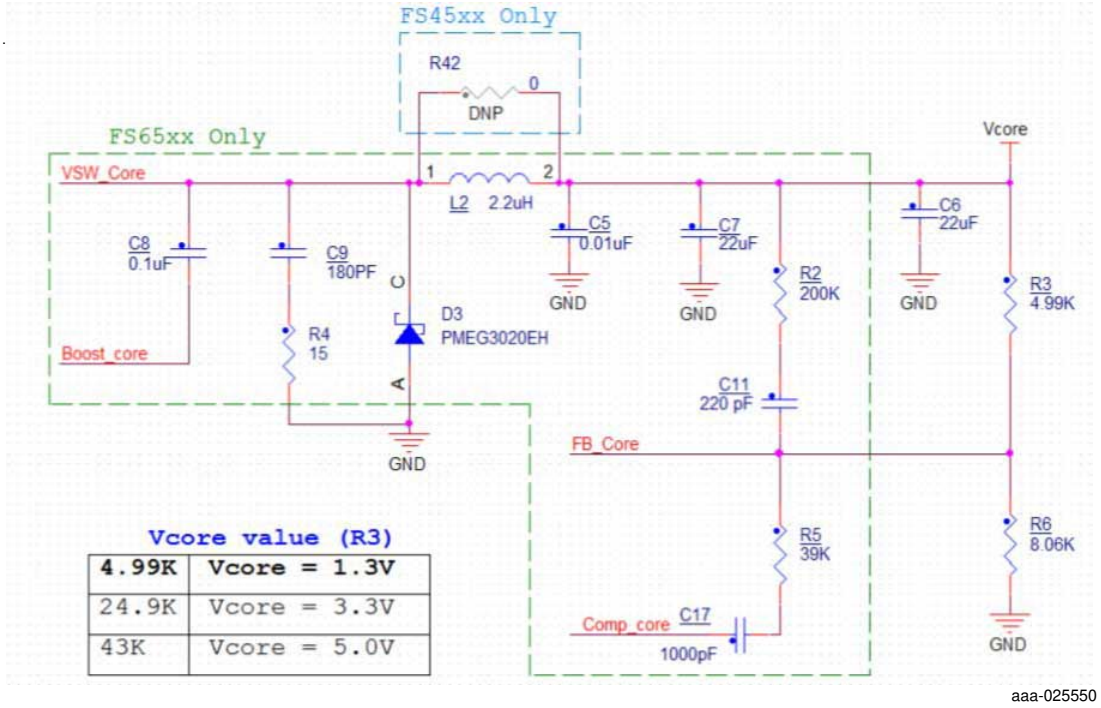


Figure 11. V_{CORE} configuration

5.2.2 Compensation network

Both LDO and DC/DC voltage regulators use VCORE voltage feedback to control the output voltage (see Figure 12).

For FS45xx devices using static (steady-state) LDO regulators, a simple resistor bridge (resistors R3 and R6) determines the feedback voltage. By default, the feedback voltage is 1.3 V.

For FS65xx devices using DC/DC voltage regulators, a pair of RC voltage dividers controls the dynamic behavior of the regulator.

5.2.3 FCRBM Resistor Bridge

The feedback core bridge monitoring (FCRBM) Resistor Bridge is an evaluation board safety feature.

The bridge generates the same voltage as the bridge connected to the FB_core pin. If the difference between the two voltages is greater than the VCORE_FB_DRIFT value, the FS state machine is impacted (refer to data sheet). The drift value is set to 1.3V by default.

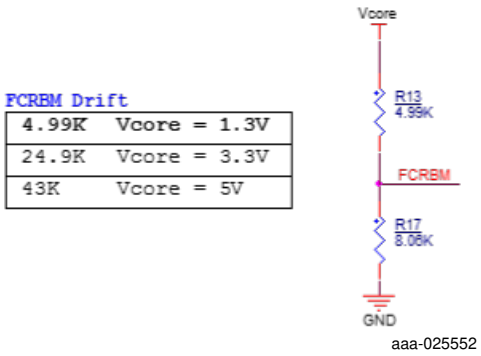


Figure 12. FCRBM Resistor Bridge

5.2.4 MCU analog input

To assure the complete isolation of analog signals connected from an external component to the MCU, remove input resistance as applicable for the following:

- V_{PRE} tied to MCU through R83
- V_{CORE} tied to MCU through R98
- V_{AUX} tied to MCU through R90
- V_{CCA} tied to MCU through R94
- CAN_5V tied to MCU through R80
- MUX_OUT tied to MCU through R18
- V_{KAM} tied to MCU through R96

6 Configuring the EVM

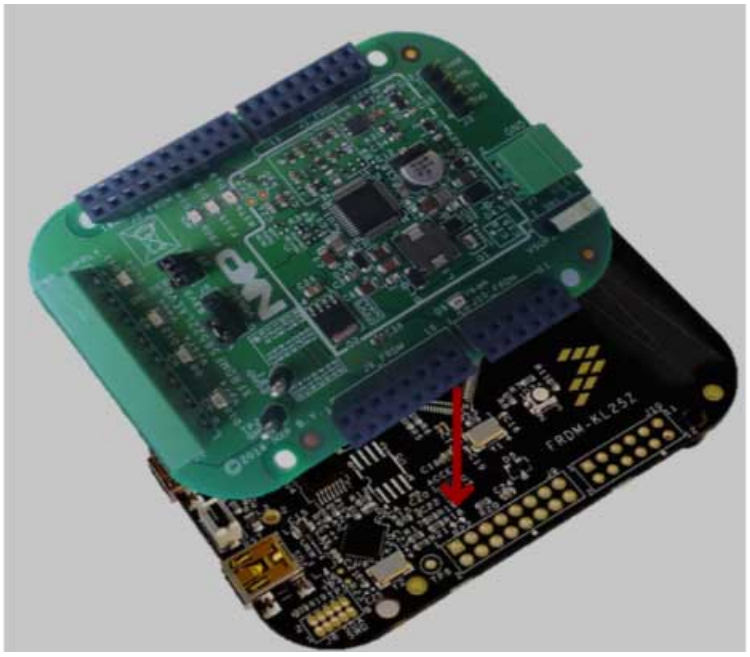
6.1 Connecting the hardware

The EVB can be connected to a PC through the FRDM-KL25Z board included with this EVM or any board with an MCU that supports SPI. A power supply with a typical value of 13.5 V must be connected to J1. Regulators can be loaded using J2 connector.

In order to use the board with an FRDM-KL25Z, these steps must be followed for the hardware setup:

Caution: To avoid damaging the board, the V_{BAT} voltage must not exceed 40 V.

1. With the power switched off, attach the DC power supply to the Phoenix connector (J1) on the evaluation board.
2. A load or an external board can be attached to J2 (not mandatory).
3. Plug the board to an FRDM-KL25Z board.



aaa-025553

4. Connect a USB cable from the USB port labeled **USBKL25Z** on the FRDM-KL25Z board to a USB port on a PC that has the FlexGUI installed.
5. Turn on the DC power supply.

Figure 13 illustrates the hardware configuration.

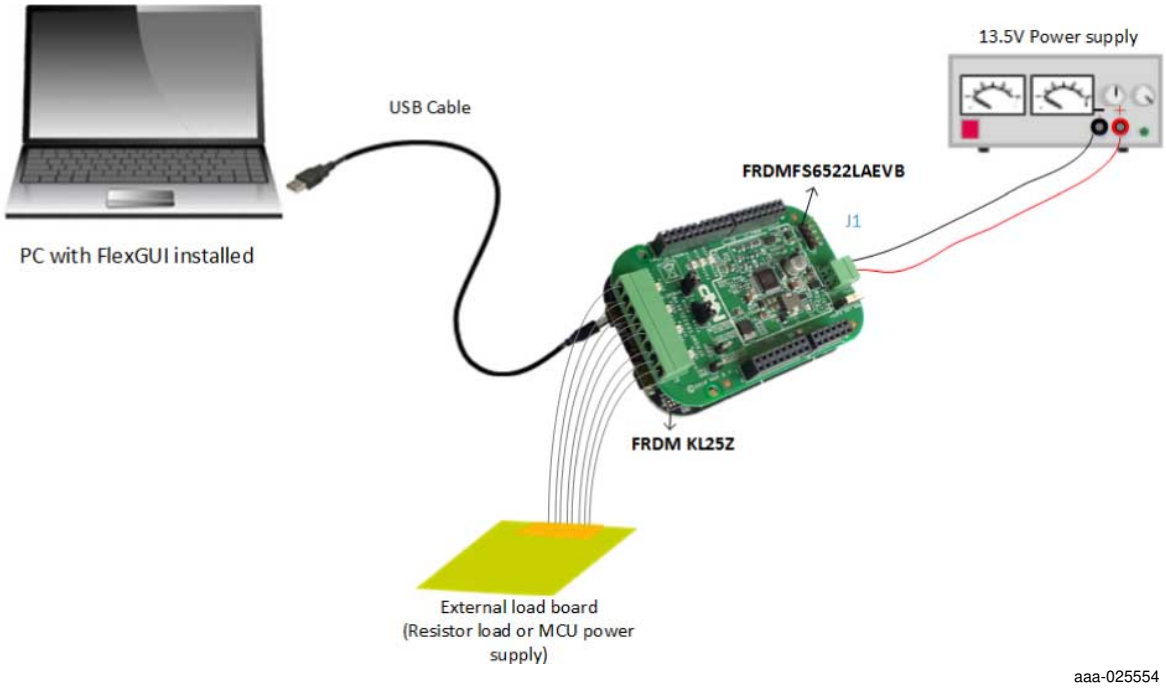


Figure 13. Evaluation board hardware configuration

The software is normally pre-loaded on the KL25Z. For future updates, the procedure for programming the KL25 is described in Section 8 "Appendix A: FRDM-KL25Z software loading".

7 Software

The FRDMFS4503CAEVB/FRDMFS6523CAEVB/FRDMFS6522LAEVB boards must be plugged into a FRDM-KL25Z. Firmware controlling the communication with the FS45xx/FS65xx must be loaded onto the MCU. The procedure for loading the firmware is described in Section 8 "Appendix A: FRDM-KL25Z software loading". The FlexGUI graphical user interface that is installed on a PC serves as the user interface to the evaluation board (Section 9 "Appendix B: Installing the FlexGUI"). When connecting the FRDM-KL25Z board to a PC through a USB cable, the following data exchanges are available:

- SPI access (read and write) to FS45xx/FS65xx
- ADC readout, connected to regulators
  - V_{PRE}
  - V_{CORE}
  - V_{AUX}
  - V_{CCA}
  - CAN_5V
  - MUX_OUT
  - V_{DDIO}
  - V_{KAM}
- I/O readout, connected to IO_2 to IO_5
- FS0B/FS1B readout
- RSTB readout
- CAN generated TX signal
- LIN generated TX signal with loopback checking

The software bundle also includes an XML file containing register descriptions for the FS45xx or FS65XX (depending on the evaluation board).This file must be installed in order for the GUI to work properly. In addition, an optional Excel file can be created to facilitate setting several registers at a click.

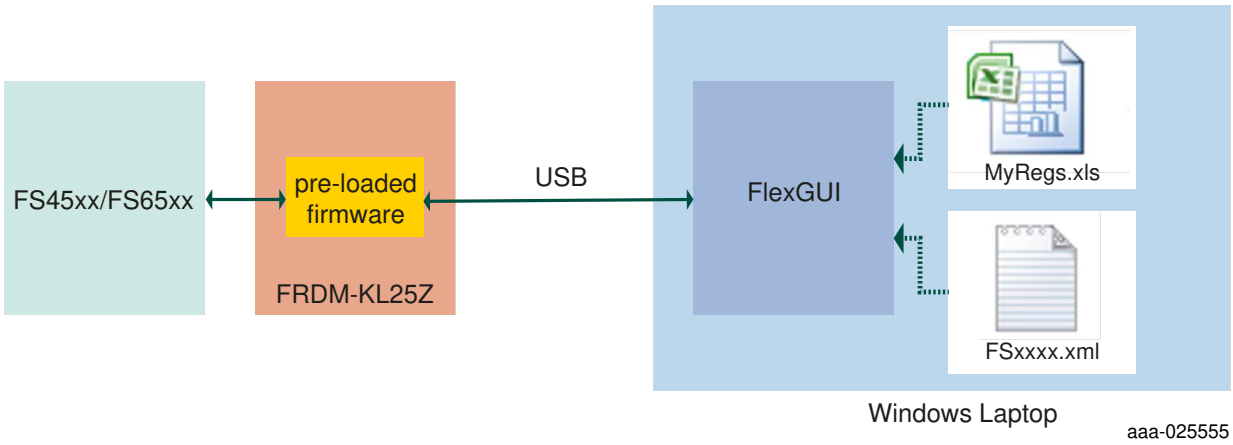
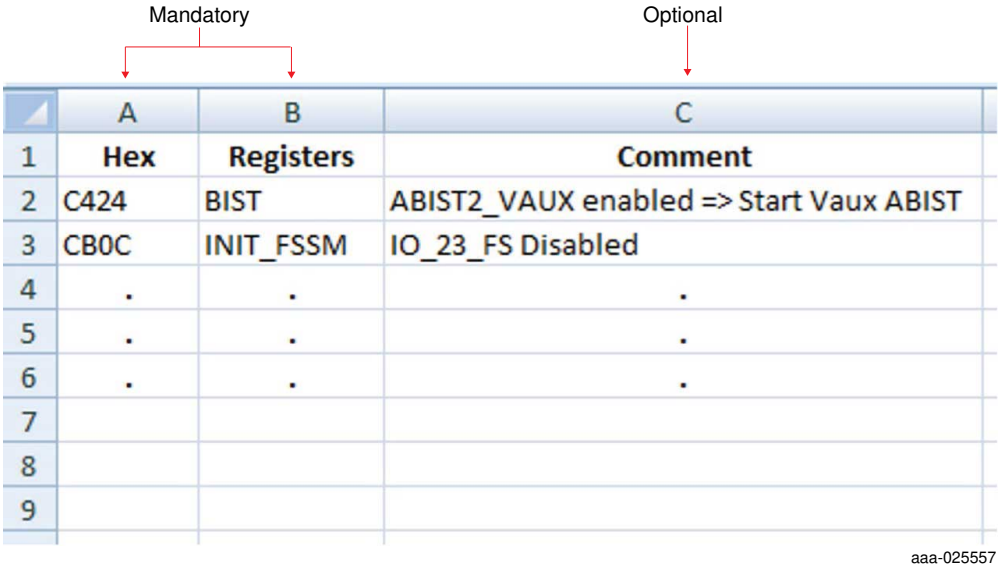


Figure 14. Software overview

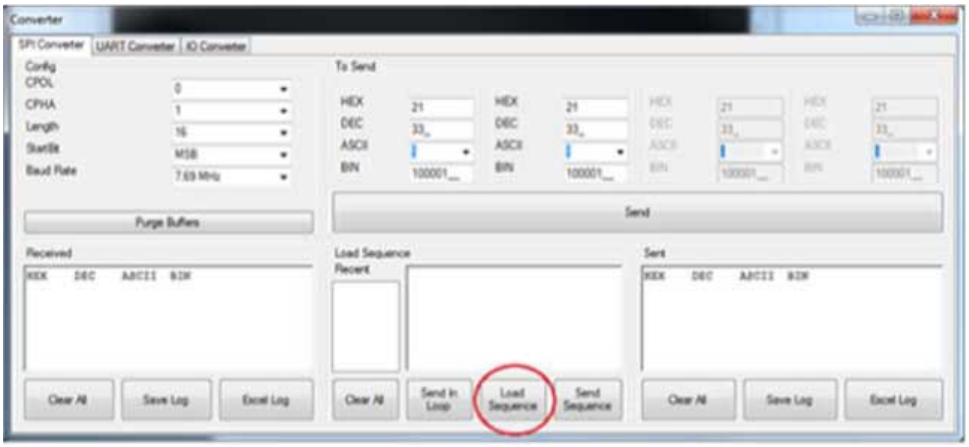
7.1 Creating and using a register configuration file

Creating an Excel register configuration file allows the user to initialize the evaluation board MCU with a predefined set of register values. To create a register configuration file, do the following:

1. Open a new Excel spreadsheet file and label the first three columns in row 1 **hex**, **registers** and **comment**. Notice that the first two columns —**hex** and **registers**— are mandatory. The **comment** column is optional.
2. In the **hex** column (column A), enter the data or address to be assigned to each register. The address and data must be contained in two bytes and must be expressed as a hexadecimal value. Enter one row per register.
3. In the **registers** column (column B), enter the register name associated with the value in the **hex** column.
4. In the **comments** column (column C), enter any comments desired. Data in this column is not processed by the FlexGUI. The image below illustrates a typical register configuration file.



5. Launch FlexGUI. When FlexGUI opens, click the **Load Sequence** button to load the register configuration file.



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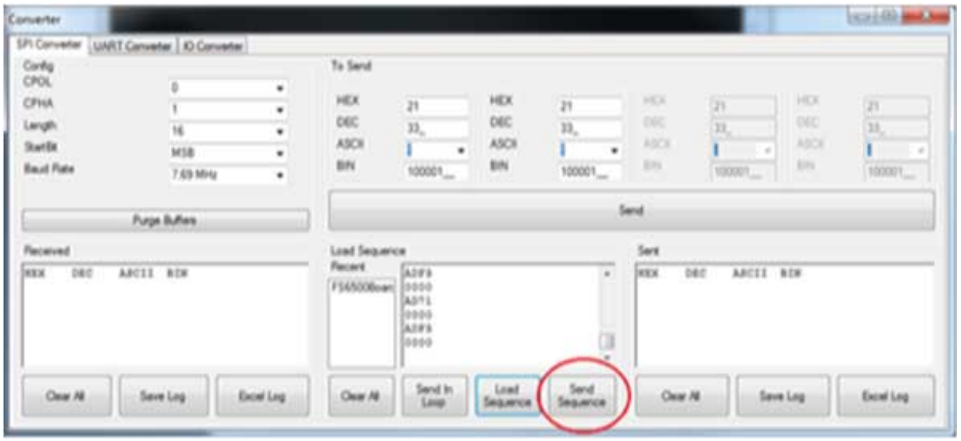
6. Send the register configuration file to the FS45xx/FS65xx by clicking the **Send Sequence** button.



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7.2 Using the FlexGUI

To start the FlexGUI, do the following:

1. Configure the hardware as described in Section 6.1 "Connecting the hardware".
2. To launch the FlexGUI, execute the .bat file created in Section 9 "Appendix B: Installing the FlexGUI" .

7.3 Use case example

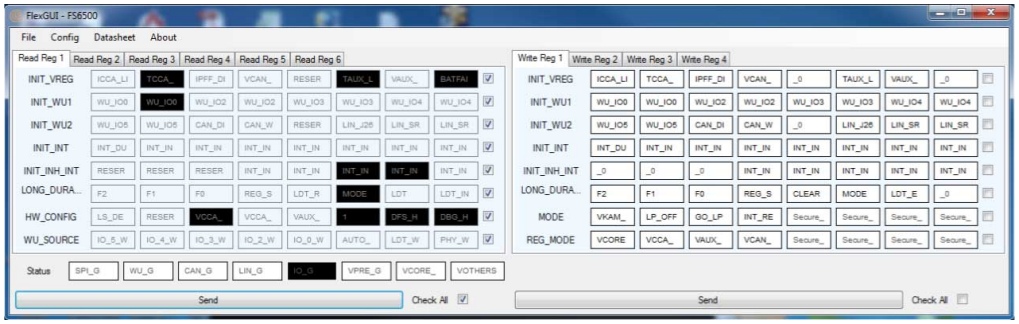
This example assumes the user has configured the hardware as shown in Figure 13 and put the evaluation board into debug mode by placing a connector on jumper J15 (see Section 6.1). After launching the FlexGUI, the example configures registers to disable IO_23_FS safety mode, disable the watchdog and release the FS*x* pins.

- Create an Excel file configured as shown in Table 15. For details on creating an Excel register configuration file, see Section 7.1 "Creating and using a register configuration file"

Table 15. Use case register configuration Excel file example

HEX	Registers	Comment
C465	BIST	Execute ABIST2_VAUX and ABIST2_FS1B
D60C	SF_OUTPUT_REQUEST	Close S1 switch between V_{PRE} and VPU_FS to enable FS1B pull up
CB0C	INIT_FSSM	IO_23_FS Disabled
8900	INIT_INT	Close main machine initialization sequence
D34D	WD_refresh_0	1st Watchdog refresh answer
D29B	WD_refresh_1	2nd Watchdog refresh answer
D237	WD_refresh_2	3rd Watchdog refresh answer
D26E	WD_refresh_3	4th Watchdog refresh answer
D2DC	WD_refresh_4	5th Watchdog refresh answer
D2B9	WD_refresh_5	6th Watchdog refresh answer
D372	WD_refresh_6	7th Watchdog refresh answer
D4A7	RELEASE_FSxB	Release FS0B & FS1B pins

- To use the register configuration file, open FlexGUI, then load the register configuration file and send it to the evaluation board .
- FlexGUI can now be used to read or write any authorized registers.
  Below is an example of registers contents:



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Get regulators and IO values from IOs tab: