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Layerscape LS1012A Freeway (FRWY-LS1012A) Board Reference Manual

Document Number: FRWY-LS1012ARM
Rev. 0, 04/2018

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Chapter 1
Overview

1.1 Introduction

The Layerscape LS1012A Freeway (FRWY-LS1012A) board is an ultra-low-cost development platform for LS1012A. The board provides connectivity support for SPI, UART, and I2C based mikroBUS™ connector. Also, the FRWY-LS1012A supports 512 MB of DDR3L memory, two 1 Gbit/s Ethernet ports, one USB 3.0 port, Audio in/out and mic interface, and PCIe Gen1/2 M.2 Type E modules.

The dimensions of the board are 83x90 mm. (Figure 1-4). The system is lead-free and RoHS-compliant.

The LS1012A processor is built on the LS architecture combining one Arm® A53 processor core with the data path acceleration and network, peripheral interfaces required for networking, wireless infrastructure, and the general-purpose embedded applications.

The FRWY-LS1012A onboard resources and debugging devices allow you to:

- Upload and run code.
- Use the FRWY-LS1012A as a demonstration tool.

FRWY-LS1012A comes loaded with Layerscape SDK, which is the next generation of Linux enablement software for Layerscape family of processors. It provides all the necessary drivers, tools and libraries required to enable all features of the Arm® based Layerscape processors.

1.2 Related documentation

Table 1-1 lists the additional documents that you can refer to, for more information about the FRWY-LS1012A.

Some of these documents may be available only under a non-disclosure agreement (NDA). To request access to these documents, contact your local NXP field applications engineer or sales representative.

Table 1-1. Related documentation

Document	Description
QorIQ FRWY-LS1012A board Getting Started Guide	Explains the FRWY-LS1012A settings and physical connections needed to boot the board.
FRWY-LS1012A Errata	Lists and describes all known errata for the FRWY-LS1012A. It also describes the available workaround for each errata and their detailed explanation, where necessary.
QorIQ LS1012A Family Reference Manual	Provides a detailed description of the LS1012A processor and of some of its features, such as memory mapping, interfaces, chip features, and clock information.
QorIQ LS1012A Data Sheet	Contains the LS1012A information on pin assignments, electrical characteristics, package information, and ordering information.
LS1012A Chip Errata	Lists the details of all known silicon errata for LS1012A.
QorIQ LS1012A Design Checklist, AN5192	This document provides recommendations for new designs based on LS1012A. This document can also be used to debug newly-designed systems by highlighting those aspects of a design that merit special attention during initial system start-up.

1.3 Acronyms and abbreviations

The following table lists the acronyms and abbreviations used in this document.

Table 1-2. Acronyms and abbreviations

Term	Description
DDR	Double Data Rate
UART	Universal asynchronous receiver/transmitter
DUT	Device Under Test
FET	Field-effect transistor
GPIO	General-purpose input/output
I2C	Inter-Integrated Circuit Multi-Master Serial Computer Bus
JTAG	Joint Test Action Group (IEEE 1149.1 standard)
LDO	Low-dropout
NGFF	Next Generation Form Factor
OTG	On-The-Go
PCIe	Peripheral Component Interconnect Express
PLL	Phased Lock Loop

Table continues on the next page...

Table 1-2. Acronyms and abbreviations (continued)

Term	Description
PS	Power supply
PSU	Power supply unit
RCW	Reset Configuration Word
SDA	Serial data line
SerDes	Serializer/deserializer used to interface with serial interfaces, such as PCIe, SGMII, and SATA
SGMII	Serial Gigabit Media Independent Interface
SPI	Serial Peripheral Interface
USB	Universal Serial Bus

1.4 FRWY-LS1012A features

The following table lists the features of the FRWY-LS1012A.

Table 1-3. FRWY-LS1012A features

Feature	Specification	Description
Processor	LS1012A processor	LS1012A processor with single core[1]
High-speed serial ports (SerDes)	3 SerDes lanes with speed up to 5 Gbit/s	• 2 SGMII 1G PHYs • 1 M.2 Type-E NGFF slot
DDR controller	One 512 MB DDR3L SDRAM memory	• 512 MB memory • Supports data rates up to 1000 MT/s • Operates at 1.35 V
Ethernet	Two Ethernet PHYs	• Two quad-speed Ethernet PHYs supporting SGMII 1G with RJ45 connectors for 1000BaseT connectivity
USB 2.0/3.0	One SuperSpeed USB 2.0/3.0 port, one USB 2.0 port	• USB 2.0/3.0 port is configured as On-The-Go (OTG) with a Micro-AB connector • USB 2.0 port is a debug port (CMSIS DAP) and is configured as a Micro-AB device
SPI	SPI	• SC16IS740IPW SPI to Dual UART bridge • mikroBUS™ host connector
QSPI	One QSPI controller	• Onboard combo flash of 16 Mbit serial NOR + 1 Gbit serial NAND QSPI memory for boot image. The data transfer speed for NOR flash memory is 50 MB/s and for NAND the speed is 40 MB/s
SDHC	One SDHC1 controller	• Onboard SDHC connector to connect the microSD cards
M.2 Type-E NGFF slot		• 1 M.2 Type-E NGFF slot
Serial ports	UART (Console) 1 UART (from SC16IS740IPW)	• UART1 (without flow control) for console • 1 UART (without flow control) from SC16IS740IPW (SPI to UART Bridge) to mikroBUS host connector
SAI	Audio interface	• One SAI port, SAI 2 with full duplex and mic support

Table continues on the next page...

Table 1-3. FRWY-LS1012A features (continued)

Feature	Specification	Description
I2C		• One I2C bus with connectivity to mikroBUS click headers and audio device
Debug features		• Arm Cortex® 10-pin JTAG connector for LS1012A • CMSIS DAP through K20 microcontroller
Package		• Package type is 9.6 mm x 9.6 mm x 0.805, 211 Flip Chip Land Grid Array (FC-LGA)
Clocks		• 25 MHz Oscillator for LS1012A • 25 MHz Oscillator for audio codec • 25 MHz crystals for 2 SGMII PHYs • 100 MHz reference clock for M.2 NGFF slot • 8 MHz Crystal for K20 • 24 MHz for SC16IS740IPW SPI to Dual UART bridge
Power supplies		• 5 V input supply from power adapter • 0.9 V, 1.35 V, and 1.8 V for VDD/Core, DDR, I/O, and other board interfaces

1. For details about features of the LS1012A SoC, see *QorIQ LS1012A Family Reference Manual*.

1.5 FRWY-LS1012A block diagram

Figure 1-1 shows the FRWY-LS1012A block diagram.

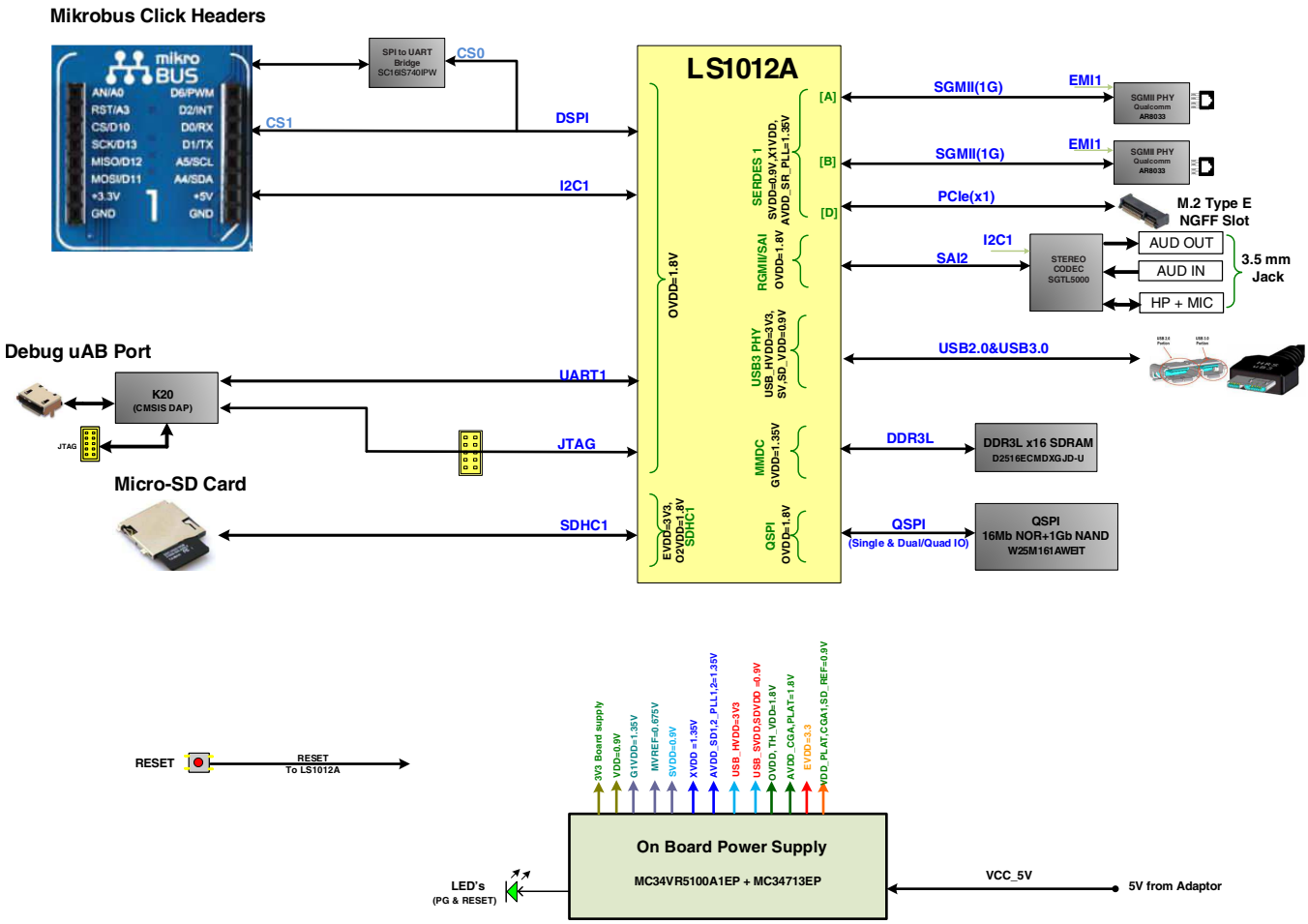

Figure 1-1. FRWY-LS1012A block diagram

1.6 FRWY-LS1012A board interface

The following figures shows the top and bottom views and assembly layout of the FRWY-LS1012A board.

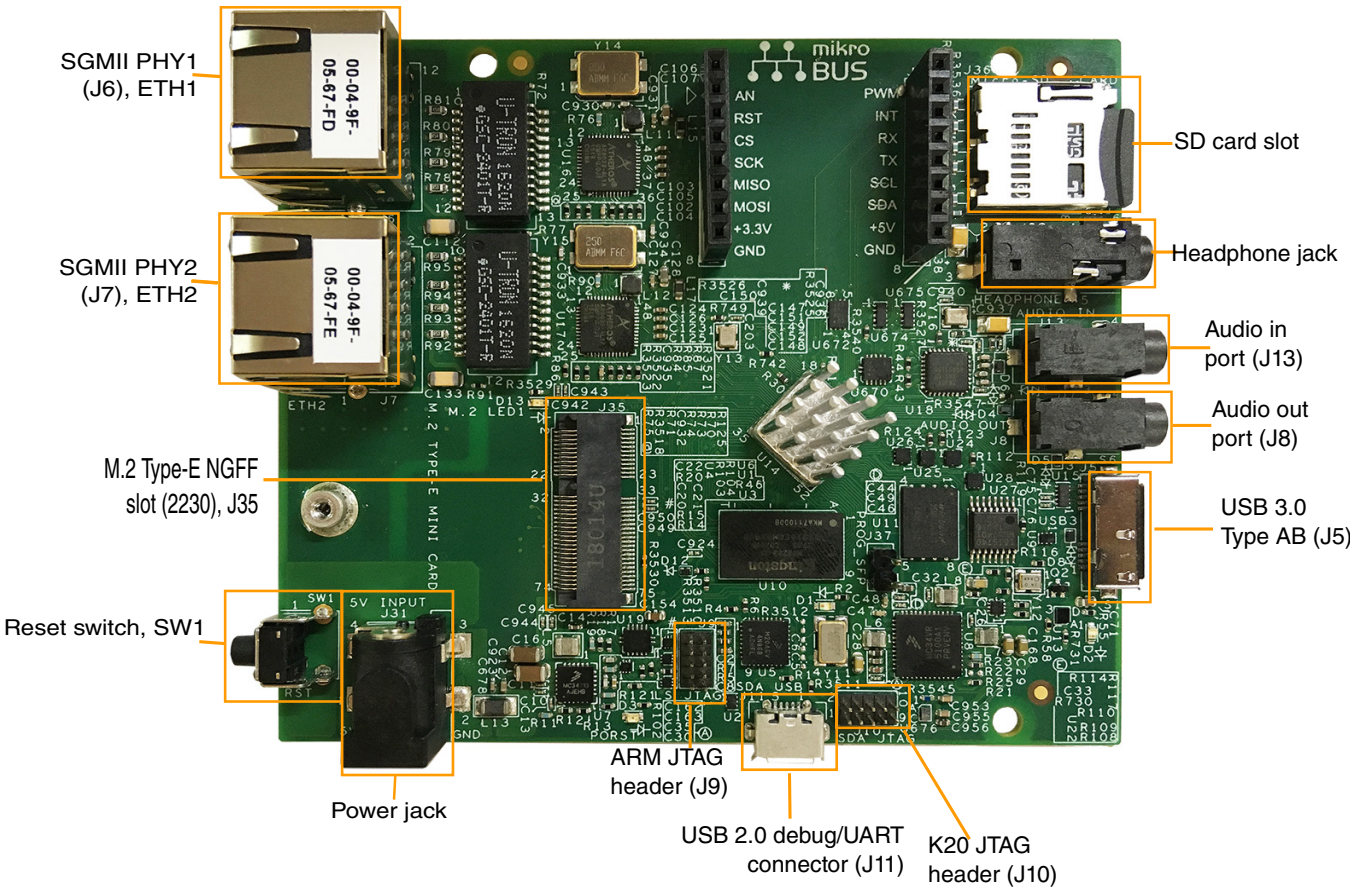

Figure 1-2. FRWY-LS1012A top view

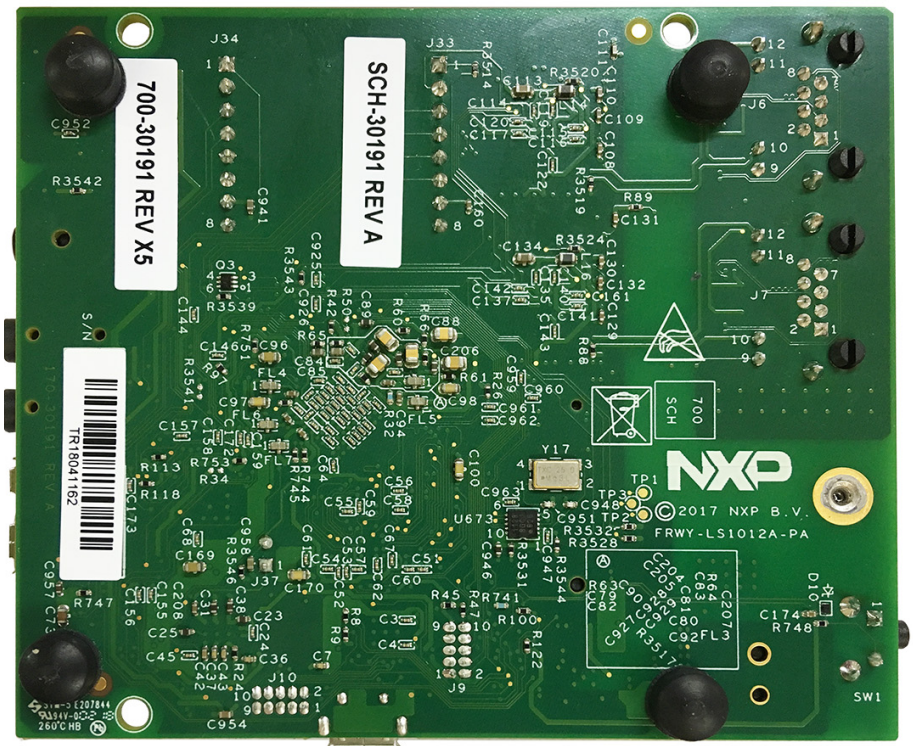

Figure 1-3. FRWY-LS1012A bottom view

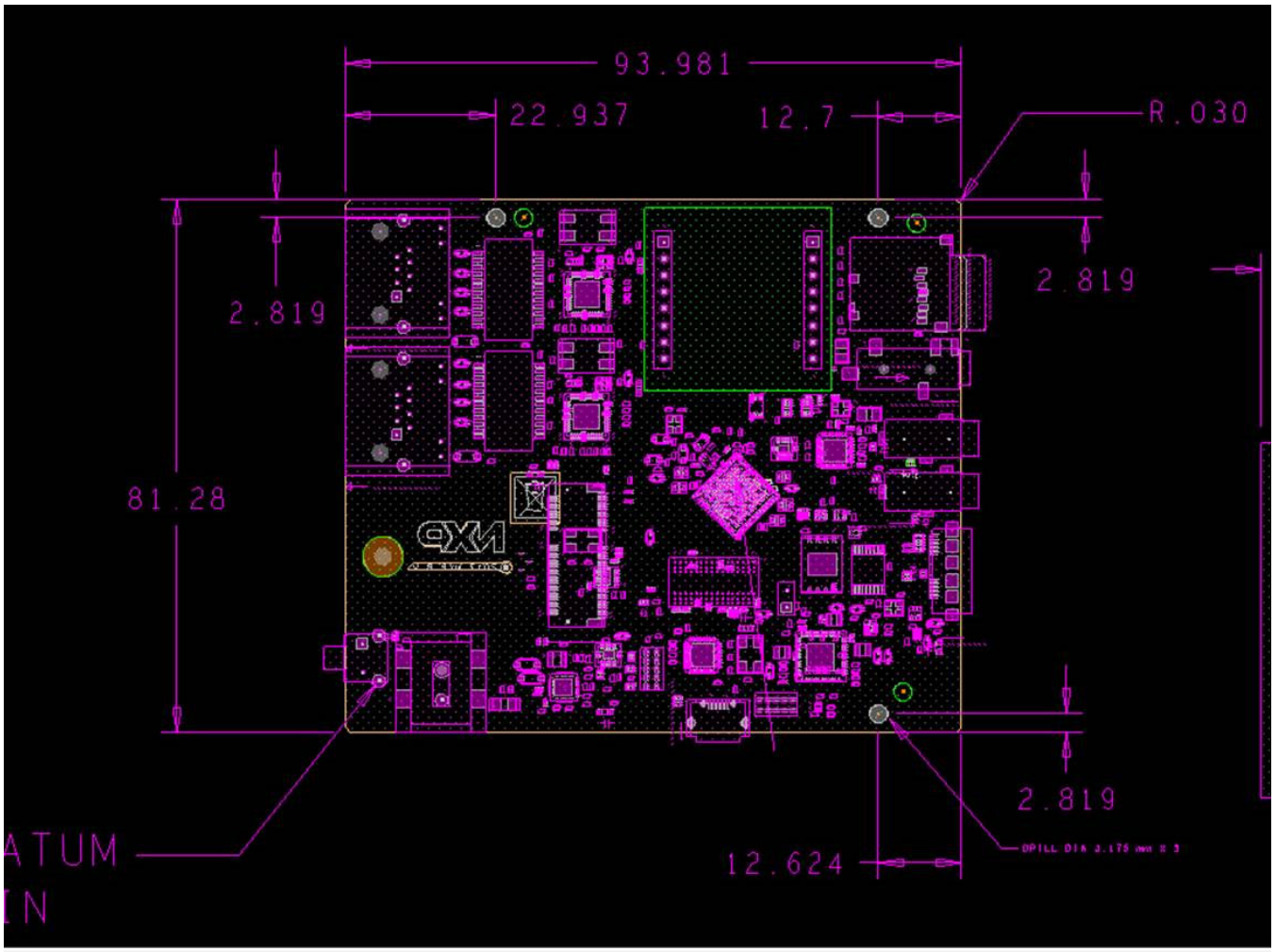

Figure 1-4. FRWY-LS1012A assembly layout (Dimensions are in 'mm')

Chapter 2
FRWY-LS1012A Functional Description

2.1 Processor

The FRWY-LS1012A includes the QorIQ LS1012A processor that features an advanced 64 bit Arm® Cortex®-A53 processor core with ECC-protected L1 and L2 cache memories. The LS1012A also features data path acceleration and network, peripheral interfaces required for networking, wireless infrastructure, and general purpose embedded applications.

NOTE

For details about features of the LS1012A processor, see *QorIQ LS1012A Family Reference Manual*.

2.2 Power supplies

The FRWY-LS1012A power supplies (PS) provide all the voltages necessary for the correct operation of the LS1012A processor, DDR3L, QSPI memory, and other onboard peripherals.

The following figure shows the FRWY-LS1012A power supplies.

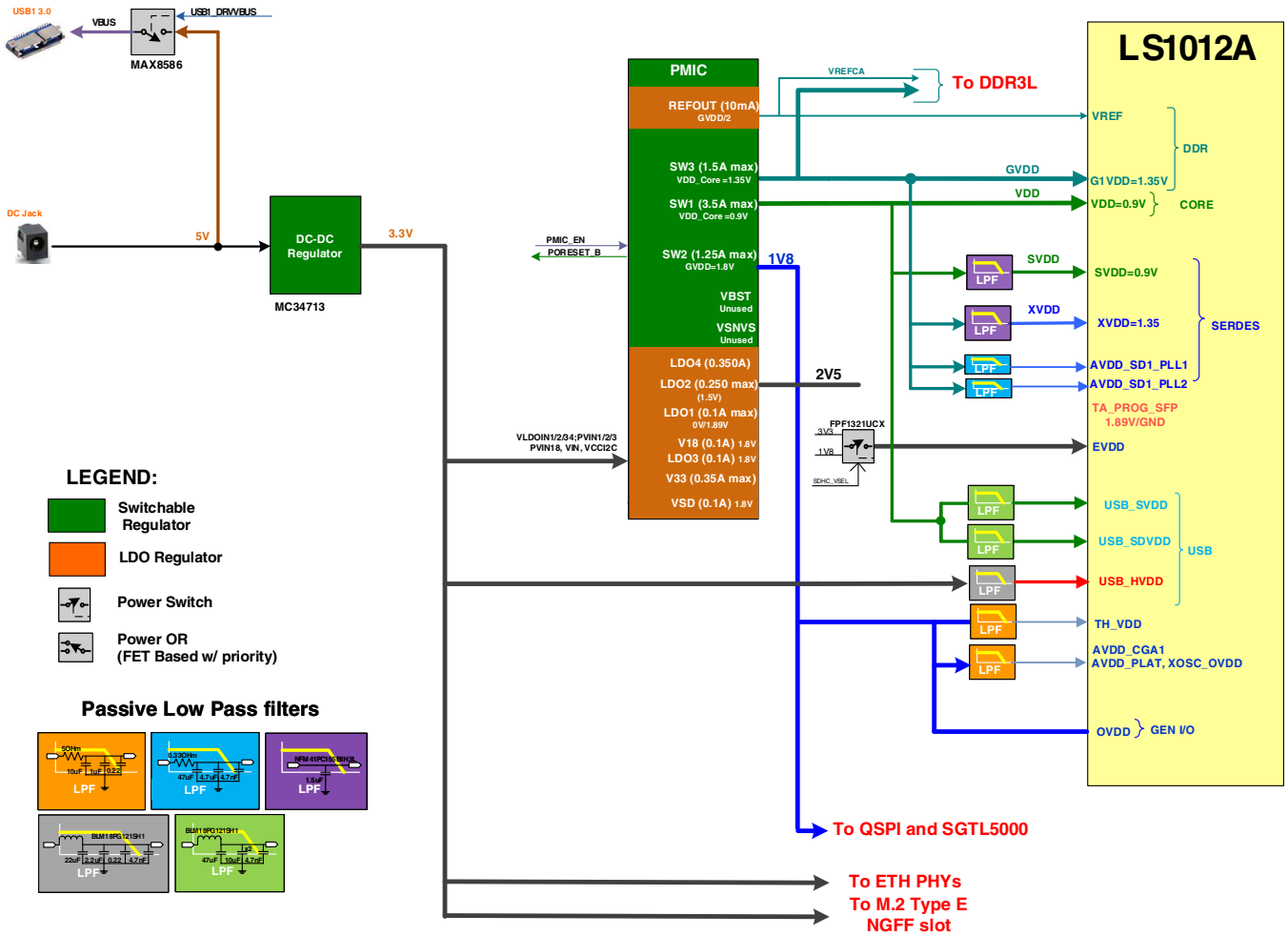

Figure 2-1. FRWY-LS1012A power supplies

2.2.1 Primary power supply

The FRWY-LS1012A is powered through the 5 V DC power adapter.

The total power required from the power adaptor depends on devices used by an application.

Recommended power supply options:

1. Part number: GST25U05-P1J, Manufacturer: MEANWELL

   https://www.mouser.com/ProductDetail/MEAN-WELL/GST25U05-P1J?qs=drgMNd%252bkGPOZrVF%252b%252bRnYJg==

2. Part number: ATS024T-A050, Manufacturer: ADAPTER TECHNOLOGY CO

http://www.adaptertech.com.tw/24-Watt-ATS024-Series.html?CID=1

The specifications of the DC adapter are as follows:

- **Input:** 100/240 V AC, 50-60 Hz
- **Output:** 5 V, 4 A DC power supply adapter (20 W) - Standard
- **Connector Size:** 5.5 mm (Outside barrel) x 2.1 mm (Inside Barrel), Center positive

The DC jack can provide power up to 3.5 A at 5 V.

Refer to the following table for the estimated power required by each of the board interface.

SL NO	Description	Power (W)/ QTY	0.9V	1.35V	1.8V	3.3V	5V	QTY	Total Power		Remarks/ Queries
1	LS1012A	1						1	1		Power of 1W assumed.
2	AR8033 SGMII	0.42						2	0.84		420mW exah phy in 1G SGMII - UTP
3	SGTL5000	0.00867						1	0.00867		
4	DDR3L (Worst case current IDD4R)	0.297						1	0.297		220mA for burst read in 1000MT/s for each x16.
5	QSPI memory	0.045						1	0.045		25mA @ 1.8V
6	K22 MCU	0.0627						1	0.0627		19mA @ 3.3V when executing from flash.
7	Misc (5 SSD @13mA)	0.117						1	0.117		For other componenets
8	M.2 Type E NGFF Slot	5						1	5		
9	USB3.0	5						1	5		
10	miKro bus click	0.726						1	0.726		
11	SD Card	0.264						1	0.264		
	Total Power								13.36037		
	Power from 5V with efficiency of	80%							16.7004625	Watt	
	Current @5V								3.3400925	A	from 5V, 3.5A DC Adaptor

Figure 2-2. Power estimation

2.2.2 FRWY-LS1012A power supply delivery system

The following table lists the different power supply components used to generate the various FRWY-LS1012A power supply rails.

Table 2-1. FRWY-LS1012A power supply devices

Source voltage rail	Output voltage rail	Reference designator	Vendor	Device	Description
5V_INP	VCC_5V	J31		DC power jack	5 V at 3.5 A power supply for onboard DC regulator
VCC_5V	VCC_3V3	U7	NXP	MC34713EP	3.3 V at 3.2 A power supply for: • secondary regulator VR5100, • onboard SGMII PHYs, • and LS1012A supplies: EVDD and USB_HVDD • NGFF slot

Table continues on the next page...

Table 2-1. FRWY-LS1012A power supply devices (continued)

Source voltage rail	Output voltage rail	Reference designator	Vendor	Device	Description
VCC_3V3	VCC_0V9 VCC_1V8 VCC_1V35 VCC_VREF VCC_POVDD VCC_2V5 VCC_EVDD	U8	NXP	MC34VR5100A1EP	Power supply for: • LS1012A power supplies • 1.35 V for DDR3L memory • SerDes, USB • 1.8 V voltage for QSPI memory, SAI2 port, general I/O • 2.5 V for Ethernet PHYs

2.2.3 Power-ON

The FRWY-LS1012A is powered using 5 V DC power adapter through a DC power jack.

The DC power adapter provides 5 V DC voltage. The 5 V voltage powers primary power supply regulator U7. U7 provides power supply to the secondary regulator U8, the onboard SGMII PHYs, and the NGFF slot. The secondary regulator, U8, generates power supply for peripherals, such as QSPI flash memory and LS1012A power supplies.

Table 2-2 describes the Power-ON sequence as implemented on the FRWY-LS1012A.

Table 2-2. Power-ON process

Step	Indication	Specifics	Description
1		5V	• Power supply provided by DC Jack, J31 • Acts as source PS for secondary regulator MC34713
2		3V3	• 3.3 V power supply for onboard SGMII PHYs and LS1012A supplies: EVDD and USB_HVDD • Acts as source PS for secondary regulators VR5100
3		1V8, 1V35	Power supplies provided by secondary regulator VR5100 • Provides power to peripherals and LS1012A IO and PLL supplies (AVDD_PLAT, AVDD_CGA1, TH_VDD, AVDD_SD1_PLL1, AVDD_SD1_PLL2, OVDD, XOSC_OVDD, USB_SVDD, USB_SDVDD, G1VDD, VREF, SVDD, and XVDD)
4		0V9	• LS1012A core supplies: VDD
5	Red LED (D3)		• Reset LED is deasserted.

2.2.4 Voltage regulation

The following table explains the FRWY-LS1012A voltage regulation.

Table 2-3. FRWY-LS1012A Voltage Regulation

Power	Voltage	Device	Description
Core, VDD	0.9 V (3.5 A max)	VR5100 SW1	Powers the LS1012A SoC Core voltage
G1VDD	1.35 V (1.5 A max)	VR5100 SW3	Powers the LS1012A SoC DDR circuitry
VCC_VREF	0.675 V	VR5100 VREF LDO	
XVDD	1.35 V	VR5100 SW3	Powers the LS1012A SoC SerDes I/O circuitry
AVDD_SD1_PLL1 AVDD_SD1_PLL2			
SVDD	0.9 V	VR5100 SW1	
TH_VDD	1.8 V (1.25 A max)	VR5100 SW2	Thermal monitor unit supply voltage
AVDD_CGA1 AVDD_PLAT			Core, Platform, DDR, and SerDes PLL supply voltages
XOSC_OVDD			OVDD supply for LS1012A crystal oscillator
OVDD			General I/O voltage
USB_SVDD USB_SDVDD	0.9 V	VR5100 SW1	Powers the LS1012A SoC USB circuitry
USB_HVDD	3.3 V	MC34713	
EVDD	3.3 V	MC34713	
VCC_2V5	2.5 V (0.350 A max)	VR5100 LDO4	Powers the 1.8 V to 2.5 V level translator for EMI1_MDC, EMI1_MDIO
VCC_POVDD	1.8 V	VR5100 LDO1	Powers the LS1012A SFP fuse programming voltage

2.3 Reset and configuration signals

The reset sequence can be triggered from various sources.

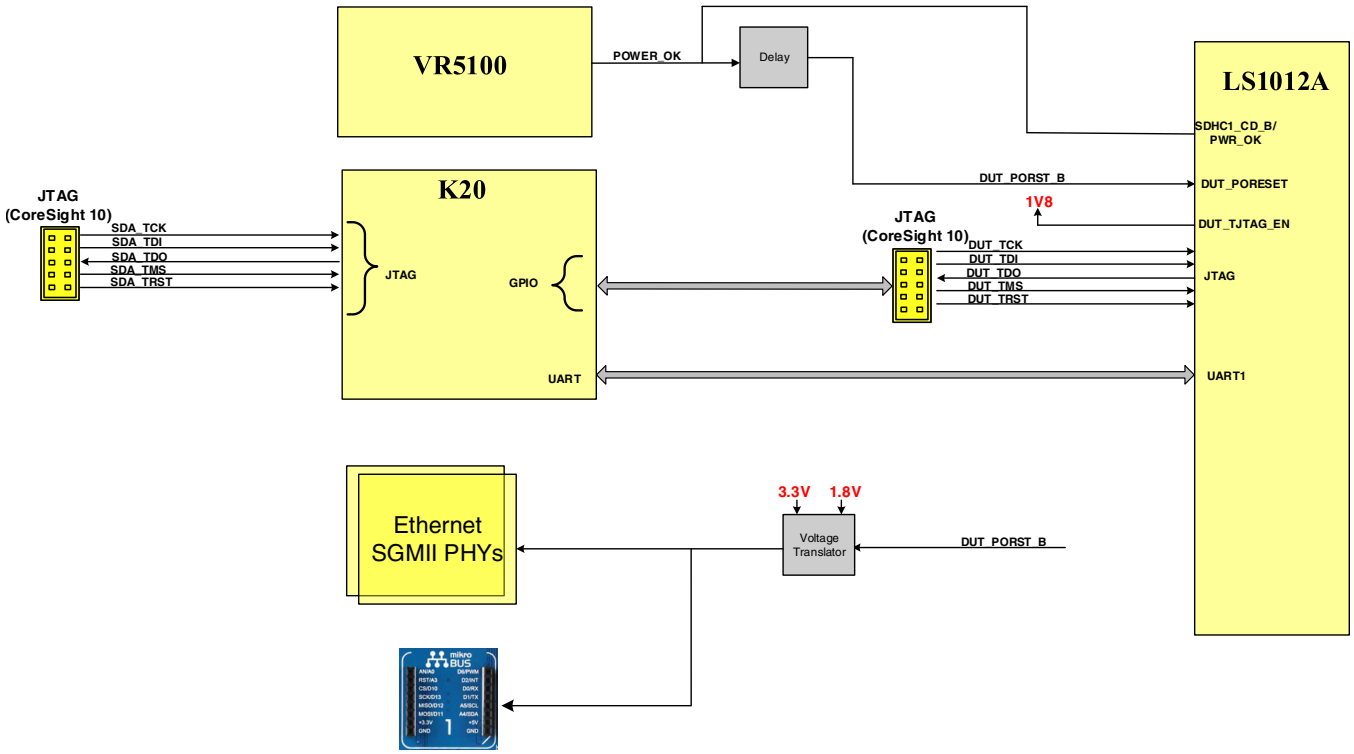

Figure 2-3. FRWY-LS1012A reset architecture

Table 2-4 summarizes the reset activity.

Table 2-4. Reset activity

Reset Source	Reset Reason	Actions taken
Power ON	Initialization after a power cycle.	All the onboard devices are reset after a power cycle. PLL and clock circuitry initialize to the default configuration.
SW1	Reset switch	Resets LS1012A and other board peripherals. Enables the BOOTLOADER mode on the K20 CMSISDAP.
Debugger reset (J9 and K20)	Reset from JTAG debugger	No power cycle. All devices are reset.
RESET_REQ_B	Reset request from LS1012A	All devices are reset. No power cycle.

The reset is asserted for about 240 ms after all power supplies are stable to meet the LS1012A 100 ms reset specification. Power failure after system operation also asserts the reset to all the devices on the board. The FRWY-LS1012A supports options to change the PORCFG through the resistor mount option. Mount the resistors to drive the corresponding PORCFG as low in Table 2-5.

Table 2-5. Configuration signals

Configuration signal	Nets sampled	Components on board	Default state
CFG_RCW_SRC1	CLK_OUT	R50	DNP

2.4 Clocks

The architecture of the FRWY-LS1012A clocks is shown in the following figure.

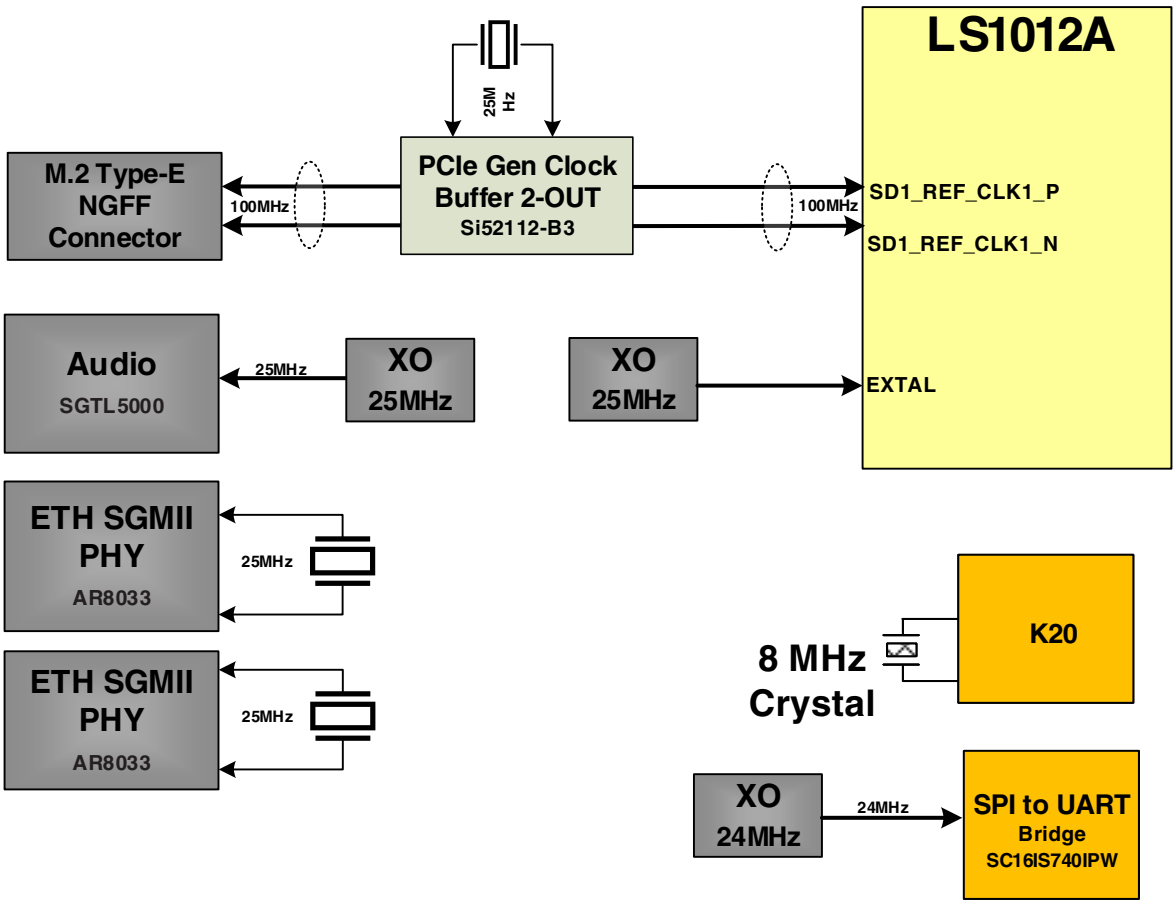

Figure 2-4. Clock architecture

The following table summarizes the FRWY-LS1012A clock distribution.

Table 2-6. FRWY-LS1012A clocks

Clock	Frequency	Destination	Device
EXTAL (Bypass mode)	25 MHz	Input clock for SoC	Oscillator
SD1_REF_CLK1_P/N	100 MHz	Reference clock for LS1012A SerDes controller	25 MHz crystal clock and PCIe clock generator, Si52112-B3: • 2 output PCIe Gen1 Clock Generator • Low power consumption • Phase jitter - 1.4 ps • Skew outputs - 60 ps • Output clock frequency (min/max) - 100 MHz
PEXM2_REFCLK_P/N	100 MHz	Reference clock for NGFF Slot	
ETH1_XTALIN, ETH1_XTALOUT	25 MHz	Crystal clock for the SGMII PHY1	Crystal

Table continues on the next page...

Table 2-6. FRWY-LS1012A clocks (continued)

Clock	Frequency	Destination	Device
ETH2_XTALIN, ETH2_XTALOUT	25 MHz	Crystal clock for the SGMII PHY2	
CODEC_SYS_MCLK	25 MHz	System clock for audio codec	
8 MHz XTAL for K20	8 MHz	Crystal clock for K20	Crystal
BRDG_CLKIN_24MHz	24 MHz	Clock for SC16IS740IPW SPI to Dual UART bridge	Oscillator

2.5 Double data rate (DDR) memory

The FRWY-LS1012A is supplied with one 16-bit, 512 MB DDR3L SDRAM memory, running at data rates up to 1000 MT/s. The part number is D2516ECMDXGJD-U from Kingston Technology.

Following are the characteristics of the LS1012A DDR3L memory controller:

- Up to 1.0 GT/s
- Supports 16 bit operation (no ECC support)
- Support for x8, x16 devices
- Supports 1 chip select, D1_MCS_B

The VR5100 VREF LDO (U8) takes 1.35 V supply and provides 0.675 V VREF supply to the DDR3L memory.

The memory interface includes all the necessary termination and I/O power, and is routed to achieve maximum performance of the memory bus.

2.6 Serializer/deserializer (SerDes)

The FRWY-LS1012A SerDes block provides three high-speed serial communication lane, supporting two SGMII PHYs and 1 M.2 Type-E NGFF slot. See QorIQ LS1012A Data Sheet for details about the SerDes protocols supported on the LS1012A processor. The following table lists the components used to support the different SerDes options.

Table 2-7. FRWY-LS1012A SerDes embedded devices

Manufacturer	Part number	Description	Lane supported	Speed
Qualcomm	AR8033	• SGMII 1G PHY	x1	1.25 Gbit/s
Qualcomm	AR8033	• SGMII 1G PHY	x1	1.25 Gbit/s

Table continues on the next page...

Table 2-7. FRWY-LS1012A SerDes embedded devices (continued)

Manufacturer	Part number	Description	Lane supported	Speed
ANYTRONIC CORPORATION LIMITED	1J0E 42010R-2LF	• M.2 Type-E NGFF NGFF slot	x1	5 Gbit/s

2.7 Ethernet controller

The LS1012A processor supports two Ethernet MACs, which connect to the onboard PHYs using the SGMII protocols.

2.7.1 SGMII ports

The onboard Ethernet PHYs, Qualcomm AR8033 (U16 and U17), are connected to the LS1012A processor EC1 and EC2 using the SGMII protocol over SerDes lane A and SerDes lane B.

Notes and Assumptions:

- MAC connected to Serdes lane B is the same MAC connected to the RGMII interface. so RGMII and SGMII (lane B) can not be use at a time.
- If the Serdes is configured for 2 SGMII interfaces, then the RGMII interface is unused (tristated unless the pinmuxing control register is configured for functionality other than EC1 RGMII).

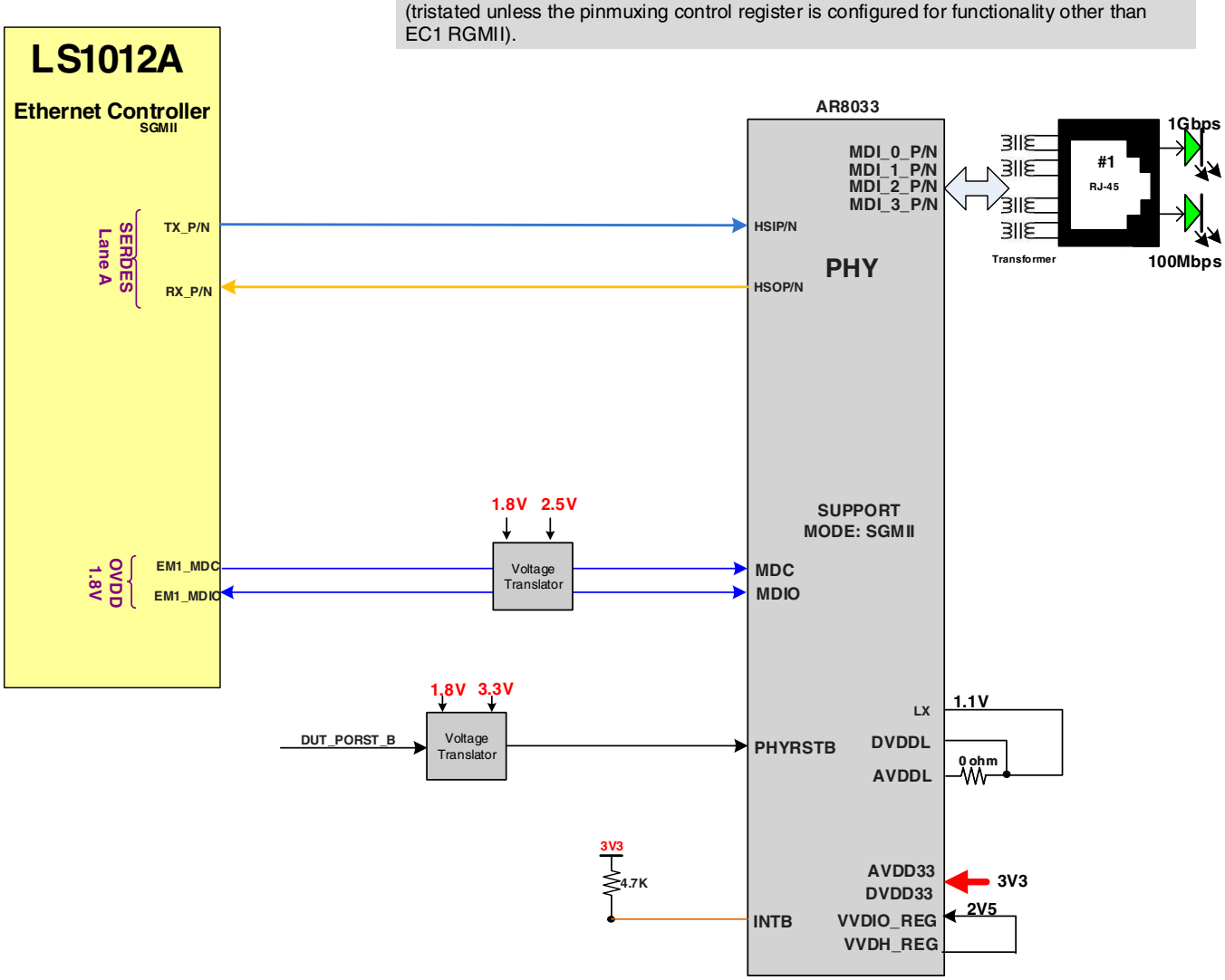

Figure 2-5. SGMII PHY1

Notes and Assumptions:

- MAC connected to Serdes lane B is the same MAC connected to the RGMII interface. so RGMII and SGMII (lane B) can not be use at a time.
- If the Serdes is configured for 2 SGMII interfaces, then the RGMII interface is unused (tristated unless the pinmuxing control register is configured for functionality other than EC1 RGMII).

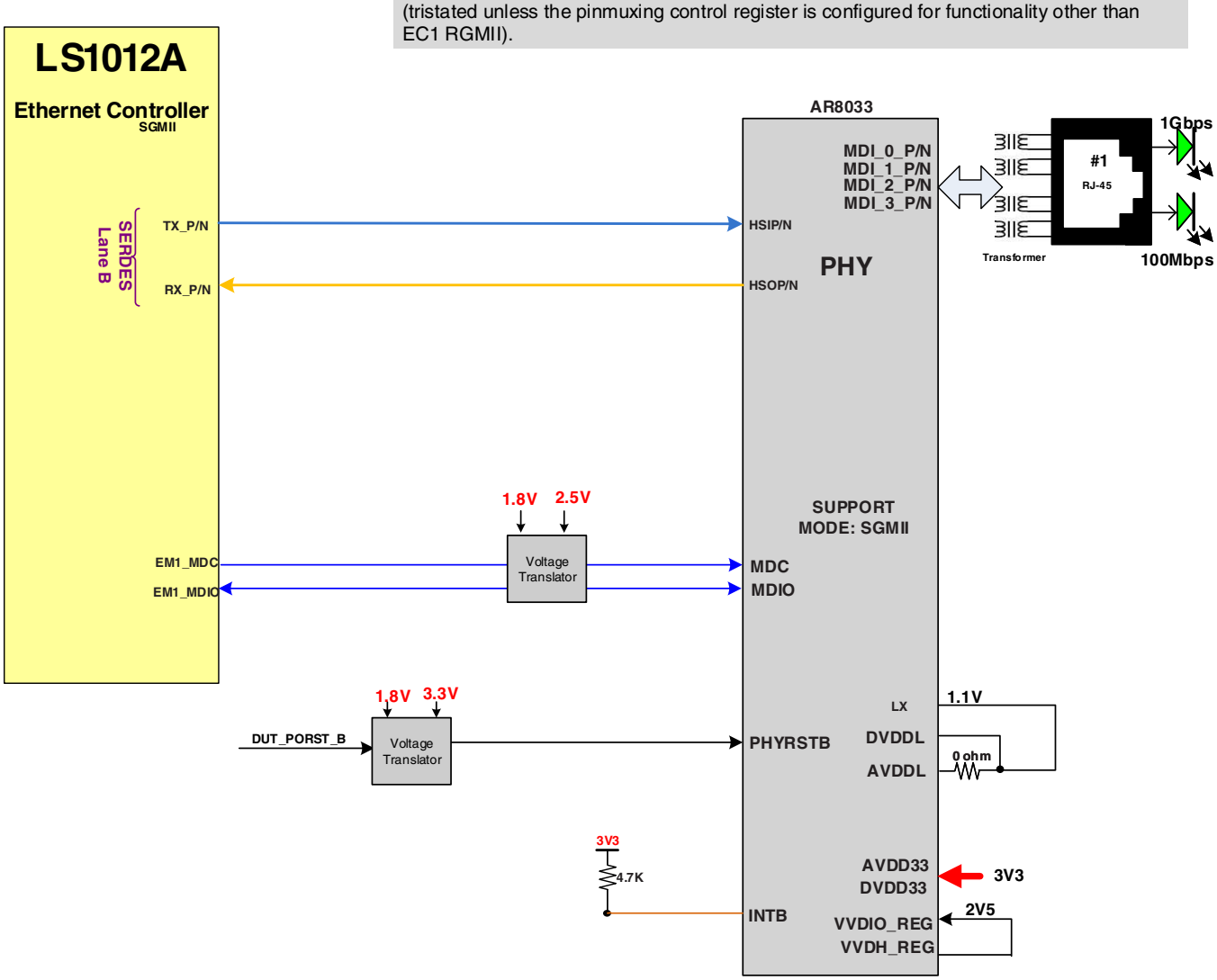

Figure 2-6. SGMII PHY2

Table 2-8. Hardware bootstrap settings for Ethernet PHYs

Setting	Description
PHY_AD[2:0] = 010 (for SGMII PHY1)	PHY Addr = 0b00010 (for SGMII PHY1)
PHY_AD[2:0] = 001 (for SGMII PHY2)	PHY Addr = 0b00001 (for SGMII PHY2)
MODE[3:0]=0001	SGMII <=> UTP (1000 BASE-T, SGMII)

2.8 M.2 Type-E NGFF slot

The FRWY-LS1012A supports 1 M.2 Type-E NGFF slot connected to LS1012A through the SerDes lane D.

The onboard M.2 NGFF onnector supports only 1630, 2230 M2 Type E cards.

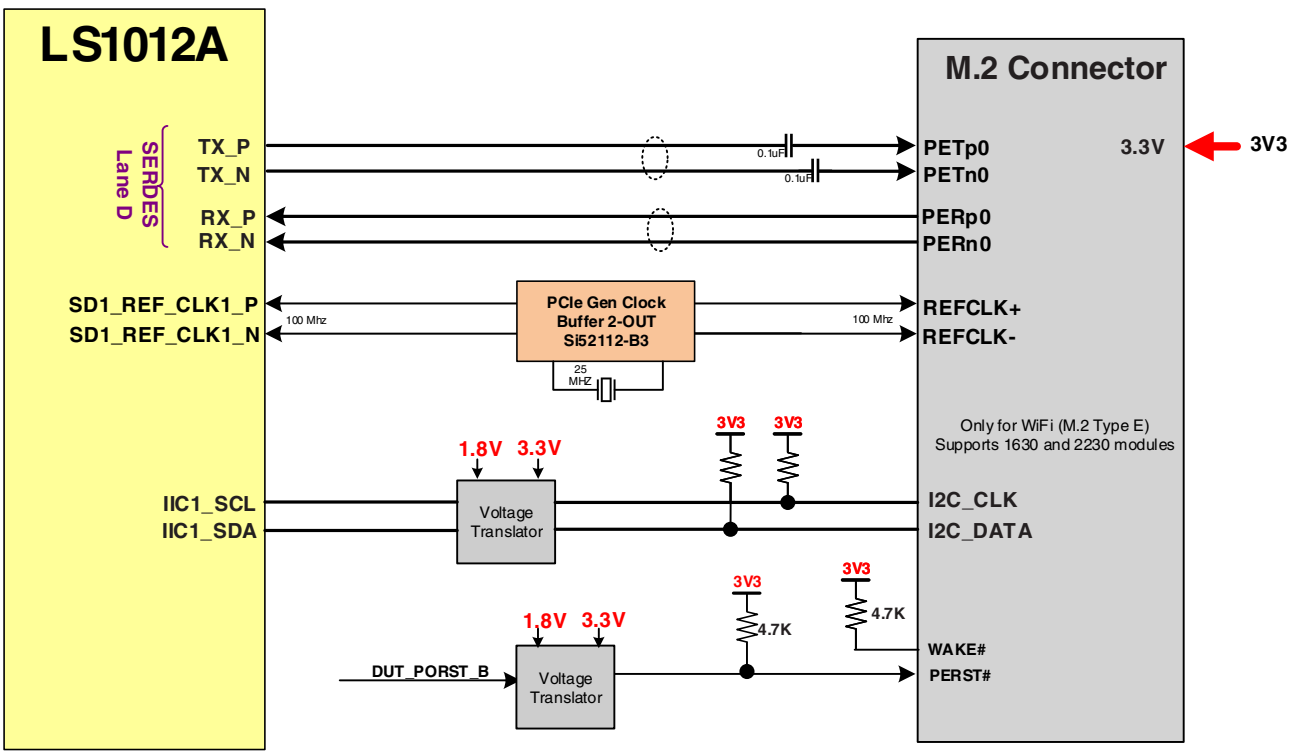

Figure 2-7. NGFF slot

2.9 Audio interface

The FRWY-LS1012A board supports 3.5mm jack for audio and mic interface using the SGTL5000 codec. This codec connects with LS1012A on the SAI2 interface.

SAI2 supports full duplex audio and takes bit clock (TX and RX BCLK) and frame clock (TX and RX SYNC) as input from SGTL5000. The SGTL5000 generates these clocks based on a 25 MHz MCLK, which is fed from the 25 MHz crystal clock. The SGTL5000 control interface is I2C-based and can be accessed at the 0x0A address.

2.10 USB interface

The FRWY-LS1012A board supports one SuperSpeed USB 2.0/3.0 port - configured as On-The-Go (OTG) with a Micro-AB connector. Based on the OTG configuration, the PHY can either operate in the Type-A or Type-B mode.

The following figure shows the USB 2.0/3.0 PHY architecture on the FRWY-LS1012A.

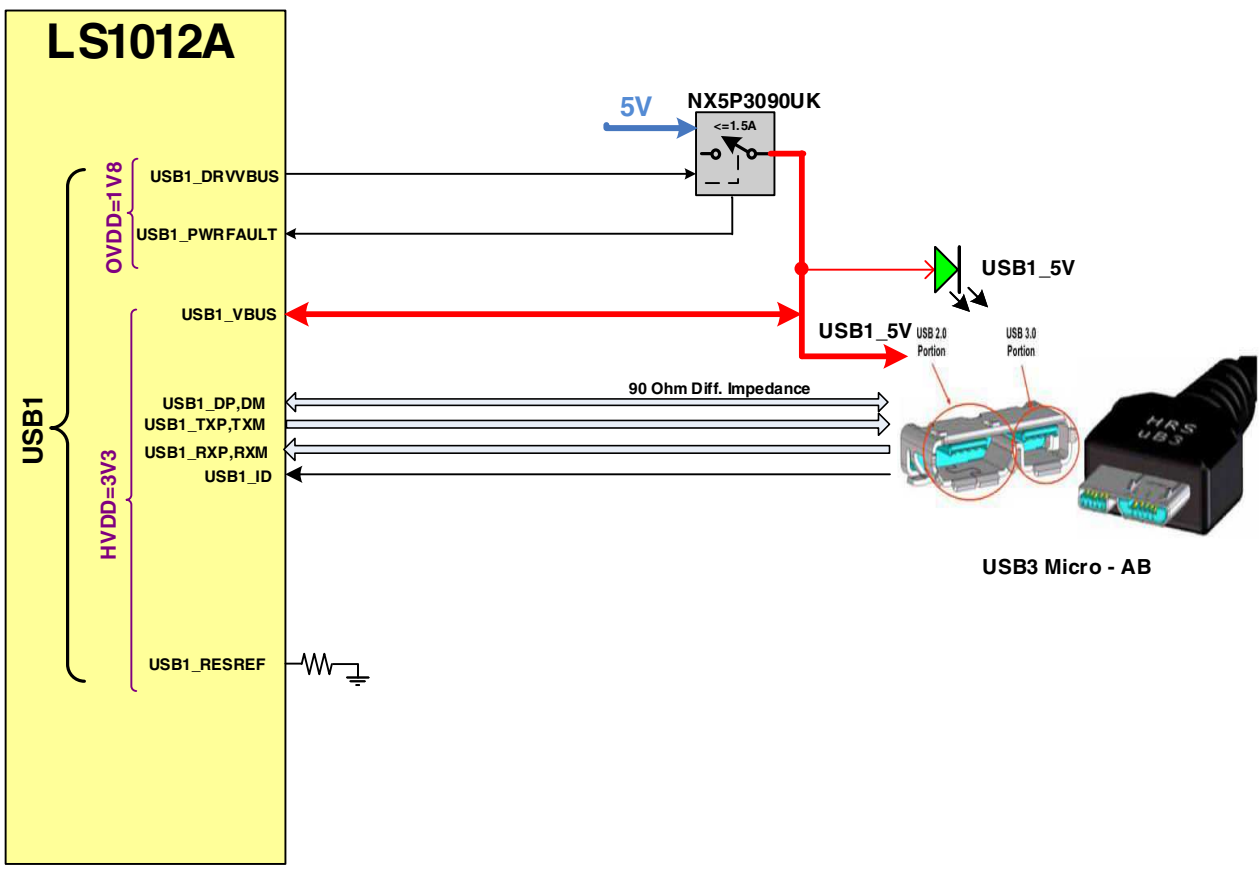

Figure 2-8. USB 2.0/3.0 PHY architecture

2.11 I²C ports

The FRWY-LS1012A support one I2C bus:

- The LS1012A I2C1 is attached to the local devices on the FRWY-LS1012A.
- The level shifter device (NTSX2102GU8H) is used on the FRWY-LS1012A I2C1 bus, to convert the LS1012A 1.8 V to 3.3 V signals for the I2C devices, on the mikroBUS click connectors.
- The I2C1 bus has one possible master - LS1012A processor.