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JTAG-Booster for IDT RC64145



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1. General

The program JTAG145 uses the JTAG port of the IDT RC64145 embedded controller in conjunction with the small JTAG-BOOSTER:

- to program data into flash memory
- to verify and read the contents of a flash memory
- to make a memory dump
- to access an I²C Device
- to test CPU signals

All functions are done without any piece of software running in the target. No firmware or BIOS must be written. Bootstrap software may be downloaded to initially unprogrammed memories.

For latest documentation please refer to the file README.TXT on the distribution disk.

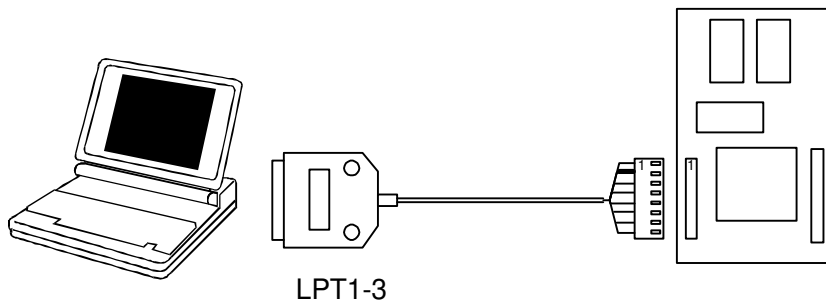
1.1. System Requirements

To successfully run this tool the following requirements must be met:

- MSDOS, WIN3.x, WIN9x or WinNT
(WinNT is supported with an additional support-kit)
- Intel 80386 or higher
- 205 kByte of free DOS memory
- no extended memory
- Parallel Port

1.2. Connecting your PC to the target system

The JTAG-Booster can be plugged into standard parallel ports (LPT1-3) with a DB25-Connector.



The target end of the cable has the following reference:

1	2*	3	4	5	6	7	8
TCK	GND	TMS	TRST#	NC	TDI	TDO	+3.3V

*PIN 2 can be detected by the white thick cable.

To connect your design to the JTAG-BOOSTER you need a single row berg connector with a spacing of 2.54mm on your PCB. The names refer to the target: Pin 7 is the **target's** TDO pin and is connected to the JTAG-Booster's TDI pin.

Since the JTAG-Booster operates with 5V, in addition a level shifter is necessary to connect the JTAG-Booster to a target operating with 3.3 volts. This level shifter must be ordered separately.

The IDT RC64145 does not have a TRST# pin. The reset of the JTAG interface is connected (internally to the IDT RC64145) to the system reset (Pin SYS_RST#). We recommend **not** to connect the system reset with the TRST# pin of the JTAG connector. For more information see chapter 3. "Implementation Information"

Before you start the program, the JTAG-BOOSTER must be plugged to a parallel interface of your PC and to the 8 pin JTAG connector on the target.

The utility is started with the general command line format:

```
JTAG145 /function [filename] [/option_1] ... [/option_n].
```

Note that the function must be the first argument followed (if needed) by the filename.

If you want to cancel execution of JTAG145, press CTRL-Break-Key.

On any error the program aborts with an MSDOS error level of one.

1.3. First Example

In the following simple example it is assumed that the JTAG-Booster is connected to LPT1 of your PC and target power is on.

Typing

```
JTAG145 /P MYAPP.BIN /VERIFY
```

at the DOS prompt results in the following output:

```
JTAG145 --- JTAG utility for IDT RC64145 (32bit)
Copyright © FS FORTH-SYSTEME GmbH, Breisach
Version 3.00 of mm/dd/yyyy

(1) Configuration loaded from file JTAG145.INI
(2) Target: Generic Target
(3) Using LPT at I/O-address 0378h
(4) JTAG Adapter detected

(5) 1 Device detected in JTAG chain
    Device 0: IDCODE=00004067 IDT RC64145, Revision 0
(6) Sum of instruction register bits : 4
(7) CPU position                    : 0
(8) Instruction register offset     : 0

(9) AMD 29LV640 (word mode) detected
(10) Erasing Flash-EPROM Block #:0
    Programming File MYAPP.BIN
    65536 Bytes programmed
    Programming ok

Erase Time   :      2.5 sec
Program Time :     60.7 sec
```


- (1) The initialization file JTAG145.INI was found in the current directory.
- (2) The target identification line of the initialization file is printed here.
- (3) The resulting I/O-address of the parallel port is printed here.
- (4) A JTAG-Booster is found on the parallel port
- (5) The JTAG chain is analyzed. There may be several parts in the JTAG chain. The chain is analyzed and all parts except the IDT RC64145 are switched to bypass mode.
- (6) The length of all instruction registers in the JTAG chain are added.
- (7) The position of the IDT RC64145 in the JTAG chain is checked.
- (8) The position of the JTAG instruction register of the IDT RC64145 is checked
- (9) One Flash-EPROMs AMD 29LV640 selected with chip select BOOTCS# is found.
- (10) In this example one block must be erased.

1.4. Trouble Shooting

Avoid long distances between your Host-PC and the target. If you are using standard parallel extension cable, the JTAG-BOOSTER may not work. Don't use Dongles between the parallel port and the JTAG-BOOSTER.

Switch off all special modes of your printer port (EPP, ECP, ...) in the BIOS setup. Only standard parallel port (SPP) mode is allowed.

On very fast PCs there could be verify errors. To avoid this, watch for the 'IO recovery time'-switch in the BIOS Setup which must be turned on. Otherwise try to slow down your PC by setting the turbo switch off.

When using older flash devices (nearly maximum erase cycles reached), we propose to use the /VERIFY option. This is also true for the relatively slow 3 Volt only flash devices.

Some newer fast flash devices need a setup time between address/data and the write strobe signal. If programming of this devices fails, try with the option /WRSETUP again.

If there are problems with autodetection of the flash devices use the /DEVICE= option. To speed up autodetection specify the option /16BIT or /8BIT.

Don't use hardware protected flash memories.

The used chip selects must be defined as output and inactive in the initialization file (see chapter 1.6 "Initialization file JTAG145.INI"). Also the address bits must be defined as output.

1.5. Error Messages

- **80386 or greater required**
The JTAG-BOOSTER does not work on a 8088/8086 or a 80286 platform.
- **Adapter not connected or target power fail**
The JTAG-Booster wasn't found. Please check connection to parallel port and connection to target. Check target power. Check your BIOS-Setup.
- **Can't open x:\yyy\zzz\JTAG145.OVL**
The overlay file JTAG145.OVL must be in the same directory as JTAG145.EXE.
- **Configuration file XYZ not found.**
The file specified with the option /INI= wasn't found.
- **Device offset out of range**
The value specified with the option /OFFSET= is greater than the size of the detected flash device.
- **Disk full**
Writing a output file was aborted as a result of missing disk space.
- **Error creating file:**
The output file could not be opened. Please check free disk space or write protection.
- **Error: *Pin-Name* is an output only pin**
The specified pin cannot be sampled. Check the command line. Check the initialization file.
- **Error: *Pin-Name* is an input only pin**
The specified pin cannot be activated. Check the command line. Check the initialization file.
- **Error: *Pin-Name* may not be read back**
The specified pin can be switched to tristate, but cannot be read back. Check the command line.

- **illegal function:**
The first parameter of the command line must be a valid function. See chapter 2 “JTAG145 Parameter Description” for a list of supported functions.
- **illegal number:**
The specified number couldn't be interpret as a valid number. Check the relevant number base.
- **illegal option:**
See chapter 2 “JTAG145 Parameter Description” for a list of supported options.
- **illegal Pin Type:**
The name specified with the option /PIN= must be one of the list of chapter 1.6 "Initialization file JTAG145.INI"
- **illegal Flash Type:**
The name specified with the option /DEVICE= must be one of the list of chapter 1.7 "Supported flash devices".
- **Input file not found:**
The specified file cannot be found
- **Input file is empty:**
Files with zero length are not accepted
- **" " is undefined**
Please check the syntax in your configuration file. (See chapter 1.6 "Initialization file JTAG145.INI").
- **LPTx not installed**
The LPT port specified with /LPTx cannot be found. Please check the LPT port or specify a installed LPT port. Check your BIOS setup.
- **missing filename**
Most functions need a filename as second parameter.

- **missing option /I2CCLK=**
Some functions need the option /I2CCLK= to be defined.
- **missing option /I2CDAT=**
Some functions need the option /I2CDAT= or the options /I2CDATO= and /I2CDATI= to be defined.
- **missing option /LENGTH=**
Some functions need the option /LENGTH= to be defined.
- **missing option /PIN=**
Some functions need the option /PIN= to be defined.
- **More than 9 devices in the JTAG chain or TDI pin stuck at low level**
The JTAG chain is limited to 9 parts. Check target power. Check the target's TDO pin.
- **No devices found in JTAG chain or TDI pin stuck at high level**
A stream of 32 high bits was detected on the pin TDI. TDI may stuck at high level. Check the connection to your target. Check the target power. Check the target's TDO pin.
- **Option /CPUPOS= out of range**
The number specified with the option /CPUPOS= must be less or equal to the number of parts minus 1.
- **Option /IROFFS= out of range**
Please specify a smaller value
- **Part at specified position is not a IDT RC64145**
The option /CPUPOS= points to a part not a IDT RC64145 (32bit). The part may be switched to the 64bit JTAG mode.
- **Pins specified with /I2CCLK= and /I2CDAT= must have different control cells**
The pin specified with the option /I2CDAT= must be able to be switched to high impedance while the pin specified with option /I2CCLK= is an active output. See chapter 1.6 "Initialization file JTAG145.INI".

- **Pins specified with /I2CCLK= and /I2CDATI= must have different control cells**
The pin specified with the option /I2CDATI= must be able to be switched to high impedance while the pin specified with option /I2CCLK= is an active output. See chapter 1.6 “Initialization file JTAG145.INI”.
- **Pins specified with /I2CDATO= and /I2CDATI= must have different control cells**
The pin specified with the option /I2CDATI= must be able to be switched to high impedance while the pin specified with option /I2CDATO= is an active output. See chapter 1.6 “Initialization file JTAG145.INI”.
- **Specify only one of that options:**
Some options are exclusive (i.e. /8BIT and /16BIT). Don't mix them.
- **There are unknown parts in the JTAG chain. Please use the option /IROFFS= to specify the instr. reg. offset of the CPU.**
If there are unknown parts in the JTAG chain, the program isn't able to determine the logical position of the CPU's instruction register.
- **There is no IDT RC64145 in the JTAG chain**
No IDT RC64145 was found in the JTAG chain. Check the target power. Try with option /DRIVER=4 again.
- **Value of option /FILE-OFFSET out of range**
The value of the option /FILE-OFFSET= points behind end of file.
- **wrong driver #**
The value specified with the option /DRIVER= is out of range.
- **wrong Identifier (xxxx)**
No valid identifier found. Check the specified chip select signal and the bus width. Try with the option /DEVICE= .

1.6. Initialization file JTAG145.INI

This file is used to set the CPU signals for input/output. In case of output signal an additional parameter is used to set the default level to high or low. This file can be used to adapt your own IDT RC64145 design to the JTAG-BOOSTER. The Target-Entry is used to identify your design which is displayed with most commands.

When the JTAG145 software is started it scans the current directory for an existing initialization file named JTAG145.INI. If no entry is found the default values are used. You may also specify the initialization file with the option /INI= . If the specified file isn't found, the program aborts with an error message.

The CPU pins can also be used with the functions /BLINK (chapter 2.9), /PIN? (chapter 2.10) and /SAMPLE (chapter 2.11) to test the signals on your design.

Example of JTAG145.INI:

```
// Description file for IDT RC64145
Target: Generic Target
// All chip select signals are set to output and inactive.
// All signals should be defined. Undefined signals are set to their defaults.
// Pin names are defined in upper case.

// The following pins are complete bidirectional pins.
// The direction of each pin can be set independent of the other pins.
// Each pin can be used as input.
CPU_AD31      Inp      // Address/Data to/from CPU
CPU_AD30      Inp      //
CPU_AD29      Inp      //
CPU_AD28      Inp      //
CPU_AD27      Inp      //
CPU_AD26      Inp      //
CPU_AD25      Inp      //
CPU_AD24      Inp      //
CPU_AD23      Inp      //
CPU_AD22      Inp      //
CPU_AD21      Inp      //
CPU_AD20      Inp      //
CPU_AD19      Inp      //
CPU_AD18      Inp      //
```

CPU_AD17	Inp	//
CPU_AD16	Inp	//
CPU_AD15	Inp	// Address/Data to/from CPU
CPU_AD14	Inp	//
CPU_AD13	Inp	//
CPU_AD12	Inp	//
CPU_AD11	Inp	//
CPU_AD10	Inp	//
CPU_AD9	Inp	//
CPU_AD8	Inp	//
CPU_AD7	Inp	//
CPU_AD6	Inp	//
CPU_AD5	Inp	//
CPU_AD4	Inp	//
CPU_AD3	Inp	//
CPU_AD2	Inp	//
CPU_AD1	Inp	//
CPU_AD0	Inp	//
CPU_CMD8	Inp	// Command/Data Identifier to/from CPU
CPU_CMD7	Inp	//
CPU_CMD6	Inp	//
CPU_CMD5	Inp	//
CPU_CMD4	Inp	//
CPU_CMD3	Inp	//
CPU_CMD2	Inp	//
CPU_CMD1	Inp	//
CPU_CMD0	Inp	//
PCI_AD31	Inp	// PCI Address/Data
PCI_AD30	Inp	//
PCI_AD29	Inp	//
PCI_AD28	Inp	//
PCI_AD27	Inp	//
PCI_AD26	Inp	//
PCI_AD25	Inp	//
PCI_AD24	Inp	//
PCI_AD23	Inp	//
PCI_AD22	Inp	//
PCI_AD21	Inp	//
PCI_AD20	Inp	//
PCI_AD19	Inp	//
PCI_AD18	Inp	//
PCI_AD17	Inp	//
PCI_AD16	Inp	//


```

PCI_AD15      Inp    //
PCI_AD14      Inp    //
PCI_AD13      Inp    //
PCI_AD12      Inp    //
PCI_AD11      Inp    //
PCI_AD10      Inp    //
PCI_AD9       Inp    //
PCI_AD8       Inp    //
PCI_AD7       Inp    //
PCI_AD6       Inp    //
PCI_AD5       Inp    //
PCI_AD4       Inp    //
PCI_AD3       Inp    //
PCI_AD2       Inp    //
PCI_AD1       Inp    //
PCI_AD0       Inp    //
PCI_CBE3#     Inp    // PCI Command/Byte Enable
PCI_CBE2#     Inp    // PCI Command/Byte Enable
PCI_CBE1#     Inp    // PCI Command/Byte Enable
PCI_CBE0#     Inp    // PCI Command/Byte Enable
PCI_FRAME#    Inp    // PCI Cycle Frame
PCI_IRDY#     Inp    // PCI Initiator Ready
PCI_TRDY#     Inp    // PCI Target Ready
PCI_DEVSEL#   Inp    // PCI Device Select
PCI_STOP#     Inp    // PCI Stop
PCI_PERR#     Inp    // PCI Parity Error
PCI_PAR       Inp    // PCI Parity Bit
PIO12         Inp    //
PIO11         Inp    //
PIO10         Inp    //
PIO9          Inp    //
DMA_REQ3#     Inp    // DMA Request Input = PIO7
DMA_REQ2#     Inp    // DMA Request Input = PIO6
DMA_REQ1#     Inp    // DMA Request Input = PIO5
DMA_REQ0#     Inp    // DMA Request Input = PIO4
SYS_WAIT      Inp    // Wait      = PIO8
DMA_ACK3#     Out,Hi // DMA Acknowledge Output = PIO3
DMA_ACK2#     Out,Hi // DMA Acknowledge Output = PIO2
DMA_ACK1#     Out,Hi // DMA Acknowledge Output = PIO1
DMA_ACK0#     Out,Hi // DMA Acknowledge Output = PIO0
SYS_DATA31    Inp    // System Interface Data
SYS_DATA30    Inp    //
SYS_DATA29    Inp    //

```

SYS_DATA28	Inp	//
SYS_DATA27	Inp	//
SYS_DATA26	Inp	//
SYS_DATA25	Inp	//
SYS_DATA24	Inp	//
SYS_DATA23	Inp	//
SYS_DATA22	Inp	//
SYS_DATA21	Inp	//
SYS_DATA20	Inp	//
SYS_DATA19	Inp	//
SYS_DATA18	Inp	//
SYS_DATA17	Inp	//
SYS_DATA16	Inp	//
SYS_DATA15	Inp	//
SYS_DATA14	Inp	//
SYS_DATA13	Inp	//
SYS_DATA12	Inp	//
SYS_DATA11	Inp	//
SYS_DATA10	Inp	//
SYS_DATA9	Inp	//
SYS_DATA8	Inp	//
SYS_DATA7	Inp	//
SYS_DATA6	Inp	//
SYS_DATA5	Inp	//
SYS_DATA4	Inp	//
SYS_DATA3	Inp	//
SYS_DATA2	Inp	//
SYS_DATA1	Inp	//
SYS_DATA0	Inp	//

// The following pin is tristateable, but can not be read back

PCI_REQ#	Out,Hi	// PCI Bus Request
----------	--------	--------------------

// The following pins are output only pins.

// Setting to input (tristate) one of that pins results in an error.

VALIDIN#	Out,Hi	// RC64145 drives valid Data
CPU_RDY#	Out,Hi	// Ready, connects to the CPU
CPU_INT#	Out,Hi	// Interrupt Output to CPU
PCI_SERR#	Out,Hi	// PCI System Error, open drain output
PCI_INT#	Out,Hi	// PCI Interrupt Request, open drain output
UART0_SOUT	Out,Hi	// UART0 Serial Data Out
UART0_RTS#	Out,Hi	// UART0 Request to Send
UART0_DTR#	Out,Hi	// UART0 Data Terminal Ready

UART1_SOUT	Out,Hi	// UART1 Serial Data Out
SYS_ALE	Out,Lo	// Address Latch Enable, High->Latch transparent
SPI_CS#	Out,Hi	// SPI Chip Select, No connect???
SPI_MOSI	Out,Lo	// SPI Master Out Slave In, No connect????
SPI_CLK	Out,Lo	// SPI Clock, No connect????
XCVRDIR_WR#	Out,Hi	// External Transceiver Direction
XCVROE#	Out,Hi	// External Transceiver Output Enable
SYS_BOOTCS#	Out,Hi	// Boot Chip Select
SYS_DEVCS0#	Out,Hi	// Device Chip Select
SYS_DEVCS1#	Out,Hi	// Device Chip Select
SYS_DEVCS2#	Out,Hi	// Device Chip Select
SYS_DEVCS3#	Out,Hi	// Device Chip Select
SYS_DEVOE#	Out,Hi	// Device Output Enable
SD_WE#	Out,Hi	// SDRAM Write Enable
SD_CAS#	Out,Hi	// SDRAM CAS#
SD_RAS#	Out,Hi	// SDRAM RAS#
SD_BA1	Out,Lo	// SDRAM Bank Address
SD_BA0	Out,Lo	// SDRAM Bank Address
SD_CS3#	Out,Hi	// SDRAM Chip Select
SD_CS2#	Out,Hi	// SDRAM Chip Select
SD_CS1#	Out,Hi	// SDRAM Chip Select
SD_CS0#	Out,Hi	// SDRAM Chip Select
SYS_DQM_WE3#	Out,Hi	// Data Mask
SYS_DQM_WE6#	Out,Hi	// Data Mask
SYS_DQM_WE1#	Out,Hi	// Data Mask
SYS_DQM_WE4#	Out,Hi	// Data Mask
SYS_ADR11	Out,Lo	//
SYS_ADR10	Out,Lo	//
SYS_ADR9	Out,Lo	//
SYS_ADR8	Out,Lo	//
SYS_ADR7	Out,Lo	//
SYS_ADR6	Out,Lo	//
SYS_ADR5	Out,Lo	//
SYS_ADR4	Out,Lo	//
SYS_ADR3	Out,Lo	//
SYS_ADR2	Out,Lo	//
SYS_ADR1	Out,Lo	//
SYS_ADR0	Out,Lo	//

```
// The following pins are input only.  
// Setting to output of one of these pins results in an error.  
// Declaration of the direction of these pins is optional.  
VALIDOUT#      Inp      // CPU drives valid Data  
SYS_CLK        Inp      // Input Clock to RC64145  
PCI_IDSEL      Inp      // PCI Initialization Device Select  
PCI_LOCK#      Inp      // PCI Locked Cycle  
PCI_GNT#       Inp      // PCI Bus Grant  
PCI_CLK        Inp      // PCI Clock  
UART1_SIN      Inp      // UART1 Serial Data In  
UART0_CTS#     Inp      // UART0 Clear to Send  
UART0_DCD#     Inp      // UART0 Data Carrier Detect  
UART0_SIN      Inp      // UART0 Serial Data In  
SPI_MISO       Inp      // SPI Master In Slave Out, VCC CORE????
```

This example is equal to the default initialization which is used when no initialization file could be found in the current directory and no initialization file is specified with the option /INI=.

Changes to the structure of the file could result in errors. Remarks can be added by using //.

1.7. Supported flash devices

The following names could be used with the /DEVICE= option:

AM29F010	: AMD 29F010	
AM29F010*2	: Dual AMD 29F010	
* AM29LV010	: AMD 29LV010	(3.3V)
* AM29LV010*2	: Dual AMD 29LV010	(3.3V)
* AM29F100BW	: AMD 29F100B	(word mode)
* AM29F100BB	: AMD 29F100B	(byte mode)
* AM29F100TW	: AMD 29F100T	(word mode)
* AM29F100TB	: AMD 29F100T	(byte mode)
* AM29F200BW	: AMD 29F200B	(word mode)
* AM29F200BB	: AMD 29F200B	(byte mode)
* AM29F200TW	: AMD 29F200T	(word mode)
* AM29F200TB	: AMD 29F200T	(byte mode)
* AM29LV200BW	: AMD 29F200B	(3.3V, word mode)
* AM29LV200BB	: AMD 29F200B	(3.3V, byte mode)
* AM29LV200TW	: AMD 29F200T	(3.3V, word mode)
* AM29LV200TB	: AMD 29F200T	(3.3V, byte mode)
AM29F040	: AMD 29F040	
AM29F040*2	: Dual AMD 29F040	
* AM29F400BW	: AMD 29F400B	(word mode)
* AM29F400BB	: AMD 29F400B	(byte mode)
AM29F400TW	: AMD 29F400T	(word mode)
AM29F400TB	: AMD 29F400T	(byte mode)
* AM29LV400BW	: AMD 29LV400B	(3.3V, word mode)
* AM29LV400BB	: AMD 29LV400B	(3.3V, byte mode)
* AM29LV400TW	: AMD 29LV400T	(3.3V, word mode)
* AM29LV400TB	: AMD 29LV400T	(3.3V, byte mode)
* AM29LV004B	: AMD 29LV004B	(3.3V)
* AM29LV004T	: AMD 29LV004T	(3.3V)
AM29F080	: AMD 29F080	
* AM29F080*2	: Dual AMD 29F080	
* AM29LV081	: AMD 29LV081	(3.3V)
* AM29LV081*2	: Dual 29LV081	(3.3V)
* AM29F800BW	: AMD 29F800B	(word mode)
* AM29F800BB	: AMD 29F800B	(byte mode)
AM29F800TW	: AMD 29F800T	(word mode)
* AM29F800TB	: AMD 29F800T	(byte mode)
* AM29LV800BW	: AMD 29LV800B	(3.3V, word mode)
* AM29LV800BB	: AMD 29LV800B	(3.3V, byte mode)

AM29LV800TW	: AMD 29LV800T	(3.3V, word mode)
* AM29LV800TB	: AMD 29LV800T	(3.3V, byte mode)
* AM29LV008T	: AMD 29LV008T	(3.3V)
* AM29LV008B	: AMD 29LV008B	(3.3V)
AM29F016	: AMD 29F016	
AM29F016*2	: Dual AMD 29F016	
* AM29F017	: AMD 29F017	
AM29F017*2	: Dual AMD 29F017	
AM29LV017*2	: Dual AMD 29LV017	(3.3V)
* AM29F160BW	: AMD 29F160B	(word mode)
* AM29F160BB	: AMD 29F160B	(byte mode)
* AM29F160TW	: AMD 29F160T	(word mode)
* AM29F160TB	: AMD 29F160T	(byte mode)
* AM29F160BB*2	: Dual AMD 29F160B	(byte mode)
* AM29F160TB*2	: Dual AMD 29F160T	(byte mode)
AM29LV160BW	: AMD 29LV160B	(3.3V, word mode)
* AM29LV160BB	: AMD 29LV160B	(3.3V, byte mode)
* AM29LV160TW	: AMD 29LV160T	(3.3V, word mode)
* AM29LV160TB	: AMD 29LV160T	(3.3V, byte mode)
AM29LV160BB*2	: Dual AMD 29LV160B	(3.3V, byte mode)
* AM29LV160TB*2	: Dual AMD 29LV160T	(3.3V, byte mode)
AM29F032	: AMD 29F032	
AM29F032*2	: Dual AMD 29F032	
* AM29LV033	: AMD 29LV033	(3.3V)
* AM29LV033*2	: Dual AMD 29F033	(3.3V)
* AM29LV640	: AMD 29LV160	(3.3V, word mode)
* I28F001T	: Intel 28F001T	
* I28F001T*2	: Dual Intel 28F001T	
* I28F001B	: Intel 28F001B	
* I28F200BW	: Intel 28F200B	(word mode)
* I28F200BB	: Intel 28F200B	(byte mode)
* I28F200TW	: Intel 28F200T	(word mode)
* I28F200TB	: Intel 28F200T	(byte mode)
* I28F002B	: Intel 28F002B	
* I28F002T	: Intel 28F002T	
* I28F400BW	: Intel 28F400B	(word mode)
* I28F400BB	: Intel 28F400B	(byte mode)
I28F400TW	: Intel 28F400T	(word mode)
I28F400TB	: Intel 28F400T	(byte mode)
* I28F004B	: Intel 28F004B	
* I28F004T	: Intel 28F004T	
* I28F400B3B	: Intel 28F400B3B	Boot Block Smart3 Bottom

* I28F400B3T	: Intel 28F400B3T	Boot Block Smart3 Top
* I28F004S5	: Intel 28F004	FlashFile Smart3/5
* I28F800BW	: Intel 28F800B	(word mode)
* I28F800BB	: Intel 28F800B	(byte mode)
I28F800TW	: Intel 28F800T	(word mode)
* I28F800TB	: Intel 28F800T	(byte mode)
* I28F800B3B	: Intel 28F800B3B	Boot Block Smart3 Bottom
* I28F800B3T	: Intel 28F800B3T	Boot Block Smart3 Top
* I28F008B	: Intel 28F008B	
* I28F008T	: Intel 28F008T	
I28F008SA	: Intel 28F008	FlashFile 12V
I28F008SA*2	: Dual Intel 28F008	FlashFile 12V
I28F008S5	: Intel 28F008	FlashFile Smart3/5
I28F008S5*2	: Dual Intel 28F008	FlashFile Smart3/5
I28F016W	: Intel 28F016	FlashFile (word mode)
* I28F016B	: Intel 28F016	FlashFile (byte mode)
* I28F016S5	: Intel 28F016	FlashFile Smart3/5
* I28F160B3B	: Intel 28F160	Boot Block Smart3 Bottom
* I28F160B3T	: Intel 28F160	Boot Block Smart3 Top
* I28F160S5W	: Intel 28F160	FlashFile Smart5 (word mode)
* I28F160S5B	: Intel 28F160	FlashFile Smart5 (byte mode)
I28F320S5W	: Intel 28F320	FlashFile Smart3/5 (word mode)
* I28F320S5B	: Intel 28F320	FlashFile Smart3/5 (byte mode)
* I28F320J5W	: Intel 28F320	StrataFlash (word mode)
* I28F320J5B	: Intel 28F320	StrataFlash (byte mode)
* I28F320J3W	: Intel 28F320	StrataFlash (3.3V, word mode)
* I28F320J3B	: Intel 28F320	StrataFlash (3.3V, byte mode)
* I28F640J5W	: Intel 28F640	StrataFlash (word mode)
* I28F640J5B	: Intel 28F640	StrataFlash (byte mode)
* I28F640J3W	: Intel 28F640	StrataFlash (3.3V, word mode)
* I28F640J3B	: Intel 28F640	StrataFlash (3.3V, byte mode)
* I28F128J3W	: Intel 28F128	StrataFlash (3.3V, word mode)
* I28F128J3B	: Intel 28F128	StrataFlash (3.3V, byte mode)
* MBM29F200BW	: Fujitsu 29F200B	(word mode)
* MBM29F200BB	: Fujitsu 29F200B	(byte mode)
* MBM29F200TW	: Fujitsu 29F200T	(word mode)
* MBM29F200TB	: Fujitsu 29F200T	(byte mode)
* MBM29LV200BW	: Fujitsu 29LV200B	(3.3V, word mode)
* MBM29LV200BB	: Fujitsu 29LV200B	(3.3V, byte mode)
* MBM29LV200TW	: Fujitsu 29LV200T	(3.3V, word mode)
* MBM29LV200TB	: Fujitsu 29LV200T	(3.3V, byte mode)
* MBM29F002B	: Fujitsu 29F002B	

* MBM29F002SB	: Fujitsu 29F002SB	(TSOP40)
* MBM29LV002B	: Fujitsu 29LV002B	(3.3V)
* MBM29F002T	: Fujitsu 29F002T	
* MBM29F002ST	: Fujitsu 29F002ST	(TSOP40)
* MBM29LV002T	: Fujitsu 29LV002T	(3.3V)
* MBM29F040	: Fujitsu 29F040	
* MBM29F400BW	: Fujitsu 29F400B	(word mode)
* MBM29F400BB	: Fujitsu 29F400B	(byte mode)
* MBM29F400TW	: Fujitsu 29F400T	(word mode)
* MBM29F400TB	: Fujitsu 29F400T	(byte mode)
* MBM29LV400BW	: Fujitsu 29LV400B	(3.3V, word mode)
* MBM29LV400BB	: Fujitsu 29LV400B	(3.3V, byte mode)
* MBM29LV400TW	: Fujitsu 29LV400T	(3.3V, word mode)
* MBM29LV400TB	: Fujitsu 29LV400T	(3.3V, byte mode)
* MBM29LV004B	: Fujitsu 29LV004B	(3.3V)
* MBM29LV004T	: Fujitsu 29LV004T	(3.3V)
* MBM29F080	: Fujitsu 29F080	
* MBM29LV080	: Fujitsu 29LV080	(3.3V)
* MBM29F800BW	: Fujitsu 29F800B	(word mode)
* MBM29F800BB	: Fujitsu 29F800B	(byte mode)
* MBM29F800TW	: Fujitsu 29F800T	(word mode)
* MBM29F800TB	: Fujitsu 29F800T	(byte mode)
* MBM29LV800BW	: Fujitsu 29LV800B	(3.3V, word mode)
* MBM29LV800BB	: Fujitsu 29LV800B	(3.3V, byte mode)
* MBM29LV800TW	: Fujitsu 29LV800T	(3.3V, word mode)
* MBM29LV800TB	: Fujitsu 29LV800T	(3.3V, byte mode)
* MBM29LV008B	: Fujitsu 29LV008B	(3.3V)
* MBM29LV008T	: Fujitsu 29LV008T	(3.3V)
* MBM29F016	: Fujitsu 29F016	
* MBM29F016*2	: Dual Fujitsu 29F016	
* MBM29F017	: Fujitsu 29F017	
* MBM29F017*2	: Dual Fujitsu 29F017	
* MBM29F160BW	: Fujitsu 29LV160B	(word mode)
* MBM29F160BB	: Fujitsu 29LV160B	(byte mode)
* MBM29F160TW	: Fujitsu 29LV160T	(word mode)
* MBM29F160TB	: Fujitsu 29LV160T	(byte mode)
* MBM29F160BB*2	: Dual Fujitsu 29LV160B	(byte mode)
* MBM29F160TB*2	: Dual Fujitsu 29LV160T	(byte mode)
* MBM29LV160BW	: Fujitsu 29LV160B	(3.3V, word mode)
* MBM29LV160BB	: Fujitsu 29LV160B	(3.3V, byte mode)
* MBM29LV160TW	: Fujitsu 29LV160T	(3.3V, word mode)
* MBM29LV160TB	: Fujitsu 29LV160T	(3.3V, byte mode)
MBM29LV160BB*2	: Dual Fujitsu 29LV160B	(3.3V, byte mode)

* MBM29LV160TB*2	: Dual Fujitsu 29LV160T	(3.3V, byte mode)
MBM29F032	: Fujitsu 29F032	
MBM29F032*2	: Dual Fujitsu 29F032*2	
* M29F100BW	: ST 29F100B	(word mode)
* M29F100BB	: ST 29F100B	(byte mode)
* M29F100TW	: ST 29F100T	(word mode)
* M29F100TB	: ST 29F100T	(byte mode)
M29F200BW	: ST 29F200B	(word mode)
* M29F200BB	: ST 29F200B	(byte mode)
* M29F200TW	: ST 29F200T	(word mode)
* M29F200TB	: ST 29F200T	(byte mode)
* M29F040	: ST 29F040	
* M29F040*2	: Dual ST 29F040	
* M29W040	: ST 29W040	(3.3V)
* M29W040*2	: Dual ST 29W040	(3.3V)
* M29F400BW	: ST 29F400B	(word mode)
* M29F400BB	: ST 29F400B	(byte mode)
* M29F400TW	: ST 29F400T	(word mode)
* M29F400TB	: ST 29F400T	(byte mode)
* M29W400BW	: ST 29W400B	(3.3V, word mode)
* M29W400BB	: ST 29W400B	(3.3V, byte mode)
* M29W400TW	: ST 29W400T	(3.3V, word mode)
* M29W400TB	: ST 29W400T	(3.3V, byte mode)
* M29W004B	: ST 29W004B	(3.3V)
* M29W004T	: ST 29W004T	(3.3V)
* M29F800BW	: ST 29F800B	(word mode)
* M29F800BB	: ST 29F800B	(byte mode)
* M29F800TW	: ST 29F800T	(word mode)
* M29F800TB	: ST 29F800T	(byte mode)

The flash devices signed with '*' are not yet tested.

2. JTAG145 Parameter Description

When you start JTAG145.EXE without any parameters the following help screen with all possible functions and options is displayed:

```
JTAG145 --- JTAG utility for the IDT RC64145 (32bit)
Copyright © FS FORTH-SYSTEME GmbH, Breisach
Version 3.00 of mm/dd/yyyy
```

Programming of Flash-EPROMs and Debugging on targets with the IDT RC64145.

The JTAG-Booster is needed to connect the parallel port of the PC to the JTAG port of the IDT RC64145.

Usage: JTAG145 /function [filename] [/option_1] ... [/option_n]

Supported functions:

```
/P      : Program a Flash Device
/R      : Read a Flash Device to file
/V      : Verify a Flash Device with file
/DUMP   : Make a target dump
/PI2C   : Program an I2C Device with file
/RI2C   : Read an I2C Device to file
/VI2C   : Verify an I2C Device with file
/DUMPI2C : Make a dump of an I2C Device
/BLINK  : Toggle a CPU pin
/PIN?   : Test a CPU pin
/SAMPLE : Test a CPU pin while CPU is running
/LIST   : Print a list of supported Flash devices
```

Supported Options:

```
/BOOTCS  /DEVCS0  /DEVCS1  /DEVCS2  /DEVCS3
/NOCS    /WRSETUP  /VERIFY  /TOP      /PAUSE
/P       /NODUMP   /NOERASE /LATTICE  /ERASEALL
/LPT1    /LPT2     /LPT3    /LPT-BASE /16BIT
/8BIT    /NOMAN    /32H     /32L     /LENGTH=
/L=      /FILE-OFFSET= /FO=     /OFFSET=
/O=      /DELAY=   /DEVICE-BASE= /DB=
/DRIVER= /DATA-MASK= /DM=     /IROFFS= /CPUPOS=
/DEVICE= /PIN=     /I2CCLK= /I2CDAT= /I2CDATI=
/I2CDATO= /WATCH=  /OUT=    /INI=
```