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# S32R274

# S32R274 Data Sheet

## Features

- On-chip modules available within the device include the following features:
- Safety core: Power Architecture® e200Z4 32-bit CPU with checker core
- Dual issue computation cores: Power Architecture® e200Z7 32-bit CPU
- 2 MB on-chip code flash (FMC flash) with ECC
- 1.5 MB on-chip SRAM with ECC
- RADAR processing
  - Signal Processing Toolbox (SPT) for RADAR signal processing acceleration
  - Cross Timing Engine (CTE) for precise timing generation and triggering
  - Waveform generation module (WGM) for chirp ramp generation
  - 4x 12-bit ΣΔ-ADC with 10 MSps
  - One DAC with 10 MSps
  - MIPICSI2 interface to connect external ADCs
- Memory Protection
  - Each core memory protection unit provides 24 entries
  - Data and instruction bus system memory protection unit (SMPU) with 16 region descriptors each
  - Register protection
- Clock Generation
  - 40 MHz external crystal (XOSC)
  - 16 MHz Internal oscillator (IRCOSC)
  - Dual system PLL with one frequency modulated phase-locked loop (FMPLL)
  - Low-jitter PLL to ΣΔ-ADC and DAC clock generation (not supported on SC66760x devices)
- Functional Safety
  - Enables up to ASIL-D applications
  - FCCU for fault collection and fault handling
  - MEMU for memory error management
  - Safe eDMA controller
  - Self-Test Control Unit (STCU2)
  - Error Injection Module (EIM)
  - On-chip voltage monitoring
  - Clock Monitor Unit (CMU)
- Security
  - Cryptographic Security Engine (CSE2)
  - Supports censorship and life-cycle management
- Timers
  - Two Periodic Interval Timers (PIT) with 32-bit counter resolution
  - Three System Timer Module (STM)
  - Three Software Watchdog Timers (SWT)
  - Two eTimer modules with 6 channels each
  - One FlexPWM module for 12 PWM signals
- Communication Interfaces
  - Two Serial Peripheral interface (SPI) modules
  - One LINFlexD module
  - Two inter-IC communication interface (I2C) modules
  - One dual-channel FlexRay module with 128 message buffers
  - Three FlexCAN modules with configurable buffers - CAN FD optionally supported on 2 FlexCAN modules
  - One ENET MAC supporting MII/RMII/RGMII interface
  - ZipWire high-speed serial communication
- Debug Functionality
  - 4-pin JTAG interface and Nexus/Aurora interface for serial high-speed tracing
  - e200Z7 core and e200Z4 core: Nexus development interface (NDI) per IEEE-ISTO 5001-2012 Class 3+
- Two analog-to-digital converters (SAR ADC)
  - Each ADC supports up to 16 input channels
  - Cross Trigger Unit (CTU)
- On-chip voltage DC/DC regulator for core clock (VREG)
- Two Temperature Sensors (TSENS)

# Table of Contents

# 1 Introduction

## 1.1 Family comparison

The following table provides a comparison of the devices: S32R274, , and MPC5775K . This information is intended to provide an understanding of the range of functionality offered by this family. For full details of all of the family derivatives please contact your marketing representative.

**Table 1. S32R274 Family Comparison**

| Feature | S32R274 | MPC5775K |
|---|---|---|
| CPUs | e200z420 lock-step<br>2x e200z7260 | |
| SIMD | SPE2 + EFP2 (z7) | |
| Maximum Operating Frequency | 240 MHz (z7 cores) / 180 MHz (z4) | 266 MHz (z7 cores) / 133 MHz (z4) |
| Flash | 2 MB with ECC | 4 MB with ECC |
| EEPROM support | 64 KB (emulation) | 96 KB (emulation) |
| RAM | 1.5 MB with ECC | |
| ECC | end-to-end | |
| MPU | Core MPU: 24 entries per core, System MPU: 2x16 entries | |
| eDMA | safe eDMA with 32 channels, 64 triggers | |
| Control ADC | 2x 12-bit SAR ADC, 1 MSps input mux for 16 external channels | 4x 12-bit SAR ADC, 1 MSps, input mux for 37 external channels |
| SD-ADC | 4 channels, 10 MSps | 8 channels, 10 MSps |
| SPT | 1x | |
| CTE | 1x | |
| WGM | 1x | |
| CTU | 1x | 2x |
| SWT | 3x | |
| STM | 3x | |
| PIT | 2x | |
| CRC | 2x | |
| SEMA42 | 1x | |
| LINFlexD | 1x | 4x |
| CAN | 3x FlexCAN including 2x FlexCAN-FD | 4x FlexCAN + 1x MCAN-FD |
| SPI | 2x | 4x |
| $I^2C$ | 2x | 3x |
| Zipwire | 1x LFAST+SIPI, 320 MHz | |
| FlexRay | 1x dual channel | |

*Table continues on the next page...*

**Table 1. S32R274 Family Comparison (continued)**

| Feature | S32R274 | MPC5775K |
|---|---|---|
| Ethernet | 10/100 and >100 Mbps, RMII/MII/RGMII I/F, AVB support | 10/100 Mbps, RMII/MII I/F, AVB support |
| FlexPWM | 1x, 12 PWM channels | 2x, 12 PWM channels each |
| eTimer | 2x, 6 channels each | 3x, 6 channels each |
| External ADC interface | 1x 4 lanes MIPICSI2 Rx, 1 Gbps/lane | 1x PDI (16-bit data, clock, sync) |
| IRCOSC | 16 MHz | |
| XOSC | 40 MHz | |
| FMPLL | dual system PLL, 1x FM modulated | |
| DAC | 1x 12-bit 10 MSps | 1x 12-bit 2 MSps |
| SIUL2 | 1x | |
| BAM | 1x | |
| INTC | 1x | |
| SSCM | 1x | |
| FCCU/FOSU | 1x | |
| MEMU | 1x | |
| STCU2 | 1x | |
| CSE | 1x | - |
| PASS/TDM | 1x | - |
| MC_ME | 1x | |
| MC_CGM | 1x | |
| MC_RGM | 1x | |
| TSENS | 2x | |
| Debug | JTAGC, JTAGM, CJTAG, with class3+ Nexus, Aurora only | |
| Safety level | ISO26262 SEooC ASIL-B to ASIL-D | |
| Temp. range (Tj) | -40 to 150˚C | |

## 1.2 Feature list

On-chip modules available within the device include the following features:

- Safety core: Power Architecture® e200Z4 32-bit CPU with checker core
  - 2 cycle delayed lockstep
  - Harvard architecture with 64-bit bus for data and instructions
  - Dual issue: up to two instructions per clock cycle
  - 8 KB instruction cache and 4 KB data cache
  - 64 KB data local memory
    - with background load/store: backdoor access
    - 0-wait state for all read and 32/64-bit write accesses
    - Low number of wait states for backdoor accesses

    - Support for decorated storage
    - Variable Length Encoding (VLE) compliant for higher code density
    - Single precision floating point operations
- Computation cores: Power Architecture® e200Z7 32-bit CPU
    - Dual issue: up to two instructions per clock cycle
    - Harvard architecture with 64-bit bus for data instructions
    - 16 KB instruction cache and 16 KB data cache
    - 64 KB data local memory
        - with background load/store: backdoor access
        - 0-wait state for all read and 32/64-bit write accesses
        - Low number of wait states for backdoor accesses
    - Support for decorated storage
    - Using variable length encoding (VLE) for higher code density
    - 4-way integer processing unit (SPE2)
    - 2-way single-precision Floating Point Unit (EFPU2)
- 2 MB on-chip code flash (FMC flash) with ECC
    - Three ports (one per CPU) shared between code and data flash with 4 × 256 bit buffer for code and data flash including prefetch functions
    - Data flash is part of the code flash module
    - Including 64 KB EEPROM emulation
- 1.5 MB on-chip SRAM with ECC
    - Decorated memory controller to support atomic read-modify-write operations
    - Single- and double-bit error visibility is supported
    - Up to four ports (one per CPU and SPT) and up to 8 banks allow simultaneous accesses from different masters to different banks
- RADAR processing
    - Signal Processing Toolbox (SPT) for RADAR signal processing acceleration
    - Cross Timing Engine (CTE) for precise timing generation and triggering
    - Waveform generation module (WGM) for chirp ramp generation
    - 4x 12-bit ΣΔ-ADC with 10 MSps
    - One DAC with 10 MSps
    - MIPICSI2 interface to connect external ADCs
        - Four data lanes, with up to 1 Gbps per lane and in total
        - One clock lane
- Memory Protection
    - Each core memory protection unit provides 24 entries
    - Data and instruction bus system memory protection Unit (SMPU) with 16 region descriptors each
    - Register protection
- Clock Generation
    - 40 MHz external crystal (XOSC)

  - 16 MHz Internal oscillator (IRCOSC)
  - Dual system PLL with one frequency modulated phase-locked loop (FMPLL)
  - Low-jitter PLL to ΣΔ-ADC and DAC clock generation
- Functional Safety
  - Enables up to ASIL-D applications
  - End to end ECC ensuring full protection of all data accesses throughout the system, from each of the systems masters through the crossbar and into the memories and peripherals
  - FCCU for fault collection and fault handling
  - MEMU for memory error management
  - Safe eDMA controller
  - User selectable Memory BIST (MBIST) can be enabled to run out of various reset conditions or during runtime
  - Self-Test Control Unit (STCU2)
  - Error Injection Module (EIM)
  - On-chip voltage monitoring
  - Clock Monitor Unit (CMU) to support monitoring of critical clocks
- Security
  - Cryptographic Security Engine (CSE2) enabling advanced security management
  - Supports censorship and life-cycle management via Password and Device Security (PASS) module
  - Diary control for tamper detection (TDM)
- Support Modules
  - Global Interrupt controller (INTC) capable of routing interrupts to any CPU
  - Semaphore unit to manage access to shared resources
  - Two CRC computation units with four polynomials
  - 32-channel eDMA controller with multiple transfer request sources using DMAMUX
  - Boot Assist Module (BAM) supports internal flash programming via a serial link (LIN / CAN)
- Timers
  - Two Periodic Interval Timers (PIT) with 32-bit counter resolution
  - Three System Timer Module (STM)
  - Three Software Watchdog Timers (SWT)
  - Two eTimer modules with 6 channels each
  - One FlexPWM module for 12 PWM signals
- Communication Interfaces
  - Two Serial Peripheral interface (SPI) module
  - Two inter-IC communication interface (I2C) modules
  - One LINFlexD module
  - One dual-channel FlexRay module with 128 message buffers

    - Three FlexCAN modules with configurable buffers
        - CAN FD optionally supported on 2 FlexCAN modules
    - One ENET MAC supporting MII/RMII/RGMII interface
        - Supports 10/100 Mbps (MII/RMII/RGMII) and >100 Mbps (RGMII)
        - Supports IEEE1588 timestamps and PTP
    - Zipwire high-speed serial communication
        - Supports LFAST and SIPI protocol
        - Fast interprocessor communication with 320 Mbps gross data rate
        - DMA based access to memory resources
- Debug Functionality
    - 4-pin JTAG interface and Nexus/Aurora interface for serial high-speed tracing
    - e200Z7 core and e200Z4 core: Nexus development interface (NDI) per IEEE-ISTO 5001-2012 Class 3+
    - All platform bus masters except CSE can be monitored via Nexus/Aurora
    - Device/board boundary Scan testing supported with per Joint Test Action Group (JTAG) (IEEE 1149.1) and 1149.7 (cJTAG)
    - On-chip control for Nexus development interface by JTAGM module
- Two analog-to-digital converters (SAR ADC)
    - Each ADC supports up to 16 input channels
    - Cross Trigger Unit to enable synchronization of ADC conversions with eTimer
- On-chip voltage DC/DC regulator for core clock (VREG)
- Two Temperature Sensors (TSENS)

## 1.3 Block diagram

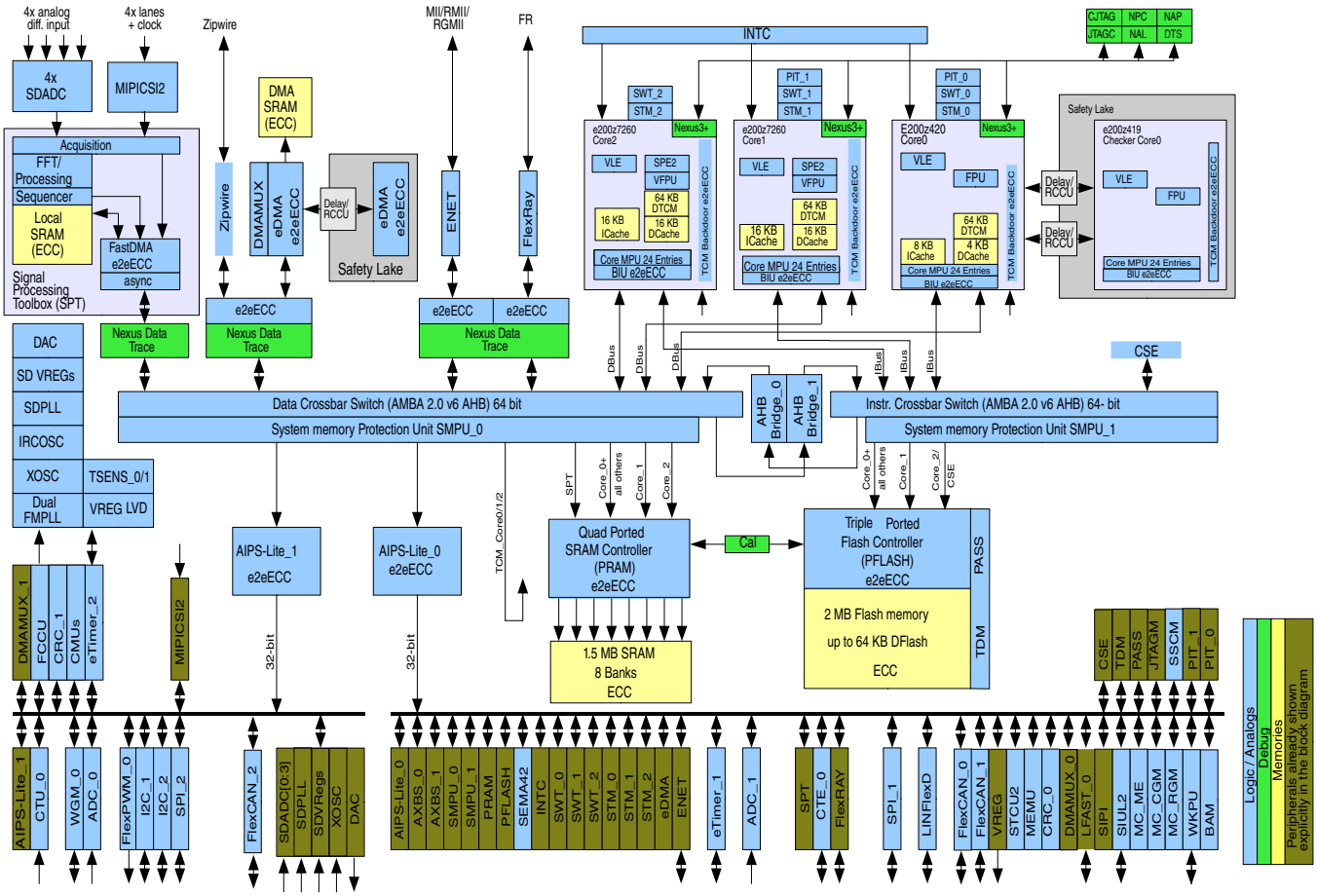


**Figure 1. S32R274 block diagram**

# 2 Ordering parts

## 2.1 Determining valid orderable parts

Valid orderable part numbers are provided on the web. To determine the orderable part numbers for this device, go to www.nxp.com and perform a part number search for the device number.

# 3 Part identification

## 3.1 Description

Part numbers for the chip have fields that identify the specific part. You can use the values of these fields to determine the specific part you have received.

## 3.2 Fields

This section lists the possible values for each field in the part number (not all combinations are valid):

**Table 2. Configuration**

| 257MAPBGA | Configuration | Performance | Temperature |
|---|---|---|---|
| FS32R274KSK2MMM | S | K | M |
| FS32R274KCK2MMM | C | K | M |
| FS32R274VBK2MMM | B | V | M |
| FS32R274VCK2MMM | C | V | M |
| FS32R274KSK2VMM | S | K | V |
| FS32R274KCK2VMM | C | K | V |
| FS32R274VBK2VMM | B | V | V |
| FS32R274VCK2VMM | C | V | V |

**Table 3. Configuration**

| Configuration | 2 MB Flash | 1.5 MB RAM | CSE |
|---|---|---|---|
| B or S | Yes | Yes | Yes |
| C | Yes | Yes | No |

**Table 4. Performance**

| Perf (MHz) | Z7 | Z7 | Z4 | Z4 |
|---|---|---|---|---|
| K | 240 | 240 | 120 | 120 |
| V | 200 | 200 | 100 | 100 |

**Table 5. Temperature values**

| Temperature | $T_A$ |
|---|---|
| M | -40 °C to 125 °C |
| V | -40 °C to 105 °C |

# 4 General

## 4.1 Absolute maximum ratings

**NOTE**

Functional operating conditions appear in the DC electrical characteristics. Absolute maximum ratings are stress ratings only, and functional operation at the maximum values is not guaranteed.

Stress beyond the listed maximum values may affect device reliability or cause permanent damage to the device.

**Table 6. Absolute maximum ratings**

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DD\_HV\_PMU}$ | 3.3 V PMU supply voltage | — | –0.3 | 4.0[1, 2] | V |
| $V_{DD\_HV\_REG3V8}$ | REG3V8 Supply Voltage | — | –0.3 | 5.5 | V |
| $V_{DD\_HV\_IO*}$ | 3.3 V Input/Output Supply Voltage, LFAST IO Supply, RGMII IO Supply and PWM IO Supply | — | –0.3 | 3.63[1, 2] | V |
| $V_{SS\_HV\_IOx}$ | Input/output ground voltage | — | –0.1 | 0.1 | V |
| $V_{DD\_HV\_FLA}$ | 3.3 V flash supply voltage | — | –0.3 | 3.63[1, 2] | V |
| $V_{DD\_HV\_RAW}$ | AFE RAW supply voltage | — | –0.1 | 4 | V |
| $V_{DD\_HV\_DAC}$ | AFE DAC supply voltage | — | –0.1 | 4 | V |
| $V_{DD\_LV\_IO*}$ | Aurora supply voltage | — | –0.3 | 1.5 | V |
| $V_{DD}$ | 1.25 V core supply voltage[3, 4, 5] | — | –0.3 | 1.5 | V |
| $V_{SS}$ | 1.25 V core supply ground[3, 4, 5] | — | –0.3 | 0.3 | V |
| $V_{SS\_LV\_OSC}$ | Oscillator amplifier ground | — | –0.1 | 0.1 | V |
| $V_{DD\_LV\_PLL0}$ | System PLL supply voltage | — | –0.3 | 1.5 | V |
| $V_{DD\_LV\_LFASTPLL}$ | LFAST PLL supply voltage | — | –0.3 | 1.5 | V |
| $V_{DD\_HV\_ADCREF0/1}$ | ADC_0 and ADC_1 high reference voltage | — | –0.3 | 5.5 | V |
| $V_{SS\_HV\_ADCREF0/1}$ | ADC_0 and ADC_1 ground and low reference voltage | — | –0.1 | 0.1 | V |
| $V_{DD\_HV\_ADC}$ | 3.3 V ADC supply voltage | — | –0.3 | 4.0 [1, 2] | V |

*Table continues on the next page...*

## Table 6. Absolute maximum ratings (continued)

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{SS\_HV\_ADC}$ | 3.3 V ADC supply ground | — | –0.1 | 0.1 | V |
| $TV_{DD}$ | Supply ramp rate[6] | — | 0.00005 | 0.1 | V/µs |
| $V_{IN\_XOSC}$ | Voltage on XOSC pins with respect to ground | — | -0.3 | 1.47 | V |
| $V_{INA}$ | Voltage on SAR ADC analog pin with respect to ground ($V_{SS\_HV\_ADCREFx}$) | — | –0.3 | 6.0 | V |
| $V_{INA\_SD}$ | Voltage on Sigma-Delta ADC analog pin with respect to ground[7] | Powered up [8] | -0.3 | $V_{DD\_HV\_RAW}$ + 0.3 | V |
| | | Powered down [9] | -0.3 | 1.47 | |
| $V_{IN}$ | Voltage on any digital pin with respect to ground ($V_{SS\_HV\_IOx}$) | Relative to $V_{DD\_HV\_IOx}$ | –0.3 | $V_{DD\_HV\_IOx}$ + 0.3 [10] | V |
| $V_{DD\_LV\_DPHY}$ | MIPICSI2 DPHY voltage supply[3, 4, 5] | — | –0.3 | 1.5 | V |
| $V_{SS\_LV\_DPHY}$ | MIPICSI2 DPHY supply ground[3, 4, 5] | — | –0.3 | 0.3 | V |
| $I_{INJPAD}$[11] | Injected input current on any pin during overload condition[12] | — | –10 | 10[13] | mA |
| $I_{INJSUM}$ | Absolute sum of all injected input currents during overload condition | — | –50 | 50 | mA |
| $T_{STG}$ | Storage temperature | — | –55 | 150 | °C |

1. 5.3 V for 10 hours cumulative over lifetime of device; 3.3 V +10% for time remaining.
2. Voltage overshoots during a high-to-low or low-to-high transition must not exceed 10 seconds per instance.
3. 1.45 V to 1.5 V allowed for 60 seconds cumulative time at maximum $T_J$ = 150°C; remaining time as defined in note 5 and note 6.
4. 1.375 V to 1.45 V allowed for 10 hours cumulative time at maximum $T_J$ = 150°C; remaining time as defined in note 6.
5. 1.32 V to 1.375 V range allowed periodically for supply with sinusoidal shape and average supply value below 1.275 V at maximum $T_J$=150°C.
6. $TV_{DD}$ is relevant for all external supplies.
7. ADC inputs include an overvoltage detect function that detects any voltage higher than 1.2 V with respect to ground on either ADC input and open circuit (disconnect) the input in order to prevent damage to the ADC internal circuitry. The ADC input remains disconnected until the inputs return to the normal operating range.
8. SDADC is powered up and overvoltage protection is ON.
9. SDADC is powered up and overvoltage protection is OFF.
10. Only when $V_{DD\_HV\_IOx}$ < 3.63 V.
11. The maximum value limits of injection current and input voltage both must be followed together for proper device operation.
12. No input current injection circuitry on AFE pins.
13. The maximum value of 10 mA applies to pulse injection only. DC current injection is limited to a maximum of 5 mA.

## 4.2 Operating conditions

The following table describes the operating conditions for the device, and for which all specifications in the datasheet are valid, except where explicitly noted. The device operating conditions must not be exceeded, or the functionality of the device is not guaranteed.

**Table 7. Device operating conditions**

| Symbol | Parameter | Conditions | Min | Typ | Max[1] | Unit |
|---|---|---|---|---|---|---|
| $V_{DD\_HV\_PMU}$ | 3.3V PMU Supply Voltage | — | 3.13[2] | 3.3 | 3.6 | V |
| $V_{DD\_HV\_REG3V8}$ | REG3V8 Supply Voltage | — | 3.13 | 3.8 | 5.5 | V |
| $V_{DD}$ | Core Supply Voltage | — | 1.19[2] | 1.25 | 1.31[3] | V |
| $V_{DD\_HV\_IO*}$ | Main GPIO 3V Supply Voltage, LFAST IO Supply, RGMII IO Supply, PWM IO Supply Voltage | — | 3.13[2] | 3.3 | 3.6 | V |
| $V_{DD\_LV\_IO\_*}$[4] | Aurora Supply Voltage | — | 1.19 | 1.25 | 1.31 | V |
| $V_{DD\_LV\_PLL0}$ | System PLL Supply Voltage | — | 1.19[2] | — | 1.31 | V |
| $V_{DD\_LV\_LFASTPLL}$ | LFAST PLL Supply Voltage | — | 1.19 | — | 1.31 | V |
| $V_{DD\_HV\_FLA}$[5] | Flash Supply Voltage | — | 3.13[2] | 3.3 | 3.6 | V |
| $V_{DD\_HV\_ADC}$ | SAR ADC Supply Voltage (HVD supervised) | — | 3.13[2] | 3.3 | 3.6[6] | V |
| $V_{DD\_HV\_RAW}$ | 3.3V AFE RAW Supply Voltage | — | 3.13 | 3.3 | 3.6 | V |
| $V_{DD\_HV\_DAC}$ | 3.3V AFE DAC Supply Voltage | — | 3.13 | 3.3 | 3.6 | V |
| $V_{DD\_HV\_ADCREF0/1}$ | ADC_0 and ADC_1 high reference voltage | — | 3.13 | 3.3 | 3.6 | V |
| $V_{IN}$ | Voltage on digital pin with respect to ground ($V_{SS\_HV\_IOx}$) | — | — | — | $V_{DD\_HV\_IOx}$ +0.3 | V |
| $V_{INSDPP}$ | Sigma-Delta ADC Input Voltage (peak-peak)[7, 8] | Differential | — | — | 1.2 | V |
| $V_{INSR}$ | Sigma-Delta ADC Input Slew Rate[7] | — | — | — | 165 | V/µs |
| $R_{TRIM\_TOL}$ | External Trim Resistor tolerance | ±0.1% | 40.16 | 40.2 | 40.25 | kΩ |
| $R_{TRIM\_TEMPCO}$ | External Trim Resistor Temperature Coefficient | — | — | — | 25 | ppm/°C |
| $V_{INA}$[9] | Voltage on SAR ADC analog pin with respect to ground ($V_{SS\_HV\_ADCREFx}$) | — | — | — | $V_{DD\_HV\_ADCREFx}$ | V |
| $V_{DD\_LV\_DPHY}$ | MIPICSI2 DPHY voltage supply[10] | | 1.19 | 1.25 | 1.31 | V |
| $T_A$,[11] | Ambient temperature at full performance [12] | — | –40 | — | 125 | °C |

*Table continues on the next page...*

## Table 7. Device operating conditions (continued)

| Symbol | Parameter | Conditions | Min | Typ | Max[1] | Unit |
|---|---|---|---|---|---|---|
| $T_J$[11] | Junction temperature | — | –40 | — | 150 | °C |
| $F_{XTAL}$ | XOSC Crystal Frequency[13] | — | — | 40 | — | MHz |
| **AFE Bypass Modes Only** | | | | | | |
| **Single-Ended External Clock**[14] | | | | | | |
| $EXTAL_{clk}$ | EXTAL external clock frequency | | | 40 | | MHz |
| $V_{inxoscjit}$ | EXTAL external clock Cycle to Cycle Jitter (RMS) | — | — | — | 2.5[15] | ps |
| $V_{inxoscclkvil}$ | EXTAL external clock input low voltage | — | 0 | — | 0.4 | V |
| $V_{inxoscclkvih}$ | EXTAL external clock input high voltage | — | 1 | — | 1.23 | V |
| $t_r/t_f$ | Rise/fall time of EXTAL external clock input | | | | 1 | ns |
| $t_{dc}$ | Duty Cycle of EXTAL external clock input | | 47 | 50 | 53 | % |
| **Differential LVDS External Clock** | | | | | | |
| $LVDS_{clk}$ | LVDS external clock frequency | | | 40 | | MHz |
| $LVDSV_{inxoscclk}$ | LVDS external clock input voltage | | 0 | | 1.36 | V |
| $LVDSV_{inxoscclk(p-p)}$ | LVDS external clock input voltage (peak-peak) | Voltage driven, AC coupled Differential | 0.45 | 0.70 | 1.12 | V |
| $LVDSI_{inxoscclk}$ | LVDS external clock input current | Current driven, DC coupled. | 3.0 | 3.5 | 4.0 | mA |
| $LVDSV_{inxoscjit}$ | LVDS external clock Jitter (RMS) [15] | | | | 2.5 | ps |
| $t_r/t_f$ | Rise/fall time of LVDS external clock input | 20% - 80% | | | 1.5 | ns |
| $t_{dcLVDS}$ | Duty Cycle of LVDS external clock input | | 47 | 50 | 53 | % |

1. Full functionality cannot be guaranteed when voltages are out of the recommended operating conditions.
2. Min voltage takes into account the LVD variation.
3. Max voltage takes into account HVD variation.
4. Aurora supply must connect to core supply voltage at board level.
5. The ground connection for the $V_{DD\_HV\_FLA}$ is shared with $V_{SS}$.
6. Supply range does not take into account HVD levels. Full range can be achieved after power-up, if HVD is disabled. See Voltage regulator electrical characteristics section for details.
7. Around common mode voltage of 0.7 V. Input voltage cannot exceed 1.4 V prior to AFE start-up completion (VREF and VREGs on and LVDs cleared).
8. SDADC input voltage full scale is 1.2 Vpp
9. On channels shared between ADC0 and 1, $V_{DD\_HV\_ADCREFx}$ is the lower of $V_{DD\_HV\_ADCREF0/1}$.
10. $V_{DD\_LV\_DPHY}$ supply should be shorted to core supply voltage VDD on board. Refer to AN5251. Contact your NXP sales representative for details.

11. While determining if the operating temperature specifications are met, either the ambient temperature or junction temperature specification can be used. It is critical that the junction temperature specification is not exceeded under any condition.
12. Full performance means Core0 running @ 120 MHz, Core1/2 running @ 240 MHz, SPT running @ 200 MHz, rich set of peripherals used.
13. Recommended Crystal 40 MHz (ESR≤30 Ω), 8 pF load capacitance.
14. External mode can be used as differential input with EXTAL and XTAL
15. The number is 3.5 ps when SD-ADC and/or DAC is not used in the device.

## 4.3 Supply current characteristics

Current consumption data is given in the following table. These specifications are design targets and are subject to change per device characterization.

**Table 8. Current consumption characteristics**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $I_{DD\_CORE}$ | Core current in run mode | All cores at max frequency. 1.31 V. Tj = 150°C | - | - | 1480[1] | mA |
| $I_{DD\_HV\_FLA}$ | Flash operating current | Tj = 150°C. $V_{DD\_HV\_FLA}$ = 3.6 V | - | 3[2] | 40[3] | mA |
| $I_{DD\_LV\_AURORA}$ | Aurora operating current | Tj = 150°C. $V_{DD\_LV\_AURORA}$ = 1.31 V. 4 TX lanes enabled. | - | - | 60 | mA |
| $I_{DD\_HV\_ADC}$ | ADC operating current | Tj = 150°C. $V_{DD\_HV\_ADC}$ = 3.6 V. 2 ADCs operating at 80 MHz. | - | 2 | 5 | mA |
| $I_{DD\_HV\_ADCREF}$ | Reference current per ADC[4]<br>Reference current per temp sensor[5] | Tj = 150°C. $V_{DD\_HV\_ADCREFx}$ = 3.6 V. ADC operating at 80 MHz. | -<br>- | -<br>- | 1.5<br>0.75 | mA |
| $I_{DD\_HV\_RAW}$ | AFE SD and regulator operating current | Tj = 150°C. $V_{DD\_HV\_RAW}$ = 3.6 V. SD-PLL, AFE regulators and 4 SD enabled. | - | 70[6] | 75 | mA |
| $I_{DD\_HV\_DAC}$ | AFE DAC operating current | Tj = 150°C. $V_{DD\_HV\_DAC}$ = 3.6 V. DAC enabled. | - | 10 | 15 | mA |
| $I_{DD\_HV\_PMU}$ | PMU operating current | Tj = 150°C. VDD_HV_PMU = 3.6 V. Internal regulation enabled. | - | 2 | 10 | mA |
| $I_{DD\_LV\_DPHY}$ | MIPICSI2 DPHY operating current in HS-RX mode | Tj = 150°C, $V_{DD\_LV\_DPHY}$ =1.31 V | - | 14.9 | 23.2 | mA |

1. Strong dependence on use case, cache usage.
2. Measured during flash read.
3. Peak Flash current measured during read while write (RWW) operation.
4. ADC0 and 1 on ADCREF0/1.
5. Temp sensor current when PMC_CTL_TD[TSx_AOUT_EN] = 1. TS0 on ADCREF0/1.
6. Typical number is approximately 10 mA per each SD-ADC enabled, 12 mA for SD-PLL and 15 mA for the AFE regulators.

## 4.4 Voltage regulator electrical characteristics

**Table 9. Voltage regulator electrical specifications**

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| POR-R | 1.25 V VDD core POR release | — | 0.97 | 1.02 | 1.06 | V |
| POR-E | 1.25 V VDD core POR engage | — | 0.93 | 0.98 | 1.02 | V |
| LVD12R | Low-Voltage Detection 1.25 V release (Core VDD supply, and PLL0/1 supply LVDs) | Untrimmed | 1.122 | 1.157 | 1.192 | V |
| LVD12R-trim | | Trimmed | 1.142 | 1.157 | 1.172 | V |
| LVD12E | Low-Voltage Detection 1.25 V engage (Core VDD supply and PLL0/1 supply LVDs) | Untrimmed | 1.102 | 1.137 | 1.172 | V |
| LVD12E-trim | | Trimmed | 1.122 | 1.137 | 1.152 | V |
| HVD12R-trim | High-Voltage Detection 1.25 V release (Core VDD) | Trimmed | 1.33 | 1.35 | 1.37 | V |
| HVD12E-trim | High-Voltage Detection 1.25 V engage (Core VDD supply) | Trimmed | 1.36 | 1.38 | 1.40 | V |
| LVD_MIPI12R-trim | Low-Voltage Detection 1.25V release (MIPICSI2 DPHY supply) | — | 1.130 | 1.157 | 1.184 | V |
| LVD_MIPI12E-trim | Low-Voltage Detection 1.25V engage (MIPICSI2 DPHY supply) | — | 1.111 | 1.137 | 1.163 | V |
| POR-R-VDD_HV_PMU | 3.3 V PMU supply voltage POR release threshold | — | 2.54 | 2.645 | 2.735 | V |
| POR-E-VDD_HV_PMU | 3.3 V PMU supply voltage POR engage threshold | — | 2.50 | 2.60 | 2.695 | V |
| LVD33R | 3.3V Low-Voltage Detection Release Threshold (PMC, FLASH, IO, ADC) | Untrimmed | 2.90 | 3.02 | 3.13 | V |
| LVD33R-trim | | Trimmed | 3.00 | 3.05 | 3.10 | V |
| LVD33E | 3.3V Low-Voltage Detection Engage Threshold (PMC, FLASH, IO, ADC) | Untrimmed | 2.86 | 2.98 | 3.09 | V |
| LVD33E-trim | | Trimmed | 2.96 | 3.01 | 3.06 | V |
| HVD33R | 3.3V High-Voltage Detection Release Threshold (ADC) | Untrimmed | 3.45 | 3.61 | 3.75 | V |
| HVD33R-trim | | Trimmed | 3.47 | 3.53 | 3.58 | V |
| HVD33E | 3.3V High-Voltage Detection Engage Threshold (ADC) | Untrimmed | 3.51 | 3.65 | 3.79 | V |
| HVD33E-trim | | Trimmed | 3.51 | 3.57 | 3.62 | V |
| UVL30R | SMPS under-voltage lockout release threshold | Untrimmed | 2.75 | 2.90 | 3.05 | V |
| UVL25E | SMPS under-voltage lockout engage threshold | | 2.40 | 2.55 | 2.7 | V |
| DGLITCHE | Voltage Detector Deglitcher Filter Time - Engage | — | 2.0 | 3.5 | 5 | µs |
| DGLITCHR | Voltage Detector Deglitcher Filter Time - Release | — | 5 | 7 | 12 | µs |
| RSTDGLTC | VREG_POR_B Input Deglitch Filter Time | — | 200 | 320 | 500 | ns |
| RSTPUP | VREG_POR_B Pin Pull-up Resistance | — | 37 | 75 | 150 | kΩ |
| REGENPUP | VREG_SEL Pin Pull-up Resistance | — | 37 | 75 | 150 | kΩ |
| VSMPS | Internal switched regulator output voltage [1] | Load Current from 10 mA to 1.8 A | 1.19 | 1.255 | 1.35 | V |

*Table continues on the next page...*

## Table 9. Voltage regulator electrical specifications (continued)

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| FSMPS | Internal switched regulator operating frequency without modulation | Untrimmed | 0.65 | 1.00 | 1.35 | MHz |
| | | Trimmed | 0.93 | 1.00 | 1.07 | MHz |
| FSMPS-M7.5 | Internal switched regulator frequency modulation | — | — | 7.5 | — | % |
| FSMPS-M15 | | — | — | 15 | — | % |
| FSMPS-M30 | | — | — | 30 | — | % |
| VREGSWPUP | Internal switched regulator gate-driver pull-up resistance[2] | — | — | — | — | — |
| VREF_BG_T | PMC bandgap reference voltage for SARADC | Trimmed | 1.20 | 1.22 | 1.237 | V |
| Vih (VREG_POR_B) | VREG_POR_B pin High Voltage level | — | 0.7 x VDD_HV_PMU | — | VDD_HV_PMU + 0.3 | V |
| Vil (VREG_POR_B) | VREG_POR_B pin Low Voltage level | — | -0.3 | — | 0.3 x VDD_HV_PMU | V |
| LVDAFER | Low Voltage Detection 3.3V Release (AFE VDD_HV_DAC and VDD_HV_RAW supplies) | | 2.75 | 2.80 | 2.90 | V |
| LVDAFEE | Low Voltage Detection 3.3V Engage (AFE VDD_HV_DAC and VDD_HV_RAW supplies) | | 2.68 | 2.77 | 2.86 | V |

1. Min/Max includes transient load conditions. Steady state voltage is within the core supply operating specifications.
2. There is a strong pull up from VREG_SWP to VDD_HV_REG3V8 which is connected when SMPS is disabled. The pullup has resistance less than 1 Kohm, therefore VREG_SWP should not be connected to ground if unused.

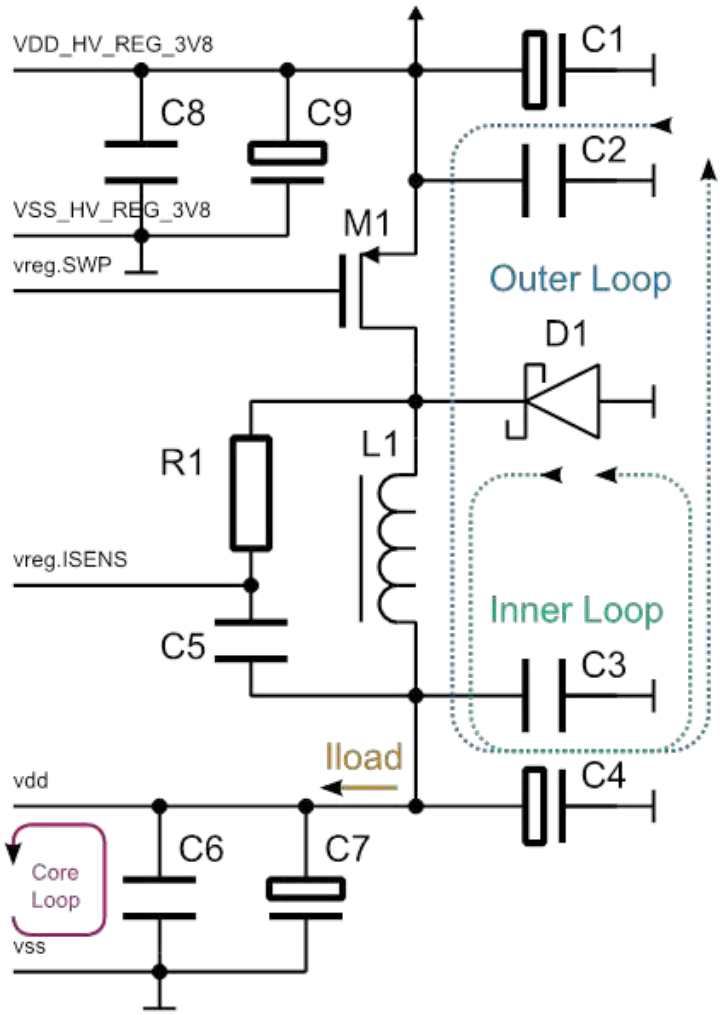


**Figure 2. SMPS External Components Configuration**

**Table 10. SMPS External Components**

| Ref | Description |
|---|---|
| M1 | SI3443, 2SQ2315 |
| L1 | 2.2 uH 3A < 100 mΩ series resistance (Ex. Bourns SRU8043-2R2Y) |
| D1 | SS8P3L 8A Schottcky Diode |
| R1 | 24 kΩ |
| C1 | 10 µF Ceramic |
| C2 | 100 nF Ceramic |
| C3 | 100 nF Ceramic (place close to inductor) |
| C4 | 10 uF Ceramic (place close to inductor) |
| C5 | 1 nF Ceramic |
| C6 | 4 x 100 nF + 4 x 10nF Ceramic (place close to MCU supply pins) |
| C7 | 4 x 10 µF Ceramic (place close to MCU supply pins) |
| C8 | 100 nF Ceramic |
| C9 | 1 µF Ceramic (Unless C1 is really close to the pin) |

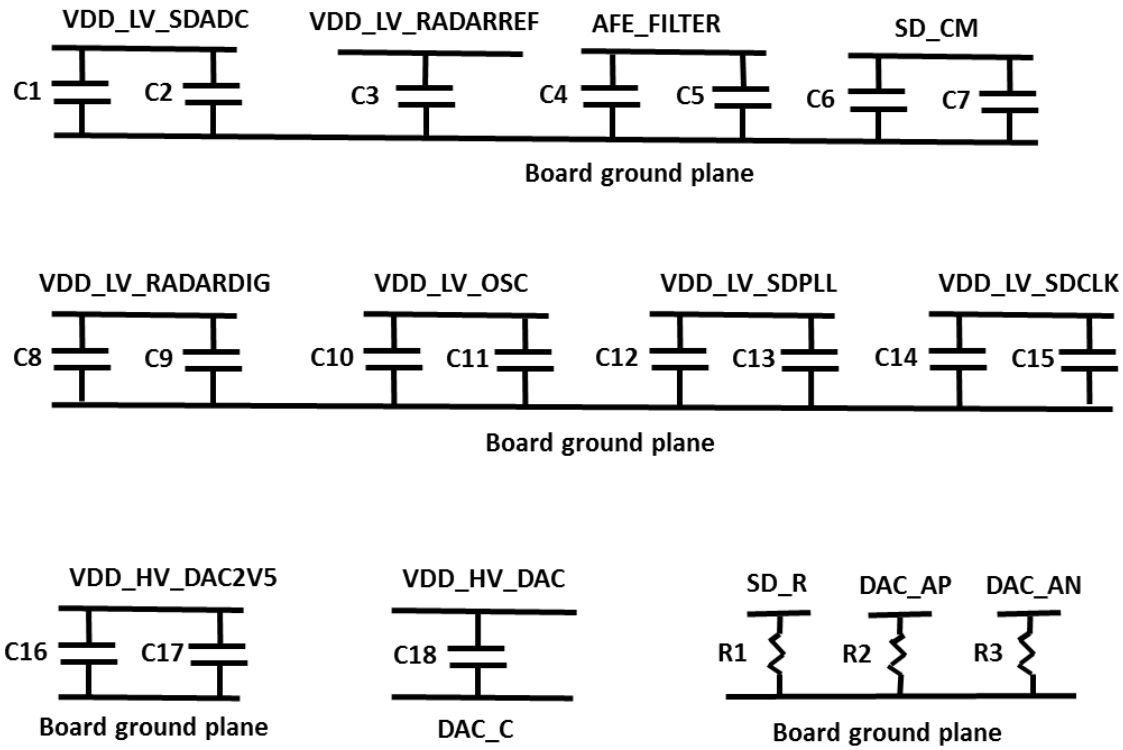


**Figure 3. Radar AFE External Components Configuration**

## Table 11. Radar AFE External Components

| Component | Component Value | Tolerance | Placement Priority of larger cap. [1] | Placement Priority of smaller cap[1] | Special notes |
|---|---|---|---|---|---|
| C1 | 0.47 µF | ±35% | 3 | — | — |
| C2 | 0.1 µF | ±35% | — | 1 | — |
| C3 | 1.0 µF | ±35% | 7 | — | — |
| C4 | 1.0 µF | ±35% | 2 | — | — |
| C5 | 0.1 µF | ±35% | — | 4 | — |
| C6 | 1.0 µF | ±35% | 8 | — | — |
| C7 | 0.1 µF | ±35% | — | 6 | — |
| C8 | 1.0 µF | ±35% | 6 | — | — |
| C9 | 0.1 µF | ±35% | — | 5 | — |
| C10 | 1.0 µF | ±35% | 4 | — | — |
| C11 | 0.1 µF | ±35% | — | 2 | — |
| C12 | 1.0 µF | ±35% | 5 | — | — |
| C13 | 0.1 µF | ±35% | — | 3 | — |
| C14 | 1.0 µF | ±35% | 10 | — | — |
| C15 | 0.1 µF | ±35% | — | 8 | — |
| C16 | 1.0 µF | ±35% | 9 | — | — |
| C17 | 0.1µF | ±35% | — | 7 | — |

*Table continues on the next page...*

**Table 11. Radar AFE External Components (continued)**

| Component | Component Value | Tolerance | Placement Priority of larger cap. [1] | Placement Priority of smaller cap[1] | Special notes |
|---|---|---|---|---|---|
| C18 | 10 µF | — | 1 | — | X7R type |
| C19 | 220 nF | — | — | — | Sigma Delta ADC input capacitor. See Figure 9 |
| C20 | 220 nF | — | — | — | Sigma Delta ADC input capacitor. See Figure 9 |
| R1 | 40.2 kΩ | ±0.1% | — | — | tempco = 25ppm/C |
| R2 | 300 Ω | — | — | — | DAC RI See Table 27 |
| R3 | 300 Ω | — | — | — | DAC RI See Table 27 |
| Crystal | 40MHz | — | — | — | Connected between XOSC_EXTAL/ XOSC_XTAL, ESR ≤ 30Ω |

1. All Radar AFE external bypass capacitors should be placed as close as possible to the associated package pin. As shown in Radar AFE External Components Configuration figure, most pins have two values of bypass capacitor. Greater than 0.1 µF is referred to as the larger cap. 0.1 µF is referred to as the smaller cap.

## 4.5 Electromagnetic Compatibility (EMC) specifications

EMC measurements to IC-level IEC standards are available from NXP on request.

## 4.6 Electrostatic discharge (ESD) characteristics

Electrostatic discharges (a positive then a negative pulse separated by 1 second) are applied to the pins of each sample according to each pin combination. The sample size depends on the number of supply pins in the device (3 parts × ($n$ + 1) supply pin). This test conforms to the AEC-Q100-002/-003/-011 standard.

**NOTE**

A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

**Table 12. ESD ratings**

| No. | Symbol | Parameter | Conditions[1] | Class | Max value[2] | Unit |
|---|---|---|---|---|---|---|
| 1 | $V_{ESD(HBM)}$ | Electrostatic discharge (Human Body Model) | $T_A$ = 25 °C | H1C | 2000 | V |

*Table continues on the next page...*

**Table 12. ESD ratings (continued)**

| No. | Symbol | Parameter | Conditions[1] | Class | Max value[2] | Unit |
|---|---|---|---|---|---|---|
| | | | conforming to AEC-Q100-002 | | | |
| 2 | $V_{ESD(CDM)}$ | Electrostatic discharge (Charged Device Model) | $T_A$ = 25 °C conforming to AEC-Q100-011 | C3A | 500[3] 750 (corners) | V |

1. All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.
2. Data based on characterization results, not tested in production.
3. 500 V for non-AFE pins, 250 V for AFE pins.

# 5 I/O Parameters

## 5.1 I/O pad DC electrical characteristics

NMI, TCK, TMS, JCOMP are treated as GPIO.

**Table 13. I/O pad DC electrical specifications**

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| Vih_hys | CMOS Input Buffer High Voltage (with hysteresis enabled) | 0.65*$V_{DD\_HV\_IO}$ | $V_{DD\_HV\_IO}$ + 0.3 | V |
| Vil_hys | CMOS Input Buffer Low Voltage (with hysteresis enabled) | -0.3 | 0.35*$V_{DD\_HV\_IO}$ | V |
| Vih | CMOS Input Buffer High Voltage (with hysteresis disabled) | 0.55 * $V_{DD\_HV\_IO}$ | $V_{DD\_HV\_IO}$ + 0.3 | V |
| Vil | CMOS Input Buffer Low Voltage (with hysteresis disabled) | -0.3 | 0.40 * $V_{DD\_HV\_IO}$ | V |
| Vhys | CMOS Input Buffer Hysteresis | 0.1 * $V_{DD\_HV\_IO}$ | — | V |
| $Vih_{TTL}$ | TTL Input high level voltage (All SAR_ADC input pins) | 2 | $V_{DD\_HV\_ADCREFx}$ + 0.3 | V |
| $Vil_{TTL}$ | TTL Input low level voltage (All SAR_ADC input pins) | -0.3 | 0.56 | V |
| $Vhyst_{TTL}$ | TTL Input hysteresis voltage (All SAR_ADC input pins) | 0.3 | — | V |
| Pull_Ioh | Weak Pullup Current[1] | 10 | 55 | µA |
| Pull_Iol | Weak Pulldown Current[2] | 10 | 55 | µA |
| Iinact_d | Digital Pad Input Leakage Current (weak pull inactive) | -2.5 | 2.5 | µA |
| Voh | Output High Voltage[3] | 0.8 * $V_{DD\_HV\_IO}$ | — | V |
| Vol | Output Low Voltage[4] | — | 0.2 * $V_{DD\_HV\_IO}$ | V |
| Ioh_f | Full drive Ioh[5] (ipp_sre[1:0] = 11) | 18 | 70 | mA |
| Iol_f | Full drive Iol[5] (ipp_sre[1:0] = 11) | 21 | 120 | mA |
| Ioh_h | Half drive Ioh[5] (ipp_sre[1:0] = 10) | 9 | 35 | mA |
| Iol_h | Half drive Iol[5] (ipp_sre[1:0] = 10) | 10.5 | 60 | mA |

1. Measured when pad = 0 V
2. Measured when pad = $V_{DD\_HV\_IO}$
3. Measured when pad is sourcing 2 mA
4. Measured when pad is sinking 2 mA
5. Ioh/Iol is derived from spice simulations. These values are NOT guaranteed by test.

### 5.1.1 RGMII pad DC electrical characteristics

**Table 14. RGMII pad DC electrical specifications**

| Symbol | Parameter | Value | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| Vih | CMOS Input Buffer High Voltage | 0.65 x $V_{DD\_HV\_IO}$ | $V_{DD\_HV\_IO}$ + 0.3 | V |
| Vil | CMOS Input Buffer Low Voltage | -0.3 | 0.35 x $V_{DD\_HV\_IO}$ | V |
| Pull_Ioh | Weak Pullup Current[1] | 10 | 55 | µA |
| Pull_Iol | Weak Pulldown Current[2] | 10 | 55 | µA |
| Iinact_d | Digital Pad Input Leakage Current (weak pull inactive) | -2.5 | 2.5 | µA |
| Voh | Output High Voltage[3] | 0.8 x $V_{DD\_HV\_IO}$ | — | V |
| Vol | Output Low Voltage[4] | — | 0.2 * $V_{DD\_HV\_IO}$ | V |
| Ioh_f | Full drive Ioh[5] | 8 | 26 | mA |
| Iol_f | Full drive Iol[6] | 8 | 24 | mA |

1. Measured when pad = 0 V
2. Measured when pad = $V_{DD\_HV\_IO}$
3. Measured when pad is sourcing 2 mA
4. Measured when pad is sinking 2 mA
5. Ioh_f value is measured with 0.8*VDDE applied to the pad.
6. Iol_f is measured when 0.2*VDDE is applied to the pad.

## 5.2 I/O pad AC specifications

AC Parameters are specified over the full operating junction temperature range of -40°C to +150°C and for the full operating range of the $V_{DD\_HV\_IO}$ supply defined in Table 7.

**Table 15. Functional Pad electrical characteristics**

| Symbol | Prop. Delay (ns)[1] L>H/H>L | | Rise/Fall Edge (ns)[2] | | Drive Load (pF) | SIUL2_MSCR[SRC] |
|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | | MSB,LSB |
| pad_sr_hv (output) | 2.5/2.5 | 8.25/7.5 | 0.7/0.6 | 3/3 | 50 | 11 |
| | 6.4/5 | 19.5/19.5 | 2.5/2.0 | 12/12 | 200 | |
| | 2.2/2.5 | 8/8 | 0.4/0.3 | 3.5/3.5 | 25 | 10 |
| | 2.9/3.5 | 12.5/11 | 1.0/0.8 | 6.5/6.5 | 50 | |
| | 11/8 | 35/31 | 6.5/3.0 | 25/21 | 200 | |

*Table continues on the next page...*

**Table 15. Functional Pad electrical characteristics (continued)**

| Symbol | Prop. Delay (ns)[1] L>H/H>L | | Rise/Fall Edge (ns)[2] | | Drive Load (pF) | SIUL2_MSCR[SRC] |
|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | | MSB,LSB |
| | 8.3/9.6 | 45/45 | 4/3.5 | 25/25 | 50 | 01[3] |
| | 13.5/15 | 65/65 | 6.3/6.2 | 30/30 | 200 | |
| | 13/13 | 75/75 | 6.8/6 | 40/40 | 50 | 00[3] |
| | 21/22 | 100/100 | 11/11 | 51/51 | 200 | |
| pad_sr_hv (input)[4] | | 2/2 | | 0.5/0.5 | 0.5 | NA |

1. As measured from 50% of core side input to Voh/Vol of the output
2. Measured from 20% - 80% of output voltage swing
3. Slew rate control modes
4. Input slope = 2ns

**NOTE**

Data based on characterization results, not tested in production.

**Table 16. Functional Pad AC Specifications**

| Symbol | Parameter | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| pad_sr_hv(Cp) | Parasitic Input Pin Capacitance | 4.5 | 4.7 | 5.0 | pF |

## 5.3 Aurora LVDS driver electrical characteristics

**NOTE**

The Aurora interface is AC coupled, so there is no common-mode voltage specification.

**Table 17. Aurora LVDS driver electrical characteristics**

| Symbol | Parameter[1] | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $F_{TXRX}$ | Data rate | — | — | 1.15 | Gbps |
| Transmitter Specifications | | | | | |
| $V_{diffout}$ | Differential output voltage swing (terminated) | +/- 400 | +/- 600 | +/- 800 | mV |
| $T_{rise}/T_{fall}$ | Rise/Fall time (10% - 90% of swing) | 60 | | | ps |
| Receiver Specifications | | | | | |
| $V_{diffin}$ | Differential voltage | +/- 100 | | +/- 800 | mV |
| Termination | | | | | |

*Table continues on the next page...*

**Table 17. Aurora LVDS driver electrical characteristics (continued)**

| Symbol | Parameter[1] | Value | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $R_{V\_L}$ | Terminating Resistance (external) | 99 | 100 | 101 | Ohms |
| $C_P$ | Parasitic Capacitance (pad + bondwire + pin) | | | 1 | pF |
| $L_P$ | Parasitic Inductance | | | 7 | nH |
| STARTUP | | | | | |
| $T_{STRT\_BIAS}$ | Bias startup time | — | — | 5 | µs |
| $T_{STRT\_TX}$ | Transmitter startup time[2] | — | — | 5 | µs |
| $T_{STRT\_RX}$ | Receiver startup time[2] | — | — | 5 | µs |
| LVDS_RXOUT[3] | Receiver o/p duty cycle | 30 | | 70 | % |

1. Conditions for these values are $V_{DD\_LV\_IO\_AURORA}$ = 1.19V to 1.32V, $T_J$ = –40 / 150 °C
2. Startup time is defined as the time taken by LVDS current reference block for settling bias current after its pwr_down (power down) has been deasserted. LVDS functionality is guaranteed only after the startup time.
3. Receiver o/p duty cycle is measured with 1.25 Gbps, 50% duty cycle, max 1 ns rise/fall time, 100 mV voltage swing signal applied at the receiver input.

## 5.4 Reset pad electrical characteristics

The device implements a dedicated bidirectional RESET_B pin.

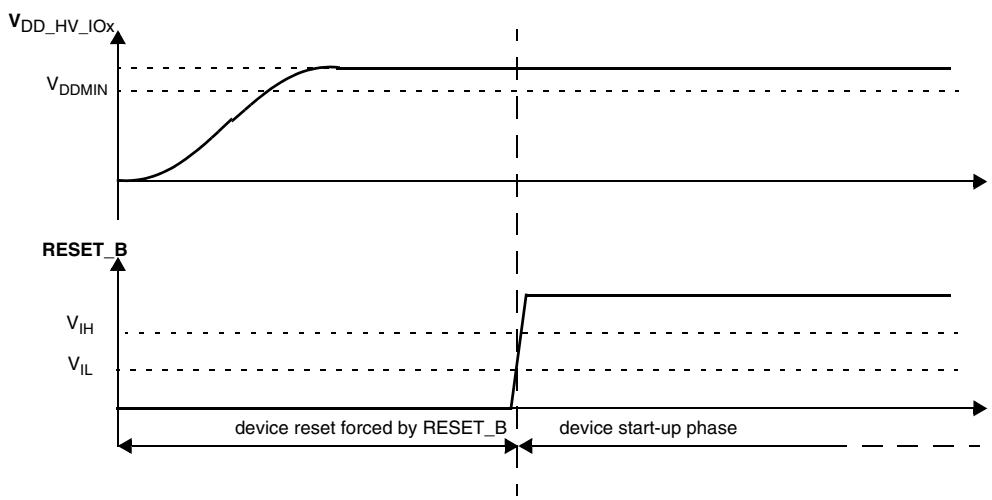


**Figure 4. Start-up reset requirements**

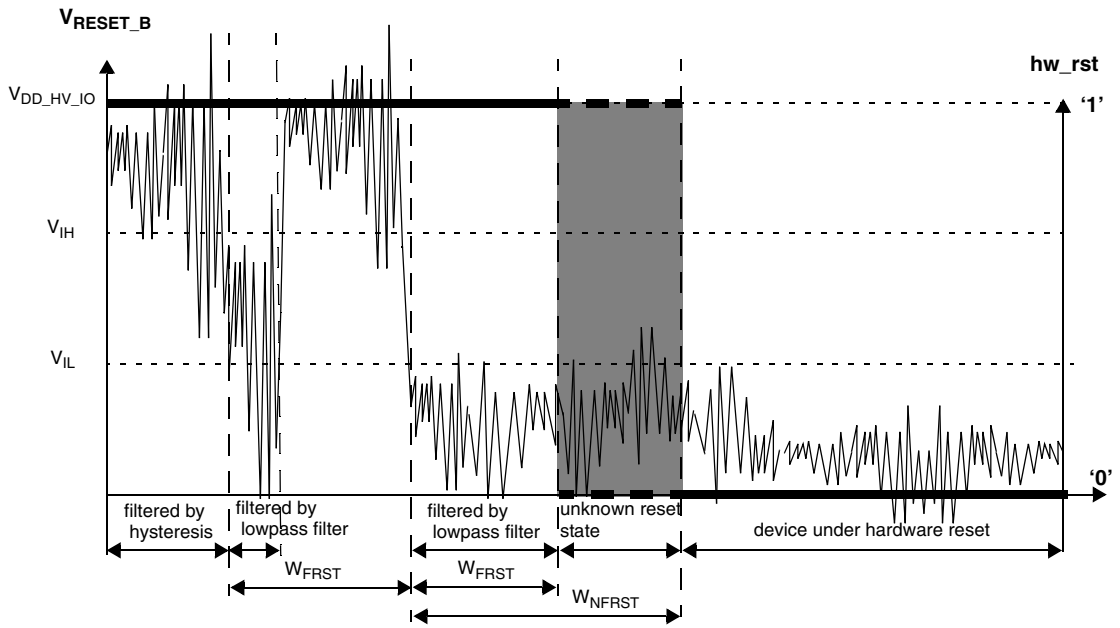


**Figure 5. Noise filtering on reset signal**

## Table 18. RESET_B electrical characteristics

| Symbol | Parameter | Conditions[1] | Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min | Typ | Max | |
| $V_{IH}$ | Input high level TTL (Schmitt Trigger) | — | 2.0 | — | $V_{DD\_HV\_IOx}$ + 0.4 | V |
| $V_{IL}$ | Input low level TTL (Schmitt Trigger) | — | –0.4 | — | 0.56 | V |
| $V_{HYS}$[2] | Input hysteresis TTL (Schmitt Trigger) | — | 300 | — | — | mV |
| $I_{OL\_R}$ | Strong pull-down current | Device under power-on reset<br>$V_{DD\_HV\_IO}$ = 1.2 V<br>$V_{OL}$ = 0.35 x $V_{DD\_HV\_IO}$ | 0.2 | — | — | mA |
| | | Device under power-on reset<br>$V_{DD\_HV\_IO}$=3.0 V<br>$V_{OL}$ = 0.35 x $V_{DD\_HV\_IO}$ | 15 | — | — | mA |
| $W_{FRST}$ | RESET_B input filtered pulse | — | — | — | 500 | ns |
| $W_{NFRST}$ | RESET_B input not filtered pulse | — | 2400 | — | — | ns |
| $\lvert I_{WPD} \rvert$ | Weak pull-down current absolute value | $V_{IN}$ = $V_{DD\_HV\_IOx}$ | 30 | — | 100 | µA |

1. $V_{DD\_HV\_IOx}$ = 3.3 V -5%,+10%, $T_J$ = –40 / 150°C, unless otherwise specified.
2. Data based on characterization results, not tested in production.