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S32V234

S32V234 Data Sheet

Features

- ARM® Cortex®-A53, 64-bit CPU
  - Up to 1000 MHz Quad ARM Cortex-A53
  - 32 KB/32 KB I-/D- L1 Cache
  - NEON MPE co-processor
  - Dual precision FPU
  - 2 clusters with 2 CPUs and 256 KB L2 cache each
  - Memory Management Unit
  - GIC Interrupt Controller
  - ECC/parity error support for its memories
  - Generic timers
  - Fault encapsulation by hardware for redundant executed application software on multiple core cluster
- ARM Cortex-M4, 32-bit CPU
  - Up to 133 MHz
  - 16 KB/16 KB I-/D- L1 Cache
  - 32+32 KB tightly coupled memory (TCM)
  - ECC/parity support for its memories
- Clocks
  - Phase Locked Loops (PLLs)
  - 1 external crystal oscillator (FXOSC)
  - 1 FIRC oscillator
- System protection and power management features
  - Flexible run modes to consume low power based on application needs
  - Peripheral clock enable register can disable clocks to unused modules, thereby reducing currents
  - Power gating of unused A53 cores and GPU
  - Low and high voltage warning and detect
  - Hardware CRC module to support fast cyclic redundancy checks (CRC)
  - 120-bit unique chip identifier
  - Hardware watchdog
  - eDMA controller with 32 channels (with DMAMUX)
  - Extended Resource Domain Controller
- Safety concept
  - ISO 26262, ASIL level target
  - Measures to detect faults in memory and logic
  - Measures to detect single point and latent faults
  - Quantitative out of context analysis of functional safety (FMEDA) tailored to application specifics
  - Safety manual and FMEDA report available
- Security
  - CSE with 16 KB of on-chip Secure RAM and ROM.
  - ARM TrustZone (TZ) architecture support
  - Boot from NOR flash with AES-128 (CTR)
  - On-Chip One-Time Programmable element Controller (OCOTP_CTRL) with on chip electrical fuse array.
  - System JTAG Controller (SJC)
- Debug functionality
  - Standard JTAG and Compact JTAG
  - 16-bit Trace port, Serial Wire Output port
- Timers
  - General purpose timers (FTM)
  - Two Periodic Interrupt Timer (PIT)
  - IEEE 1588 Timers (part of Ethernet Subsystem)
- Analog
  - 1x 12-bit 1.8 V SAR ADC with self-test
- Communications
  - UART(w/ LIN2.1l)
  - Serial peripheral interface (SPI)
  - I2C blocks
  - PCI express 2.0 with endpoint and root complex support
  - LFAST serial link
  - 1 GBit Ethernet with PTP IEEE 1588
  - FD-CAN
  - FlexRay Dual Channel, Version 2.1 RevA

NXP reserves the right to change the production detail specifications as may be required to permit improvements in the design of its products.

- Memory interfaces
  - 32-bit DRAM Controller with support for LPDDR2/DDR3/DDR3L - Data rate of up to 1066 MT/s at 533 MHz clock frequency with ECC (SEC-DED-TED) triple error detection support for subregion
  - QuadSPI supporting Execute-In-Place (XIP)
  - Boot flash fault detection and correction using two-dimensional parity.
  - Triple fault detection and single fault correction scheme for external DDR-RAM including address/page fault detection.
- Video input interfaces, Image processing, graphics processing, display
  - Display Control Unit (2D-ACE) with 24-bit RGB, GPU frame buffer decoding
  - GPU GC3000 with frame buffer compression
  - 2x VIU (Video interface unit) for camera input
  - 2x MIPICSI2 with four lanes for camera input (support 1080 pixel @ 30 fps)
  - Image signal processor (ISP), supporting 2x1 or 1x2 megapixel @ 30 fps and 4x2 megapixel for subset of functions (exposure control, gamma correction)
  - 2x APEX2-CL Image cognition processor. APEX-642CL comprises two Array Processing Unit (APU) cores configurable as single SIMD engine with 64 16-bit Computational Units (CU), or configurable as two core MIMD engines with 32 16-bit CUs each.
  - CUs are comprised of four Functional Units: 16-bit Multiplier, Load Store Unit, ALU, and Shifter
  - JPEG video decoder (8/12-bit)
  - H.264 video decoder (8/10/12-bit), High-intra and constrained baseline formats
  - H.264 video encode (8/10/12-bit), High-intra only
  - Fast DMA for data transfers between DRAM and System RAM with CRC
- Human-Machine Interface (HMI)
  - GPIO pins with interrupt support, DMA request capability, digital glitch filter
  - Configurable slew rate and drive strength on all output pins
- System RAM
  - 4 MB On-Chip System RAM with ECC

Table of Contents

1 Block diagram

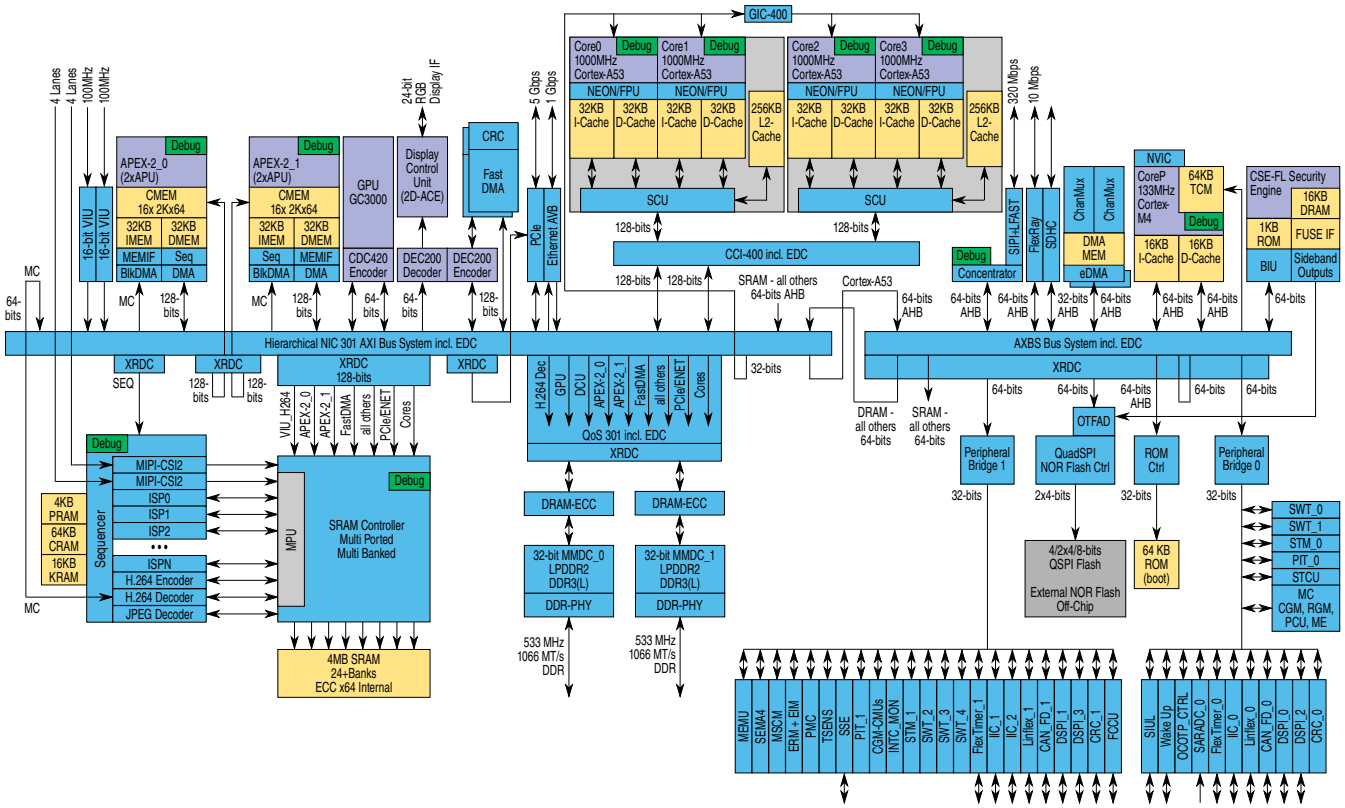

Figure 1. Block diagram

2 Family comparison

2.1 Feature Set

This family of devices supports the following features:

Table 1. Feature Set

Feature	S32V234	S32V232
ARM Cortex-A53 Core	• Up to 1000 MHz Quad ARM Cortex-A53 • 32 KB/32 KB I-/D- L1 Cache • NEON MPE co-processor • Dual precision FPU • 256 KB L2 Cache per cluster • MMU • GIC interrupt controller	• Up to 800 MHz Dual ARM Cortex-A53 (single cluster) • Rest all features same as S32V234

Table continues on the next page...

Table 1. Feature Set (continued)

Feature	S32V234	S32V232
	• ECC/parity error support for its memories • Generic timers	
ARM Cortex-M4 Core	• Up to 133 MHz • 16 KB/16 KB I-/D- L1 Cache • 32+32 KB tightly coupled memory (TCM) • ECC/parity support for its memories	• Same as S32V234
Clocks	• Phase Locked Loops (PLLs) • 1 external crystal ocillators (FXOSC) • 1 FIRC	• Same as S32V234
System, protection and power management features	• Flexible run modes to consume lower power based on application needs. • Peripheral clock enable registers can disable clocks to unused modules, thereby reducing currents • Low and high voltage warning and detect • Hardware CRC module to support fast cyclic redundancy checks (CRC) • 120-bit unique chip identifier • Hardware watchdog • Safe eDMA controller with 32 channels (with DMAMUX) • Extended Resource Domain Controller	• Same as S32V234
Safety concept	• ISO 26262, ASIL level target as per safety concept • Measures detecting faults in memory and logic • Measures to detect single point and latent faults • Quantitative out of context analysis of functional safety (FMEDA) tailored to application specifics • Safety manual and FMEDA report available • Boot flash authentication and fault detection and correction using AES-128 and two-dimensional parity. • Double and triple fault detection and single fault correction scheme for external DDR-RAM including address/ page fault detection. • Fault encapsulation by hardware for redundant executed application software on multiple core cluster. • Structural software based self test routines providing high diagnostic coverage.	• Same as S32V234
Debug	• Standard JTAG • 16-bit Trace port, Serial Wire Output port	• Same as S32V234
Timers	• General purpose timers (FTM)	• Same as S32V234

Table continues on the next page...

Table 1. Feature Set (continued)

Feature	S32V234	S32V232
	• Two Periodic Interrupt Timer (PIT) • IEEE 1588 Timers (part of Ethernet Subsystem)	
Communications	• UART(w/ LIN2.1l) • Serial peripheral interface (SPI) • I2C blocks • PCI express 2.0 with endpoint and root complex support • LFAST serial link • 1 GBit Ethernet with PTP IEEE 1588 • FD-CAN • Flexray Dual Channel, Version 2.1 RevA	• UART(w/ LIN2.1l) • Serial peripheral interface (SPI) • I2C blocks • LFAST serial link • 1 GBit Ethernet with PTP IEEE 1588 • FD-CAN • Flexray Dual Channel, Version 2.1 RevA
Memory Interfaces	• 32-bit DRAM Controller with support for LPDDR2/DDR3/DDR3L - Data rate of up to 1066 MT/s at 533 MHz clock frequency with ECC (SEC-DED-TED) single error correction, double error detection, and triple error detection support for subregion • Dual QuadSPI supporting Execute-In-Place (XIP)	• Same as S32V234
Video input interfaces, Image processing, graphics processing, display	• Display Control Unit (2D-ACE) with 24-bit RGB, GPU framebuffer decoding • GPU GC3000 with frame buffer compression • 2x Video interface unit (VIU) for camera input • 2x CSI with 4 lanes for camera input (support 1080p @ 30fps) • Image signal processor (ISP), supporting 2x1 or 1x2 MPixel @ 30fps and 4x1 MPixel for subset of functions (exposure control, gamma correction) • 2x APEX2-CL Image cognition processor (dual 32-bit array processor) • JPEG video decoder (8/12-bit) • H.264 video decoder (8/10/12-bit), High-intra and constrained baseline formats • H.264 video encoder (8/10/12-bit), I-frames only • Safe Fast DMA for data transfers between DRAM and System RAM with CRC	• Same as S32V234
Analog	• 1x 12-bit SAR ADC with self-test	• Same as S32V234
Human-Machine Interface (HMI)	• SIUL, GPIO pins with interrupt support, DMA request capability, digital glitch filter. • Configurable slew rate and drive strength on all output pins	• Same as S32V234
System RAM	• 4 MB On-Chip System RAM with ECC	• 3 MB On-Chip System RAM with ECC
Power Consumption	• Run modes:	• Same as S32V234

Table 1. Feature Set

Feature	S32V234	S32V232
	• Frequency scaling and clock gating for processing blocks and peripherals in run mode	

3 Ordering parts

3.1 Ordering information

The orderable part numbers of this chip are in the table below:

Table 2. Ordering information

Part number	ISP	GPU	CSE	Low power (leakage based)	No. of cores	Frequency
FS32V234CMN1VUB	Yes	Yes	No	No	4	1 GHz
FS32V234CON1VUB	Yes	Yes	Yes	No	4	1 GHz
FS32V234BMN1VUB	Yes	Yes	No	No	4	800 MHz
FS32V234BJN1VUB	Yes	No	No	Yes	4	800 MHz
FS32V232BMN1VUB	Yes	Yes	No	No	2	800 MHz
FS32V234BLN1VUB	Yes	No	Yes	Yes	4	800 MHz
FS32V234CKN1VUB	Yes	No	Yes	No	4	1 GHz

4 General

4.1 Operation above maximum operating conditions

Table 3. Operation above maximum operating conditions

1.8 V DGO Voltage Domain			
Electrical Specifications	Value	Conditions	Junct Temp
Absolute Maximum Supply Voltage	3.0 V	< 60 s	25 °C
Absolute Maximum Supply Voltage	2.3 V	< 10 hr	25 °C
Operating Max Supply Voltage	1.98 V	—	—

Table continues on the next page...

Table 3. Operation above maximum operating conditions (continued)

Core Voltage Domain			
Electrical Specifications	Value	Conditions	Junct Temp
Absolute Maximum Supply Voltage	1.29 V	< 60 s	25 °C
Absolute Maximum Supply Voltage	1.1 V	< 10 hr	25 °C
Operating Max Supply Voltage	1.05 V	—	—
3.3 V DGO Voltage Domain			
Electrical Specifications	Value	Conditions	Junct Temp
Absolute Maximum Supply Voltage	4.95 V	< 60 s	25 °C
Absolute Maximum Supply Voltage	4.29 V	< 10 hr	25 °C
Operating Max Supply Voltage	3.6 V	—	—

4.2 Recommended operating conditions

Table 4. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DD_GPIO0}	3.3 V I/O segment GPIO0 supply voltage	—	3.15	3.6	V
$V_{DD\_GPIO<n=1,2>}$	1.8 V input/output supply voltage	—	1.71	1.95	V
$V_{DD\_HV\_IO\_VIU0}$ $V_{DD\_HV\_IO\_VIU1}$ $V_{DD\_HV\_IO\_DIS}$ $V_{DD\_HV\_IO\_FLA}$	3.3 V input/output supply voltage	—	3.15	3.6	V
$V_{DD\_HV\_IO\_ETH}$	1.5 V I/O supply voltage	—	1.425	1.575	V
	1.8 V I/O supply voltage	—	1.71	1.95	V
	2.5 V I/O supply voltage	—	2.375	2.625	V
	3.3 V I/O supply voltage	—	3.15	3.6	V
V_{SS}	Common ground voltage[1]	—	0	0	V
$V_{DD\_LV\_CORE\_SOC}$, $V_{DD\_LV\_CORE\_ARM}$, $V_{DD\_LV\_CORE\_GPU}$	1.0 V core domain supply voltage[2]	—	0.95	1.05	V
$V_{DD\_HV\_CSI}$	1.8 V supply voltage (for MIPICSI2 D PHY)	—	1.71	1.95	V
$V_{DD\_LV\_CSI}$	1.0 V supply voltage (for MIPICSI2 D PHY)	—	0.95	1.05	V
$V_{DD\_HV\_PLL}$, $V_{DD\_HV\_LFASTPLL}$, $V_{DD\_HV\_FXOSC}$,	1.8 V supply voltage (for analog circuits, PLLs)	—	1.71	1.95	V

Table continues on the next page...

Table 4. Recommended operating conditions (continued)

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DD\_HV\_PMC}$, V_{DDIO_LFAST}, $V_{DD\_HV\_EFUSE}$, $V_{DD\_HV\_DDR}$					
$V_{DD\_LV\_PLL}$ $V_{DD\_LV\_POST}$	1.0 V supply voltage (for analog circuits, PLLs)	—	0.95	1.05	V
V_{REFH_ADC}	1.8 V ADC high reference voltage	—	1.71	1.95	V
$V_{DD\_HV\_ADV}$	1.8 V ADC supply voltage	—	1.71	1.95	V
$V_{SS\_HV\_ADV}$	ADC ground and low reference voltage	—	0	0	V
V_{REFL_ADC}	1.8 V ADC supply ground	—	0	0	V
$V_{DD\_DDR\_IO}$	DDR I/O supply voltage LPDDR2	—	1.14	1.30	V
	DDR I/O supply voltage DDR3	—	1.425	1.575	V
	DDR I/O supply voltage DDR3L	—	1.283	1.45	V
P_{CIE_VP}	PCIe supply voltages	—	0.95	1.05	V
P_{CIE_VPH}		—	1.71	1.95	V
T_A	Ambient temperature	—	-40	105[3]	°C
T_J	Junction temperature under bias	—	-40	125	°C
TV_{DD}	Supply ramp rate for all supplies on the device	—	0.05	25	V/ms

1. All the grounds viz. V_{SS}, V_{SS_XOSC}, and $V_{SS\_HV\_ADV}$ are tied together at the package level.
2. $V_{DD\_LV\_CORE\_SOC}$, $V_{DD\_LV\_CORE\_ARM}$, and $V_{DD\_LV\_CORE\_GPU}$ supply balls should all be connected together to one power plane and one regulator to avoid voltage level differences. If the GPU is power gated as it is not used, the $V_{DD\_LV\_CORE\_GPU}$ supply balls have to be statically connected to the ground plane. If the second ARM CPUs per cluster is power gated as they are not used, the $V_{DD\_LV\_CORE\_ARM}$ supply balls have to be statically connected to the ground plane.
3. Maximum ambient temperature requires management of the heat dissipation to ensure the device junction temperature does not exceed the maximum.

4.3 Power Management Controller (PMC) electrical specifications

PMC is composed of the following blocks:

- Low voltage detector (LVD_33_PMC) for 3.3 V VDD_GPIO0 supply (GPIO segment and PMC) and Low Voltage Detector for FIRC (VDD_HV_OSC)
- Low voltage detector (LVD_18) for VDD_HV_PMC
- Low voltage detector (LVD_18) for VDD_HV_FXOSC
- High voltage detector (HVD_18) for VDD_HV_PMC
- Low voltage detector (LVD_CORE) for VDD_LV_CORE_SOC
- High voltage detector (HVD_CORE) for VDD_LV_CORE_SOC
- Power on Reset (POR)

Table 5. PMC electrical specifications

Supply	Parameter	Conditions	Threshold	Min	Typical	Max	Status during power-up	Unit
VDD_LV_CORE_SOC	low voltage monitoring	Native	VTL[1]	836	880	924	Enabled	mV
			VTH[2]	850	895	940		
		Trimmed	VTL	896	910	924		
			VTH	911	925	946		
VDD_LV_CORE_SOC	high voltage monitoring	Trimmed	VTL	1049	1065	1093	Disabled	mV
			VTH	1064	1080	1093		
VDD_HV_PMC	PMC supply low voltage monitor	Native	VTL	1511	1590	1670	Enabled	mV
			VTH	1525	1605	1685		
		Trimmed	VTL	1620	1650	1680		
			VTH	1635	1665	1695		
VDD_HV_PMC	PMC supply high voltage monitor	Trimmed	VTL	2004	2045	2086	Disabled	mV
			VTH	2019	2060	2101		
VDD_GPIO0	low voltage monitor	Native	VTL	2727	2870	3014	Enabled	mV
			VTH	2746	2890	3035		
		Trimmed	VTL	2857	2915	2973		
			VTH	2876	2935	2994		
VDD_HV_OSC	OSC supply low voltage monitor	Native	VTL	1511	1590	1670	Enabled	mV
			VTH	1525	1605	1685		
		Trimmed	VTL	1620	1650	1680		
			VTH	1635	1665	1695		
PMC_BGREF	PMC Band Gap Reference value	Trimmed	–	1176	1200	1224	Enabled	mV

1. Lower threshold/assert point
2. Upper threshold/release point

4.4 Power consumption

The following table shows the power consumption data. These specifications are subject to change per device characterization.

Table 6. Power consumption

Parameter	Description	Max Values
VDD_LV_CORE[1, 2]	S32V234 Device in reset 'front view/low power part' @ 125 °C	3 A

Table continues on the next page...

Table 6. Power consumption (continued)

Parameter	Description	Max Values
	S32V232 Device in reset 'low power part' w/o GPU and w/o A53 CPU3 and CPU4 @ 125 °C	2.7 A
	S32V234 Device in reset 'high speed part' with GPU @ 125 °C	6.4 A
	S32V234 Device in reset 'high speed part' without GPU @ 125 °C	4.8 A
	Adder 4x A53 CPU with Dhrystone MIPS running on each CPU @1 GHz [3]	1.4 A
VDD_HV_CSI	Current for both MIPICSI2 interfaces operating as per 1) RX Operation at 1.5 Gbps per MIPICSI2 2) MIPICSI2 not used (IP Powered and Disabled)	1) 10 mA 2) 1 mA
VDD_LV_CSI	Current for both MIPICSI2 interfaces operating as per 1) RX Operation at 1.5 Gbps per MIPICSI2 2) MIPICSI2 not used (IP Powered and Disabled)	1) 40 mA 2) 13 mA
VDD_HV_PLL	All five PLLs operating at 1 GHz VCO frequency	35 mA
VDD_HV_LFASTPLL	Use case: 1) PLL operating with 320 MHz (LFAST used) 2) PLL not operational (LFAST not used)	1) 26 mA 2) .1 mA
VDD_HV_FXOSC	Shared supply for FXOSC operating with 40 MHz crystal and FIRC oscillator	5 mA
VDD_HV_PMC	As per default usage (no use case differentiation)	10 mA
VDD_HV_EFUSE	Use case: 1) eFuse programming happening	1) 10 mA
VDD_LV_PLL	All five PLLs operating at 1 GHz VCO frequency	80 mA
PCIE_VP	Use case: 1) 5 GHz operation (PCIe 2.0) 2) Reset/idle	1) 80 mA 2) 30 mA
PCIE_VPH	Use case: 1) 5 GHz operation (PCIe 2.0) 2) Reset/idle	1) 50 mA 2) 20 mA

1. Data represented is at 125 °C and 1.01 V vdd conditions
2. Includes SoC, GPU, and ARM supply combinations depending on use case description.

3. Adder to the static idd current component. 4xCortex A53 executing Dhrystone MIPS in AArch64 and the interconnect, System RAM, FastDMA, Cortex M4, peripheral bridges, FCCU, CSE, MEMU, PCIe, and STCU are clocked - static power consumption excluded.

4.5 Electrostatic discharge (ESD) specifications

Electrostatic discharges are applied to the pins of each sample in conformity with AEC-Q100-002/-011 to meet the HBM and CDM ratings described below.

Table 7. ESD ratings[1]

Symbol	Parameter	Conditions	Class	Max value[2]	Unit
$V_{ESD(HBM)}$	Electrostatic discharge (Human Body Model)	T_A = 25 °C conforming to AEC-Q100-002	H1C	2000	V
$V_{ESD(CDM)}$	Electrostatic discharge (Charged Device Model)	T_A = 25 °C conforming to AEC-Q100-011	C3A	500	V
				750 (corners)	V

1. A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.
2. Data based on characterization results, not tested in production.

4.6 Electromagnetic Compatibility (EMC) specifications

EMC measurements to IC-level IEC standards are available from NXP on request.

4.7 PCB routing guidelines

DDR3/DDR3L PCB design

- CLK/Addess/Commands
  - Route with 50 ohm controlled impedance and differential pair (CLK) with 100 ohm controlled impedance
  - Use Fly by topology in case of multiple memory components
  - Address and command lines Terminated to VTT with 50 ohm
  - To be referenced with Power, not Ground
  - Address/Cmd to be routed within 66 mils with respect to CLK and to be matched from controller to memory; memory to memory as well
  - All traces to be routed in internal layers
  - Preference is to use only two layers for routing this group
  - Limit the via number to less than three

NOTE

The differential clock lines on the DDR3 interface should use AC termination scheme, with a 0.1 μF series capacitor and referenced to DDR IO supply ($V_{DD\_DDR\_IO}$).

- Data/Strobe
  - Route with 50 ohm controlled impedance and differential pair (DQS strobe) with 100 ohm controlled impedance
  - Data to be routed within 33 mils with respect to respective strobe
  - To be referenced with Ground
  - All traces to be routed in internal layers
  - Strictly to be routed in only two layers
  - Avoid more than two vias

LPDDR2 PCB design

- CLK/Addess/Commands
  - Route with 50 ohm controlled impedance and differential pair (CLK) with 100 ohm controlled impedance
  - To be referenced with Power, not Ground
  - Address/Cmd to be routed within 66 mils with respect to CLK and to be matched from controller to memory
  - All traces to be routed in internal layers and delay should be less than 150 ps
  - Preference is to use only two layers for routing this group
  - Limit the via number to less than three
- Data/Strobe
  - Route with 50 ohm controlled impedance and differential pair (DQS strobe) with 100 ohm controlled impedance
  - Data to be routed within 33 mils with respect to respective strobe
  - To be referenced with Ground
  - All traces to be routed in internal layers and delay should be less than 150 ps
  - Strictly to be routed in only two layers
  - Avoid more than two vias

GPIO Interfaces

- QuadSPI
  - Put 22 ohm series termination on board when operating with DSE <2:0> 111
- TRACE
  - Put 22 ohm series termination on board when operating with DSE <2:0> 111
- ENET
  - Put 22 ohm series termination on board when operating with DSE <2:0> 111

5 I/O parameters

5.1 General purpose I/O parameters

5.1.1 GPIO speed at various voltage levels

NOTE

Rise/fall times numbers in Datasheet are guaranteed by design; to obtain actual rise/fall times parameters with specific packages and boards, use appropriate I/O IBIS model.

Table 8. GPIO rise/fall times (1.8 V range)

Parameter	Symbol	Drive strength ipp_dse<1:0>	Slew rate	Test conditions	Typ	Max	Unit
IO output transition time, rise/fall[1]	tpr	011	slow	15 pF Cload on pad ipp_do input transition time 120 ps		2.56/2.51	ns
			fast			1.97/2.20	
		100	slow			3.08/3.02	
			fast			2.59/2.58	
		101	slow			2.56/2.42	
			fast			1.84/1.96	
		111	slow			1.82/1.67	
			fast			1.13/1.24	

1. Max condition: wcs model, 0.9 V vddi, 1.62 V ovdd, and 125 °C. Input transition time is 120 ps.

   Slow slew rate means ipp_fsel = ‘00’, fast slew rate means ipp_fsel = ‘11’

Table 9. GPIO rise/fall times (2.5 V range)

Parameter	Symbol	Drive strength ipp_dse<1:0>	Slew rate	Test conditions	Typ	Max	Unit
IO output transition time, rise/fall[1]	tpr	011	slow	15 pF Cload on pad ipp_do input transition time 120 ps		3.44/3.04	ns
			fast			2.75/2.55	
		100	slow			4.05/3.54	
			fast			3.56/2.97	
		101	slow			3.39/2.93	
			fast			2.72/2.47	
		111	slow			2.31/2.03	
			fast			1.80/1.75	

1. Max condition for tpr: wcs model, 0.9 V vddi, 2.25 V ovdd, and 125 °C. Input transition time is 125 ps. Slow slew rate means ipp_fsel = ‘00’, fast slew rate means ipp_fsel = ‘11’

Table 10. GPIO rise/fall times (3.3 V range)

Parameter	Symbol	Drive strength ipp_dse<1:0>	Slew rate	Test conditions	Typ	Max	Unit
IO output transition time, rise/fall[1]	tpr	011	slow	15 pF Cload on pad ipp_do input transition time 120 ps		3.47/3.16	ns
			fast			2.90/2.73	
		100	slow			4.09/3.58	
			fast			3.73/3.07	
		101	slow			3.29/3.00	
			fast			2.68/2.37	
		111	slow			2.23/2.18	
			fast			1.47/1.57	

1. Max condition for tpr: wcs model, 0.9 V vddi, 2.97 V ovdd, and 125 °C. Input transition time is 120 ps.
   slow slew rate means ipp_fsel = '00', fast slew rate means ipp_fsel = '11'

5.1.2 DC electrical specifications

Table 11. DC electrical specifications

Symbol	Parameter	Test conditions	Min	Typ	Max	Unit
Voh	High-level output voltage	Ioh=-100 µA	ovdd[1]-0.15	—	—	V
Vol	Low-level output voltage	Iol=100 µA	—	—	0.15	V
Vihf	High-Level DC input voltage	—	0.7*ovdd	—	ovdd	V
Vil	Low-Level DC input voltage	—	0	—	0.2*ovdd	V
Iin[2]	Input current (no pull-up/down)	Vin = ovdd or 0	—	—	8	µA
Iin_33pu[2]	Input current (33 kilohm PU)	Vin = 0	—	—	220	µA
		Vin = ovdd			6	
Iin_50pu[2]	Input current (50 kilohm PU)	Vin = 0	—	—	150	µA
		Vin = ovdd			6	
Iin_100pu[2]	Input current (100 kilohm PU)	Vin = 0	—	—	60	µA
		Vin = ovdd			6	
Iin_100pd[2]	Input current (100 kilohm PD)	Vin = 0	—	—	8	µA
		Vin = ovdd			50	

1. ovdd is the IO supply for the pads.
2. Max condition: bcs model, 3.6 V, and 125 °C. These values are for I/O buffers.

NOTE

After bootup, application software should switch to manual voltage detect mode using VSEL_x settings of SRC_GPR14 register to ensure optimum performance of the GPIO pads.

Please refer to SRC chapter in the Reference Manual for the register details.

Table 12. Current-draw Characteristics for DDR_VREF

Symbol	Parameter	Min	Max	Unit
DDR_VREF	Current-draw characteristics for DDR_VREF	—	1	mA

5.2 DDR pads

5.2.1 Boot Configuration Pins Specification

Value driven on RCON and BOOTMOD pins should be stable for atleast 1 µs after RESET pin is deasserted.

5.2.2 DDR3 mode

5.2.2.1 DDR3 mode DC electrical specifications

Table 13. DDR3 mode DC electrical specifications

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
High-level output voltage	Voh	Ioh=-100 µA	0.8*ovdd	—	—	V
Low-level output voltage	Vol	Iol=100 µA	—	—	0.2*ovdd	V
High-level DC input voltage	Vih (DC)	—	Vref + 0.2	—	ovdd	V
High-level DC input voltage	Vil (DC)	—	ovss	—	Vref - 0.2	V
Input reference voltage	Vref	—	0.49*ovdd	0.5*ovdd	0.51*ovdd	V
Termination voltage[1]	Vtt	—	0.49*ovdd	0.5*ovdd	0.51*ovdd	V
Input current (no pullup/pulldown)[2]	Iin	Vi = 0 or ovdd	—	—	5	µA
Pullup/pulldown impedance mismatch	MMpupd	34 Ohm full strength driver	-10	—	+10	%
Driver 240 Ohm unit calibration resolution	Rres	—	—	—	10	Ω
Rkeep[3]	Pad keeper resistance	—	20	—	50	kΩ

1. Vtt is expected to track ovdd/2.
2. Typ condition: typ model, 1.5V, and 25 °C. Max condition: bcs model, 1.575V, and -40 °C. Min condition: wcs model, 1.425V, and 125 °C.

3. Typ condition: typ model, 1.5 V, and 25 °C, max condition: wcs model, 1.425 V, and 125 °C, min condition: bcs model, 1.575 V, and -40 °C.

5.2.3 DDR3L mode

5.2.3.1 DDR3L mode DC electrical specifications

Table 14. DDR3L mode DC electrical specifications

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
High-level output voltage	Voh	Ioh = -100 µA	0.8*ovdd	—	—	V
Low-level output voltage	Vol	Iol = 100 µA	—	—	0.2*ovdd	V
High-level DC input voltage	Vih (DC)	—	Vref + 0.2	—	ovdd	V
High-level DC input voltage	Vil (DC)	—	ovss	—	Vref - 0.2	V
Input reference voltage	Vref	—	0.49*ovdd	0.5*ovdd	0.51*ovdd	V
Vref current draw	Icc-vref	—	—	—	1	mA
Termination voltage	Vtt	—	0.49*ovdd	0.5*ovdd	0.51*ovdd	V
Input current (no pullup/pulldown)	Iin	Vi = 0 or ovdd	—	—	5	µA
Pullup/pulldown impedance mismatch (full strength driver)	MMpupd	—	-10	—	+10	%
Driver unit (240 Ohm) calibration resolution	Rres	—	—	—	10	Ω
Rkeep	Pad keeper resistance	—	20	—	50	kΩ

5.2.4 LPDDR2 mode

5.2.4.1 LPDDR2 mode DC electrical specifications

Table 15. LPDDR2 mode DC electrical specifications

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
High-level output voltage	Voh	Ioh = -100 µA	0.9*ovdd	—	—	V
Low-level output voltage	Vol	Iol = 100 µA	—	—	0.1*ovdd	V
Input reference voltage	Vref	—	0.49*ovdd	0.5*ovdd	0.51*ovdd	V
High-level DC input voltage	Vih (DC)	—	Vref + 0.17	—	ovdd	V
High-level DC input voltage	Vil (DC)	—	ovss	—	Vref - 0.17	V
Input current (no pullup/pulldown)[1]	Iin	Vi = ovdd or 0	—	—	5	µA
Pullup/pulldown impedance mismatch	MMpupd	34 Ohm full strength driver	-15	—	+15	%

Table continues on the next page...

Table 15. LPDDR2 mode DC electrical specifications (continued)

Parameter	Symbol	Test conditions	Min	Typ	Max	Unit
Driver 240 Ohm unit calibration resolution	Rres	—	—	—	10	Ω
Rkeep[2]	Pad keeper resistance	—	20	—	50	kΩ

1. Typ condition: typ model, 1.2 V, and 25 °C. Max condition: bcs model, 1.32 V, and -40 °C. Min condition: wcs model, 1.14 V, and 125 °C.
2. Typ condition: typ model, 1.2 V, and 25 °C, max condition: wcs model, 1.14 V, and 125 °C, min condition: bcs model, 1.32 V, and -40 °C.

6 Peripheral operating requirements and behaviors

6.1 Analog modules

6.1.1 ADC electrical specifications

The device provides a 12-bit Successive Approximation Register (SAR) Analog-to-Digital Converter.

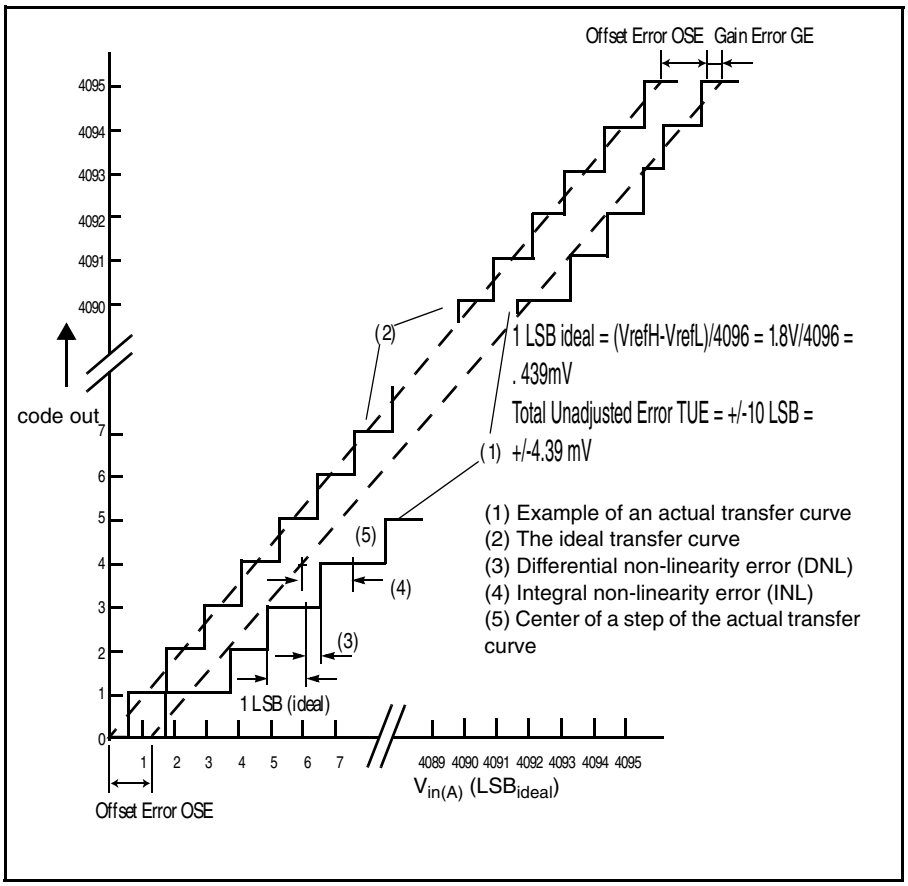

Figure 2. ADC characteristics and error definitions

NOTE

While measuring scaled supply voltages on ADC Channels, Maximum (+5/-10%) variation can be expected .

6.1.1.1 Input equivalent circuit

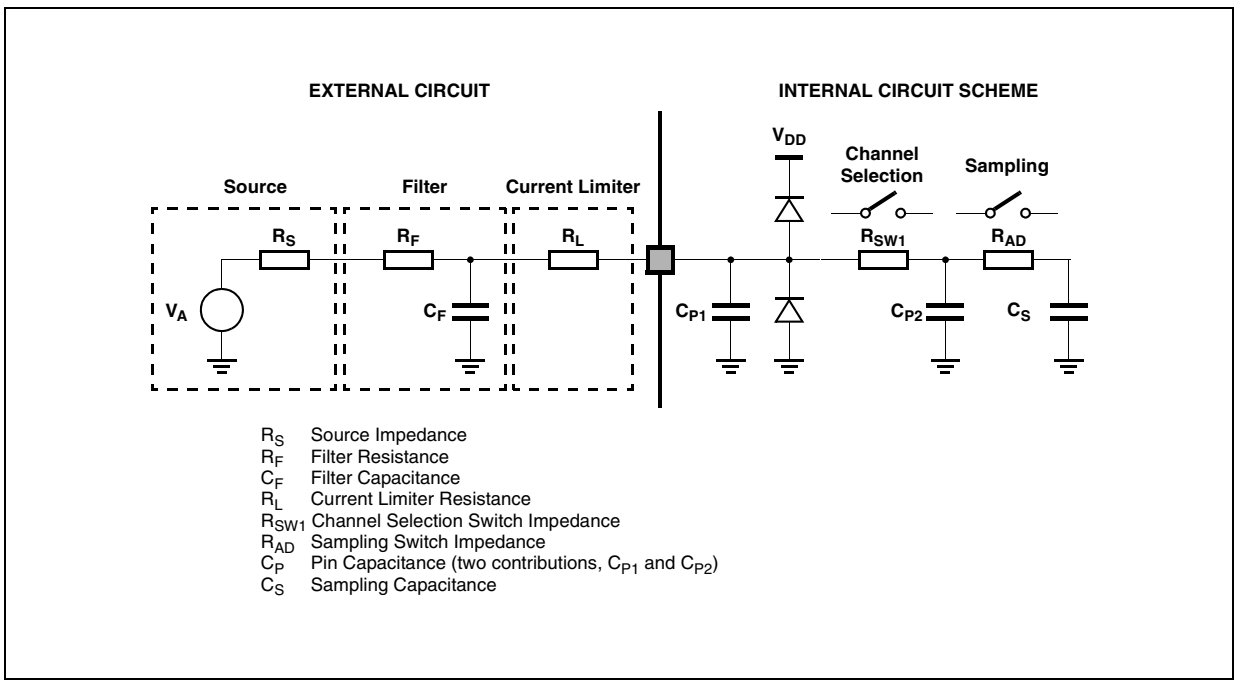

Figure 3. Input equivalent circuit

Table 16. ADC conversion characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{CK}	ADC Input Clock frequency (Bus clock)	—	20	—	80	MHz
f_{AD_clk}	ADC Conversion clock frequency[1]		20		40	MHz
f_s	Sampling frequency	—	—	—	0.5	MHz
t_{sample}	Sample time[2]		500	—	—	ns
t_{conv}	Conversion time[3]		1400	—	—	ns
C_S	ADC input sampling capacitance	—	—	—	5	pF
C_{P1}	ADC input pin capacitance 1	—	—	—	5	pF
C_{P2}	ADC input pin capacitance 2	—	—	—	0.8	pF
R_{SW1}	Internal resistance of analog source	—	—	—	875	Ω
R_{AD}	Internal resistance of analog source	—	—	—	825	Ω
INL[4]	Integral non linearity	—	–3	—	3	LSB
DNL	Differential non linearity	—	–2	—	2	LSB
OFS	Offset error	—	–6	—	6	LSB
GNE	Gain error	—	–6	—	6	LSB
Input (single ADC channel)	Max leakage	125C	—	—	2000	nA
TUE	Total unadjusted error	—	–8	—	8	LSB

1. Please see description of Clock & reset section in ADC chapter in Reference Manual for details. User need to generate AD_clk = 40 MHz for 0.5 MSPS operation. For example, if f_{ck} = 80 MHz, configure MCR[8].ADCLKSE = 0 and MCR[4].ADCLKDIV = 0 (default).
2. During the sample time the input capacitance CS can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_{sample}. After the end of the sample time t_{sample}, changes of the analog input voltage have no effect on the conversion result. Values for the sample clock t_{sample} depend on programming. For internal ADC channels, the minimum sampling time required is 3 microsecond.
3. This parameter does not include the sample time t_{sample}, but only the time for determining the digital result and the time to load the result register with the conversion result.
4. Specifications are quoted here for input signal ranging from 150 mV to VDD_HV_ADC - 150 mV. For signals outside this range, the Specifications may degrade beyond limits specified in this table.

6.1.2 Thermal Monitoring Unit (TMU)

The following table describes TMU electrical characteristics.

Table 17. TMU electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
T_j	Temperature monitoring range	—	-40	—	125	°C
T_{SENS}	Sensitivity	—	—	2.5	—	mV/°C
T_{ACC}	Accuracy	T_J = -40 °C to 40 °C	-10	—	+10	°C
		T_J = 40 °C to 125 °C	-6	—	+6	°C

6.2 Clocks and PLL interfaces modules

6.2.1 Main oscillator electrical characteristics

The device provides an oscillator/resonator driver of a Pierce-type structure.

Table 18. Main oscillator electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
$f_{FXOSCHS}$	Oscillator frequency	—	—	40.0	n/a	MHz
$T_{FXOSCHSSU}$	Oscillator start-up time	$f_{FXOSCHS}$ = 40 MHz	—	—	2[1]	ms
V_{IH}	Input high level CMOS Schmitt Trigger	Vref = 0.5*VDD_HV_OSC where VDD_HV_OSC is FXOSC HV Supply	Vref+0.5	—	VDD_HV_OSC	V
V_{IL}	Input low level CMOS Schmitt Trigger	Vref = 0.5*VDD_HV_OSC where VDD_HV_OSC is FXOSC HV Supply	0	—	Vref – 0.5	V

1. The start-up time is dependent upon crystal characteristics, board leakage, etc, high ESR and excessive capacitive loads can cause long start-up time

Following crystals are used in internal crystal oscillator validation:

- NX3225 – 40 MHz; Load capacitance = 8 pF
- NX5032 – 40 MHz; Load capacitance = 8 pF

6.2.2 48 MHz FIRC electrical characteristics

Table 19. FIRC electrical specifications

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
F_{Target}	FIRC target frequency (trimmed)	—	—	48	—	MHz
δF_{var_T}	FIRC frequency variation with respect to supply and temperature after process trimming	—	-10	—	+10	%

6.2.3 PLL electrical specifications

Table 20. PLL electrical characteristics [1]

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{PLLIN}	PLL input clock[2]	—	20[3]	—	40[3]	MHz
Δ_{PLLIN}	PLL input clock duty cycle [2]	—	40	—	60	%
$t_{PLLLOCK}$	PLL lock time	—	—	—	100	µs
Δ_{PLLT}	Period jitter	—	—	—	150	ps
Δ_{PLLTIE}	TIE	—	—	—	560	ps
f_{PLLMOD}	SSCG modulation frequency	—	—	—	32	kHz
δ_{PLLMOD}	SSCG modulation depth (Down Spread)	—	0.50	—	2.7[4]	%

1. The jitter values are gauranteed for following conditions:
    1. Measurement being done on LFAST TX pad with observed frequency greater than 250 M and less than 320 M
    2. Minimum SOC activity - Operations required to observe clock must be functional.
    3. Maximum frequency change in SSCG modulation is limited by following relation: Modulation Depth * VCO Frequency < PLL Reference (PFD) Frequency
2. PLL0IN clock retrieved from either internal RCOSC or external FXOSC clock. Input characteristics are granted when using internal RCOSC or external oscillator is used in functional mode.
3. The PLLIN clock is the frequency after the PREDIV(Pre-divider) value division, and before the Phase detector block. Please refer to the PLLs section of clocking chapter in the Reference Manual.

4. STEPSIZE x STEPNO < 18432

For the PLL frequencies supported by this device, refer to the Table - "PLL frequencies" in the "Clocking" chapter of the Reference Manual.

6.2.4 DFS electrical specifications

DFS takes input clock from PLL output. Here is relation between input and output clock of each phase divider:

F(dfsclkout) = F(dfsclkin)/[mfi+(mfn/256)]

mfi : integer part of division [1:255]

mfn: Fractional part of division [1:255]

Table 21. DFS electrical specification[1]

Parameter	Min	Typical	Max	Unit
Input Frequency	800	—	1066	MHz
Period jitter	—	—	300	ps
TIE	—	—	600	ps

1. DFSes mfi, mfn and frequencies are defined and restricted as per Reference Manual. See the table "DFS (mfi, mfn) settings" in the "Clocking" chapter of the Reference Manual for the supported mfi and mfn combinations.

6.2.5 LFAST PLL Electrical Specifications

The following table lists AC specification of the LFAST PLL block.

Table 22. LFAST PLL Interface AC Specifications

Parameter	Min	Typical	Max	Unit
PLL input clock	10	—	26	MHz
PLL VCO Frequency	312	—	320	MHz
Phase Lock time	—	—	50	µs
RMS Period Jitter	—	—	40[1]	ps
Long Term Jitter[2] Random Jitter	—	84	—	ps
Deterministic Jitter	—	80	—	ps
Total Jitter @ BER 10^{-9}	—	1.09	1.31[3]	ns

1. When SysClk = 26 MHz
2. VCO clock measured over 100 µs acquisition at ZipWire TX LVDS across 100 ohm load
3. Only Total Jitter is given a maximum specification as variation of Random and Deterministic jitter is not critical. Any combined Random and Deterministic jitter yielding a Total Jitter @ 10^{-9} BER is within maximum specification and is acceptable

6.3 Memory interfaces

6.3.1 QuadSPI AC specifications

- Measurements are with a load of 35 pF on output pins. Input slew: 1 ns, DSE[2:0] = 111, and FSEL[1:0] = 11
- QuadSPI input timing is with 15 pF load on flash output.
- QuadSPI_MCR[DQS_EN] must be set as 1 for SDR READ

The following table lists various QuadSPI modes and their corresponding configurations. Please refer to the device Reference Manual for register and bit descriptions.

Table 23. QuadSPI read/write settings

Modes supported by QuadSPI		QuadSPI_MCR[DDR_EN]	QuadSPI_MCR[DQS_EN]	QuadSPI_MCR [DQS_CD]	QuadSPI_MCR [REFCLK_SEL]	QuadSPI_MCR [DQS_MDSL]	QuadSPI_SOCCR [FDCC_FB]	QuadSPI_SOCCR [FDCC_FA]	QuadSPI_FLSHCR[TDH]
SDR mode	Internal DQS mode	0	1	000	1	1	39h @ 3.3 V 3Fh @ 1.8 V	39h @ 3.3 V 3Fh @ 1.8 V	00
DDR mode	Internal DQS mode	1	1	000	0	1	4Ah @ 3.3 V 50h @ 1.8 V	4Ah @ 3.3 V 50h @ 1.8 V	01
	External DQS mode (supported by HyperFlash)	1	1	000	0	0	00h	00h	01

SDR mode

For SDR mode, QuadSPI_MCR[DQS_EN] must be set as '1'.