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FSA2466 DATA / AUDIO Low-Voltage Dual DPDT Analog Switch

Features

Switch Type	DPDT (2x)
Input Type	Data / Audio Switch
Input Signal Range	0 to V _{CC}
V _{CC}	1.65 to 4.45 V
R _{ON}	2.5 Ω at 2.7 V
R _{FLAT}	0.8 Ω at 2.7 V
ESD	8 kV HBM
Bandwidth	245 MHz
C _{ON} at 240MHz	16 pF
C _{OFF} at 240MHz	6.0 pF
Features	Low I _{CCT}
Package	16- Lead UMLP 1.80 x 2.60 x 0.55 mm, 0.40 mm pitch
Top Mark	KA
Ordering Information	FSA2466UMX

Description

The FSA2466 is a dual Double-Pole, Double-Throw (DPDT) analog switch. The FSA2466 operates from a single 1.65 V to 4.45 V supply and features an ultra-low on resistance of 2 Ω at a +2.7 V supply and T_A=25°C. This device is fabricated with sub-micron CMOS technology to achieve fast switching speeds and is designed for break-before-make operation.

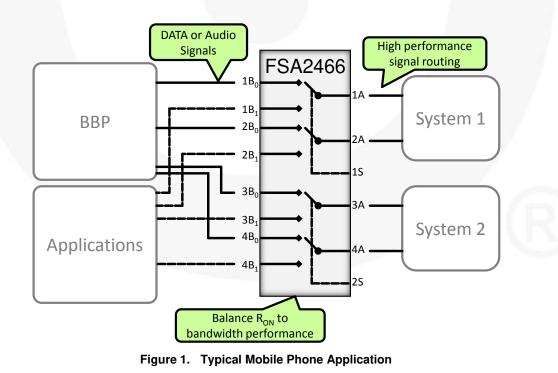
FSA2466 features very low quiescent current even when the control voltage is lower than the V_{CC} supply. This allows mobile handset applications direct interface with the baseband processor general-purpose I/Os.

Related Resources

- For samples and questions, please contact: <u>Analog.Switch@fairchildsemi.com</u>.
- FSA2466 Evaluation Board

Applications

- MP3 Portable Media Players
- Cellular Phones, Smartphones



		<pre>ibility of the second sec</pre>		
otions			_	
ne	Туре	Description		
B ₀	I/O	Data / Audio Port		
S	Input	Control Input for Data & Common Ports 1 & 2		1E 1E
B ₁	I/O	Data / Audio Port		
4	I/O	Data / Audio Common Port		
)	1/0	Data / Audia Bart		

1**A**

16

1B₁

15

4B₀

13

 \mathbf{v}_{cc}

14

Pin Descriptions

Pin Configuration

Pin #	Name	Туре	Description					
1	1B ₀	I/O	Data / Audio Port					
0	\$	lanut	Output langet for Data & Output Data 1 & O		$1B_0 = 1A \& 2B_0 = 2A$			
2	1S	Input	Control Input for Data & Common Ports 1 & 2	1	1B ₁ = 1A & 2B ₁ = 2A			
3	2B ₁	I/O	Data / Audio Port	Data / Audio Port				
4	2A	I/O	Data / Audio Common Port					
5	2B ₀	I/O	Data / Audio Port					
6	GND	GND						
7	3B1	I/O	Data / Audio Port					
8	ЗA	I/O	Data / Audio Common Port		(D)			
9	3B0	I/O	Data / Audio Port					
10	2S	Input	Control Input for Data & Common Ports 3 & 4	0	$3B_0 = 3A \& 4B_0 = 4A$			
10	20	input	Control input for Data & Common Ports 3 & 4	1	$3B_1 = 3A \& 4B_1 = 4A$			
11	4B1	I/O	Data / Audio Port					
12	4A	I/O	Data / Audio Common Port					
13	4B ₀	I/O	Data / Audio Port	Data / Audio Port				
14	V _{CC}	Supply	Voltage supply	Voltage supply				
15	1B1	I/O	Data / Audio Port					
16	1A	I/O	Data / Audio Common Port					

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit	
V _{CC}	Supply Voltage		-0.50	5.25	V	
Vs	Switch Voltage		-0.5	V _{CC} +0.3	V	
V _{IN}	Input Voltage		-0.5	5.0	V	
I _{IK}	Input Diode Current		-50		mA	
I _{SW}	Switch Current		1	350	mA	
I _{SWPEAK}	Peak Switch Current (Pulsed at 1ms Duration	n, <10% Duty Cycle)		500	mA	
T _{STG}	Storage Temperature Range		-65	+150	°C	
TJ	Junction Temperature			+150	°C	
TL	Lead Temperature, Soldering 10 Seconds			+260	°C	
		I/O to GND		8		
ESD	Human Body Model, JESD22-A114	Power to GND		8	kV	
EOD		All Other Pins		8	ĸv	
	Charge Device Model, JEDEC: JESD22-C101			2		

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
Vcc	Supply Voltage ⁽¹⁾	1.65	4.45	V
V _{IN}	Control Input Voltage ⁽²⁾	0	V _{CC}	V
Vs	Switch Input Voltage	0	V _{CC}	V
T _A	Operating Temperature	-40	+85	°C

Note:

1. For 4.45 V operation, SEL frequency (pins 1S & 2S) should not exceed 100Hz and 100ns edge rate.

2. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Typical values are at TA=25°C unless otherwise specified.

Symbol	Parameter	Condition	Condition V _{cc} (V)		T _A =+25°C			T _A =-40 to +85⁰C				
• • • • • • •				Min.	Тур.	Max.	Min	Max.	Unit			
			4.30				1.4					
M	lanut Valtaga Lligh		2.70 to 3.60				1.3		V			
VIH	Input Voltage High		2.30 to 2.70				1.1		V			
			1.65 to 1.95				0.9					
			4.30					0.7				
N/	land Maltana Land		2.70 to 3.60					0.5				
VIL	Input Voltage Low		2.30 to 2.70		0.4		V					
	1		1.65 to 1.95					0.4				
I _{IN}	Control Input Leakage	$V_{IN}=0$ V to V_{CC}	1.65 to 4.30				-0.5	0.5	μA			
		nA=0.3 V, V _{CC} -0.3 V										
	Dff Leakage Current of Port nB_0 and nB_1	nB_0 or $nB_1=0.3$ V, V_{CC} -0.3 V or Floating	1.95 to 4.30	-10		10	-50	50	nA			
		nA=0.3 V, V _{CC} -0.3V										
I _{A(ON)}	On Leakage Current of Port A				$nB_0 \text{ or } nB_1=0.3 \text{ V}, V_{CC}$ -0.3 V or Floating	1.95 to 4.30	-10		10	-50	50	nA
		I _{OUT} =100 mA	4.30		1.6			2.0				
		I _{OUT} =100 mA, nB ₀	2.70		2.0			2.5				
R _{ON}	Switch On Resistance ⁽³⁾	or nB ₁ =0 V, 0.7 V, 1.2 V, V _{CC}	2.30		2.2			2.7	Ω			
		I_{OUT} =100mA, nB ₀ or nB ₁ =0.7 V	1.80		4.3			6.0				
	On Resistance Matching	I_{OUT} =100 mA, nB ₀ or nB ₁ =0.8 V	2.70		0.04			0.20				
ΔR_{ON}	Between Channels ⁽⁴⁾	I_{OUT} =100 mA, nB ₀ or nB ₁ =0.7 V	2.30	20	0.03			0.30	Ω			
Р	On Desistance Flater (5)	I _{OUT} =100 mA, nB ₀	2.70		0.60			0.8				
$R_{FLAT(ON)}$	On Resistance Flatness ⁽⁵⁾	or $nB_1 = 0V \rightarrow V_{CC}$	2.30		0.75			0.9	Ω			
Icc	Quiescent Supply Current	V_{IN} =0 V to V _{CC} , I _{OUT} =0 V	4.30	-100		100	-500	500	nA			
	Increase in I _{cc} Current	V _{IN} =1.8 V	4.30		7	12		15				
I _{CCT}	per Control Voltage	V _{IN} =2.6 V	4.30		3	6		7	μA			

Notes:

3. On resistance is determined by the voltage drop between the A and B pins at the indicated current through the switch.

4. $\Delta R_{ON} = R_{ON max} - R_{ON min}$ measured at identical V_{CC}, temperature, and voltage.

5. Flatness is defined as the difference between the maximum and minimum value of on resistance over the specified range of conditions.

AC Electrical Characteristics

Typical values are at $T_A=25^{\circ}C$ unless otherwise specified.

Symbol	Deveneter	Condition	N	Т	=+25º	² C	T _A =-40	to +85ºC	11	Figure
Symbol	Parameter	Condition	V _{cc}	Min.	Тур.	Max.	Min.	Max.	Unit	Figure
			3.6 to 4.3			50		60		
ton	Turn-On Time	nB ₀ or nB ₁ =1.5 V R _L =50 Ω, C _L =35 pF	2.7 to 3.6			65		75	ns	Figure 3
		112-00 12, OL-00 pi	2.3 to 2.7			80		90		
			3.6 to 4.3			32		40		
t _{OFF}	Turn-Off Time	nB ₀ or nB ₁ =1.5 V R _L =50 Ω, C _L =35 pF	2.7 to 3.6			42		50	ns	Figure 3
		112-00 <u>12</u> , 02-00 pi	2.3 to 2.7			52	1	60		
			3.6 to 4.3		15				2	
t _{BBM}	Break-Before- Make Time ⁽⁶⁾	nB ₀ or nB ₁ =1.5 V R _L =50 Ω, C _L =35 pF	2.7 to 3.6		15				ns	Figure 4
	Marto Timo	112-00 12, OL-00 pi	2.3 to 2.7		15					
		$C_L=100 \text{ pF},$ $V_{GEN}=0 \text{ V}, \text{ R}_{GEN}=0 \Omega$	3.6 to 4.3		8					
Q	Charge Injection		2.7 to 3.6		6				pC	Figure 6
			2.3 to 2.7		3			V		
			3.6 to 4.3		-90					Figure 5
OIRR	Off Isolation	f=100 KHz, R _L =50 Ω, C _L =5 pF	2.7 to 3.6		-90				dB	
		0L=3 pi	2.3 to 2.7		-90					
			3.6 to 4.3		-90					
Xtalk	Crosstalk	f=100 KHz, R _L =50 Ω, C _L =5 pF	2.7 to 3.6		-90				dB	Figure 5
		OL=5 pr	2.3 to 2.7		-90					1.
BW	-3dB Bandwidth	R _L =50 Ω	2.3 to 4.3		245				MHZ	Figure 8
			3.6 to 4.3		0.21		1			
		$R_{L}=32 \Omega, V_{IN}=2V_{PP},$	2.7 to 3.6		0.17					
	Total Harmonic	f=20 to 20 kHZ	2.3. to 2.7		0.26					
THD	Distortion	R _L =600 Ω,	3.6 to 4.3		0.01				%	Figure 9
		V _{IN} =2 V _{PP} ,	2.7 to 3.6		0.008					
		f=20 to 20 kHZ	2.3. to 2.7		0.012					

Note:

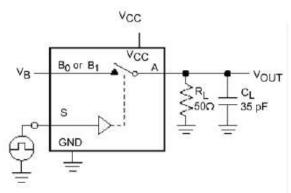
6. Guaranteed by characterization, not production tested.

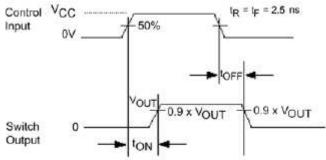
Capacitance

Symbol	Parameter	Condition	V _{cc}	T _A =+25⁰C Typical	Unit	Figure
C _{IN}	Control Pin Input Capacitance	f=1 MHz	0	1.3	pF	Figure 3
<u> </u>	D. Dart Off Canaditanaa	f=1 MHz	3.3	6.0	ъГ	Figure 0
COFF	B Port Off Capacitance	f=240 MHz	3.3	6.0	pF	Figure 3
<u> </u>	A Dart On Canaditanaa	f=1 MHz	3.3	21.0	ъ Г	
CON	A Port On Capacitance	f=240 MHz	3.3	16.0	рF	Figure 3

FSA2466 – DATA / AUDIO Low-Voltage Dual DPDT Analog Switch

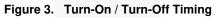
AC Loadings and Waveforms

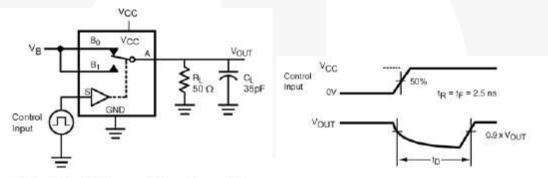




Logic Input Waveforms Inverted for Switches that have the Opposite Logic Sense

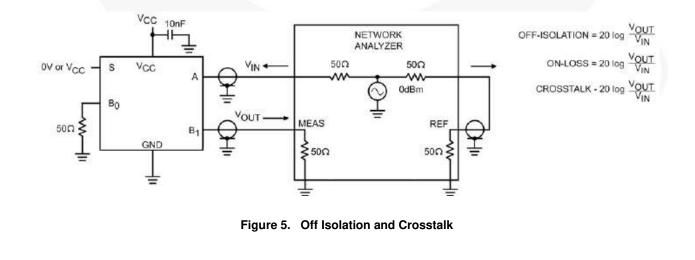
CL includes Fixture and Stray Capacitance





CL Includes Fixture and Stray Capacitance





AC Loadings and Waveforms (Continued) ΔVOUT Vcc VOUT RGEN A Vour Bo or Ba CL IN VGE OFF OFF ON GND Control ON OFF OFF Input IN $Q = (\Delta V_{OUT})(C_L)$ Figure 6. **Charge Injection** V-10nF S 0V or CAPACITANCI Vcc METER BO or B f = 1MHz GND Figure 7. On / Off Capacitance Measurement Setup 10:1 Signal Generato OdBm Ver BN Analyz ş 50Ω ogic Input OV OF VCC Figure 8. Bandwidth 100 VIN Bω Analyzer Signal Generato Logic Input -OV or V_{CC} Figure 9. **Harmonic Distortion** © 2010 Fairchild Semiconductor Corporation

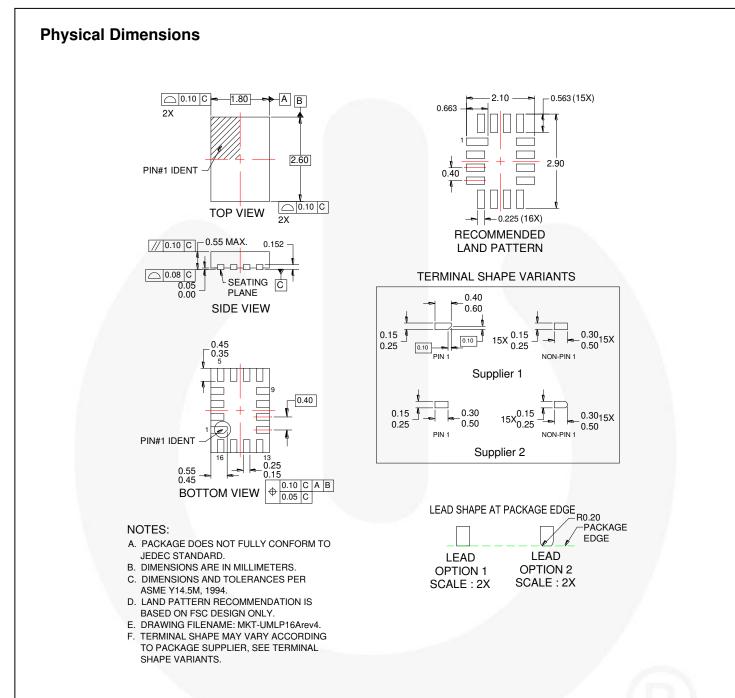


Figure 10. 16-Pin Ultrathin Molded Leadless Package (UMLP)

Order Number	Operating Temperature Range	Package Description	Packing Method
FSA2466UMX	-40 to 85°C	16-Terminal Ultrathin Molded Leadless Package	Tape & Reel

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