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Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832

Email & Skype: info@chipsmall.com Web: www.chipsmall.com

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FSA2866

Dual-Host / Dual-SIM Card Crosspoint Analog Switch

Features

Switch Type	2x2 Crosspoint Switch
Input Type	Data
Input Signal Range	0 to V _{CC}
V _{CC}	1.65V to 4.30V
R _{ON}	Data 2Ω (Typical) VSIM 2Ω (Typical)
R _{FLAT}	0.6Ω (Typical)
ESD	IEC 61000-4-2 System Air 15kV, Contact 8kV
C _{ON}	28pF (Typical)
C _{OFF}	12pF (Typical)
Package	20-Lead UMLP, 3 x 3 x 0.55mm, 0.40mm Pitch with Exposed DAP
Ordering Information	FSA2866UMX

Description

The FSA2866 is a dual-host, dual-SIM card analog switch designed specifically for cell phones that support two specific carrier services (for example, CDMA and GSM/3G).

Related Resources

- For samples and questions, please contact: Analog.Switch@fairchildsemi.com.
- FSA2866 Evaluation Board

Applications

- MP3 Portable Media Players
- Cellular Phones, Smart Phones

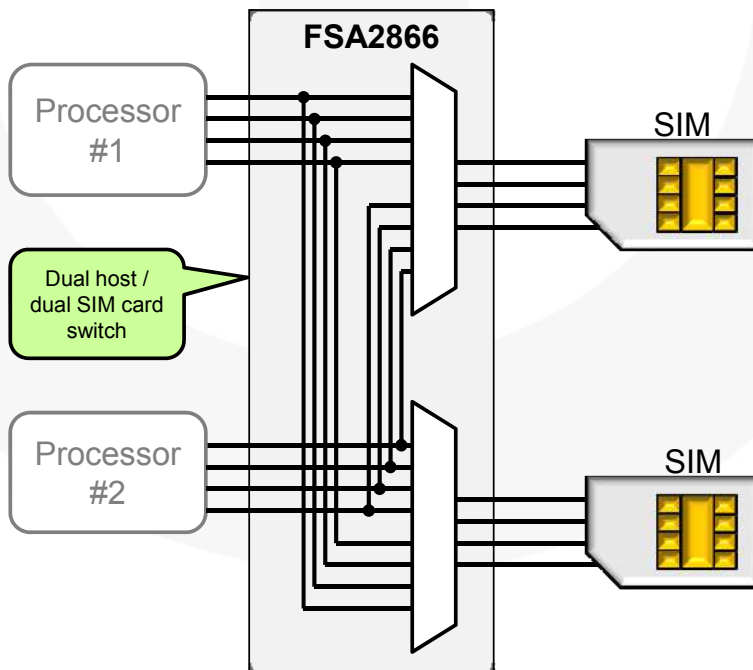


Figure 1. Typical Mobile Phone Application

Pin Descriptions

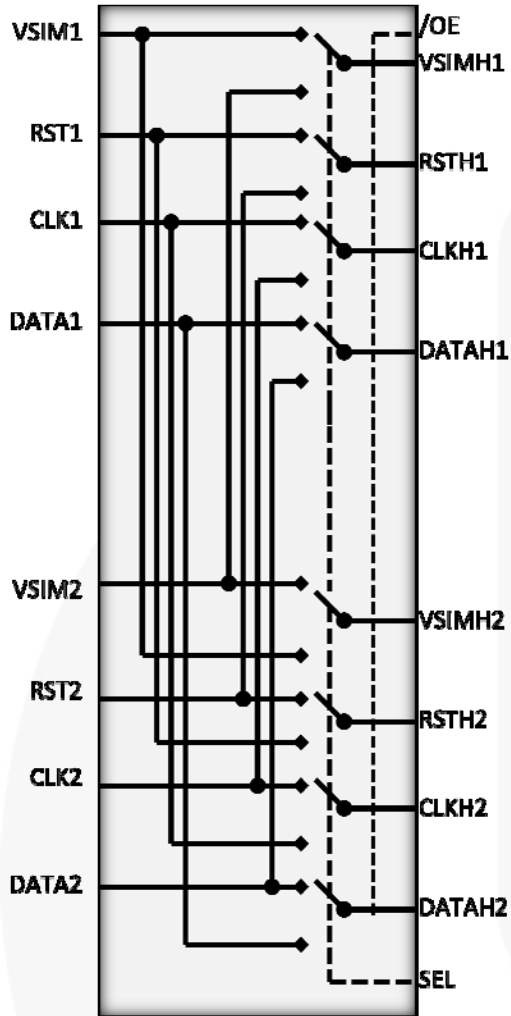


Figure 2. Functional Diagram

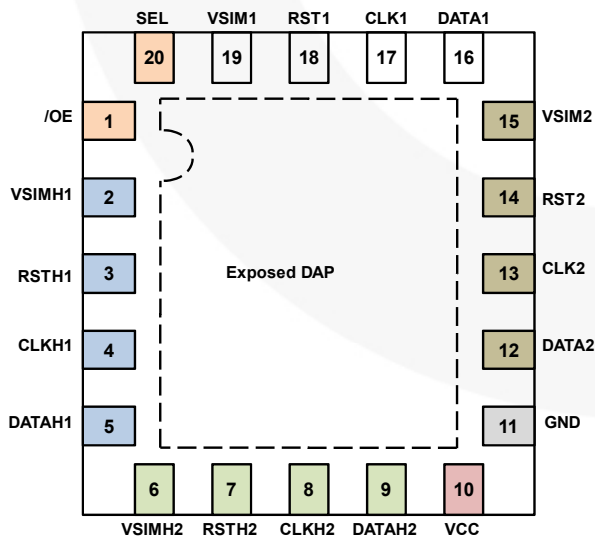


Figure 3. Pin Assignments (Top Through View)

Pin #	Name	Type	Description		
1	/OE	Input	Output Enable	0	Active
				1	Switch Disabled
2	VSIMH1	I/O	Common Ports for Host #1		
3	RSTH1	I/O			
4	CLKH1	I/O			
5	DATAH1	I/O			
6	VSIMH2	I/O	Common Ports for Host #2		
7	RSTH2	I/O			
8	CLKH2	I/O			
9	DATAH2	I/O			
10	VCC	Supply	Power		
11	GND	Ground	Ground		
12	DATA2	I/O	SIM Card Ports for Card #2		
13	CLK2	I/O			
14	RST2	I/O			
15	VSIM2	I/O			
16	DATA1	I/O	SIM Card Ports for Card #1		
17	CLK1	I/O			
18	RST1	I/O			
19	VSIM1	I/O			
20	SEL	Input	Control Pin	SEL=0	Host #1 connected to Card #1 [VSIMH1=VSIM1; DATAH1=DATA1; CLKH1=CLK1; RSTH1=RST1]
				SEL=1	Host #2 connected to Card #2 [VSIMH2=VSIM2; DATAH2=DATA2; CLKH2=CLK2; RSTH2=RST2]
					Host #1 connected to Card #2 [VSIMH1=VSIM2; DATAH1=DATA2; CLKH1=CLK1; RSTH1=RST1]
					Host #2 connected to Card #1 [VSIMH2=VSIM1; DATAH2=DATA1; CLKH2=CLK1; RSTH2=RST1]
DAP	DAP	N/C	Exposed die attach paddle (DAP) not electrically connected to any pin.		

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	-0.50	+5.5	V
V_{CNTRL}	DC Input Voltage (SEL,/OE)	-0.5	V_{CC}	V
V_{SW}	DC Switch I/O Voltage - DATAHn, CLKHn, CLKn, RSTHn, RSTn	-0.5	$V_{CC} + 0.3$	V
I_{IK}	DC Input Diode Current	-50		mA
I_{SIM}	DC Output Current – VSIMHn, VSIMn		100	mA
I_{OUT}	DC Output Current – DATAHn, CLKHn, CLKn, RSTHn, RSTn		35	mA
T_{STG}	Storage Temperature	-65	+150	°C
ESD	Human Body Model, JEDEC: JESD22-A114	All Pins	8	kV
		I/O to GND, Card Side Pins	16	
		Power to GND	9	
	Charged Device Model, JEDEC: JESD22-C101		2	
	IEC 61000-4-2 System-Level	Contact	8	
		Air Gap	15	

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding these ratings or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	1.65		4.3	V
V_{CNTRL}	Control Input Voltage (SEL, /OE)	0		V_{CC}	V
V_{SW}	Switch I/O Voltage - DATAHn, CLKHn, CLKn, RSTHn, RSTn	0		V_{CC}	V
I_{SIM}	DC Output Current – VSIMHn, VSIMn			30	mA
I_{OUT}	DC Output Current – DATAHn, CLKHn, CLKn, RSTHn, RSTn			10	mA
T_A	Operating Temperature	-40		+85	°C

DC Electrical Characteristics

$T_A=25^{\circ}\text{C}$ and $V_{CC}=3.0\text{V}$ unless otherwise noted.

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A=-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$			Unit
				Min.	Ty p.	Max.	
V_{IK}	Clamp Diode Voltage	$I_{IN}=-18\text{mA}$	2.7			-1.2	V
V_{IH}	Input Voltage High		1.65 to 2.30	1.1			V
			2.7 to 3.6	1.3			
			4.3	1.7			
V_{IL}	Input Voltage Low		1.65 to 2.30			0.4	V
			2.7 to 3.6			0.5	
			4.3			0.7	
I_{IN}	Control Input Leakage (SEL,/OE)	$V_{SW}=0$ to V_{CC}	4.3	-1		1	μA
$I_{NO(OFF)}$ $I_{NC(OFF)}$	Off Leakage Current of Ports RSTn, DATAn, CLKn, VSIMn	$V_{SIMHn}=DATAHn=CLKHn=RSTHn=0.3\text{V}$, $V_{CC}=0.3\text{V}$; RSTn, CLKn, DATAn, or $V_{SIMn}=V_{CC}-0.3\text{V}$, 0.3V , or Floating	4.3	-100		100	nA
$I_{A(ON)}$	On Leakage Current of Common Ports – RSTHn, DATAHn, CLKHn, VSIMHn	Common= 0.3V , $V_{CC}=0.3\text{V}$; $V_{SIMHn}=DATAHn=CLKHn=RSTHn=V_{CC}-0.3\text{V}$, 0.3V , or Floating	4.3	-100		100	nA
I_{OFF}	Power-Off Leakage Current	V_{SIMHn} or $DATAn$ or $CLKHn$ or $RSTHn$ $V_{IN}=0\text{V}$ to 4.3V , $V_{CC}=0\text{V}$	0	-2		2	μA
I_{OZ}	Off-State Leakage	V_{SIMHn} or $DATAn$ or $CLKHn$ or $RSTHn$ $V_{IN}=0.3\text{V}$ to 4.3V , $/OE=V_{CC}$	4.3	-5		5	μA
R_{ON_DATA}	Switch On Resistance for Data Paths	$I_{ON}=-20\text{mA}$; $/OE=0\text{V}$; $SEL=V_{CC}$ or 0V ; RSTn, CLKn, DATAn, or $V_{SIMn}=0$ or 2.7V	2.7		2.0	3.5	Ω
R_{ON_VSIM}	Switch On Resistance for VSIM Paths	$I_{ON}=-50\text{mA}$; $/OE=0\text{V}$; $SEL=V_{CC}$ or 0V ; RSTn, CLKn, DATAn, or $V_{SIMn}=0$ or 2.7V	2.7		2.0	3.5	Ω
ΔR_{ON_DATA}	On Resistance Matching Between Data Channels	$I_{ON}=-20\text{mA}$; $/OE=0\text{V}$; $SEL=V_{CC}$ or 0V ; RSTn, CLKn, or $DATAn=0\text{V}$	2.7		0.10	0.25	Ω
R_{ON_FLAT}	On Resistance Flatness Data Path Signals	$I_{ON}=-20\text{mA}$, $/OE=0\text{V}$, $SEL=V_{CC}$ or 0V , RSTn, CLKn or $DATAn=0$ to V_{CC}	2.7		0.6	0.8	Ω
I_{CC}	Quiescent Supply Current	$V_{IN}=0$ or V_{CC} , $I_{OUT}=0$	4.3			1	μA
I_{CCT}	Increase in I_{CC} Current Per Control Voltage and V_{CC}	$V_{IN}=1.65\text{V}$, $V_{CC}=4.3\text{V}$	4.3		7	9.5	μA

Notes:

1. Guaranteed by characterization; not production tested.
2. On resistance is determined by the voltage drop between the D+/D- and D+/R, D-/L pins at the indicated current through the switch.
3. $\Delta R_{ON}=R_{ON_max} - R_{ON_min}$ measured at identical V_{CC} , temperature, and voltage.

AC Electrical Characteristics

$T_A=25^{\circ}\text{C}$ and $V_{CC}=3.0\text{V}$ unless otherwise noted.

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A=-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$			Unit
				Min.	Typ.	Max.	
t_{ON}	Turn-On Time, /OE to Output	$R_L=50\Omega$, $C_L=30\text{pF}$, $V_{SW}=0.8\text{V}$ Figure 4	2.8 to 4.3		55	75	ns
			1.8			110	
t_{OFF}	Turn-Off Time, /OE to Output	$R_L=50\Omega$, $C_L=30\text{pF}$, $V_{SW}=0.8\text{V}$ Figure 4	2.8 to 4.3		24	75	ns
			1.8			110	
t_{BBM}	Break-Before-Make Time	$R_L=50\Omega$, $C_L=30\text{pF}$, $V_{SW}=0.8\text{V}$ Figure 5		2	35		ns
O_{IRR}	Off Isolation	$R_L=50\Omega$, $f=100\text{KHz}$, /OE= V_{CC} , $V_{SW}=13\text{dBm}$ ($3V_{pp}$) Figure 6	1.8 to 4.3		90		dB
X_{TALK}	Crosstalk	$R_L=50\Omega$, $f=100\text{KHz}$, $V_{SW}=13\text{dBm}$ ($3V_{pp}$) Figure 6	1.8 to 4.3		85		dB
BW	-3db Bandwidth	$R_L=50\Omega$, $C_L=0\text{pF}$, Figure 8	3.0		210		MHz
		$R_L=50\Omega$, $C_L=5\text{pF}$, Figure 8			198		
		$R_L=50\Omega$, $C_L=30\text{pF}$, Figure 8			120		
		$R_L=50\Omega$, $C_L=50\text{pF}$, Figure 8			78		

Note:

- Guaranteed by characterization; not production tested.

Capacitance

$T_A=25^{\circ}\text{C}$ unless otherwise noted.

Symbol	Parameter	Conditions	$T_A=-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$			Unit
			Min.	Typ.	Max.	
C_{IN}	Control Pin Input Capacitance	$V_{CC}=0\text{V}$, $f=1\text{MHz}$		2		pF
C_{ON}	On Capacitance	$V_{CC}=3.3\text{V}$, /OE=0V, $f=1\text{MHz}$, Figure 7		28		pF
C_{OFF}	Off Capacitance	V_{CC} and /OE=3.3V, $f=1\text{MHz}$, Figure 7		12		pF

AC Loadings and Waveforms

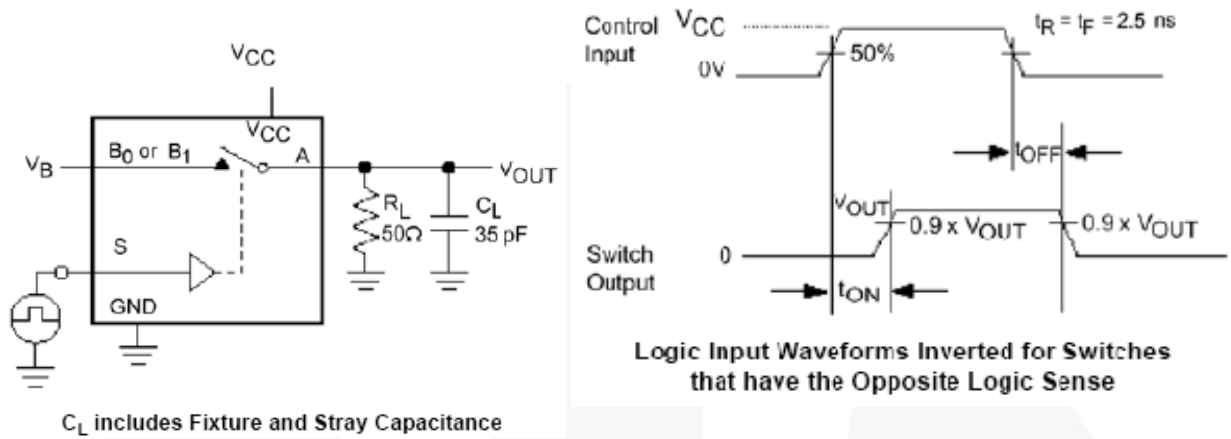


Figure 4. Turn-On / Turn-Off Timing

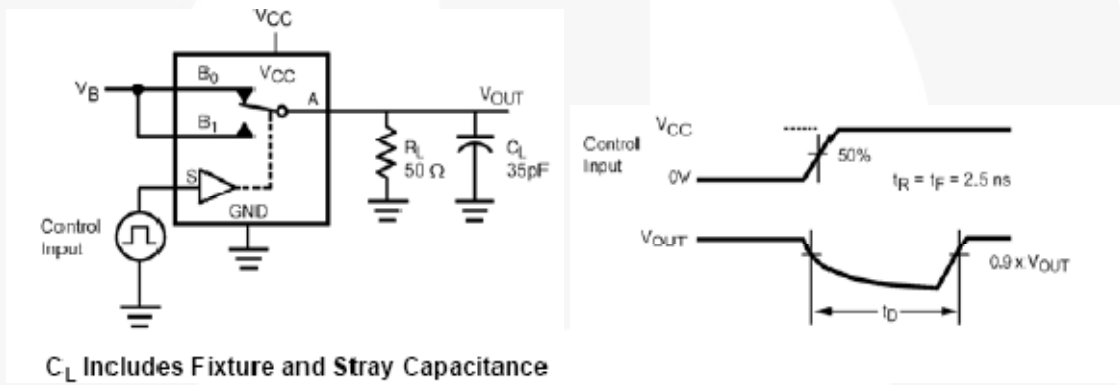


Figure 5. Break-Before-Make Timing

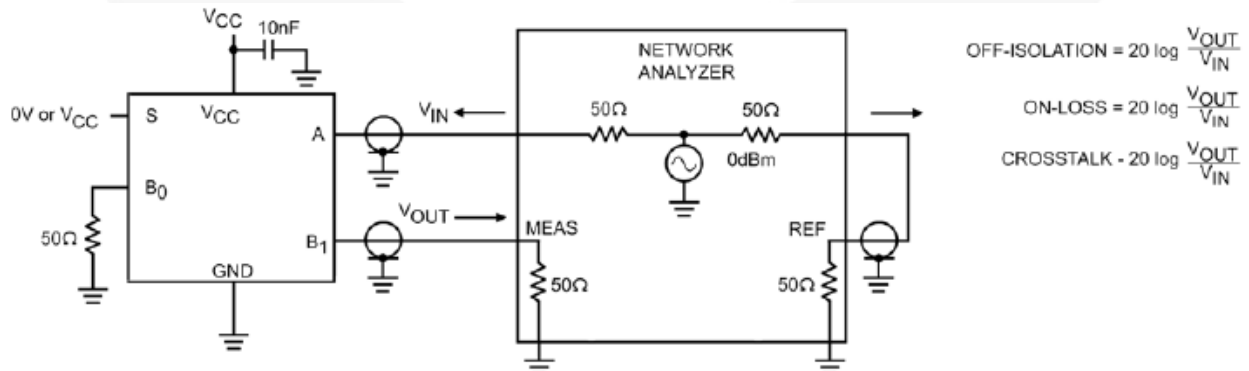


Figure 6. Off Isolation and Crosstalk

AC Loadings and Waveforms (Continued)

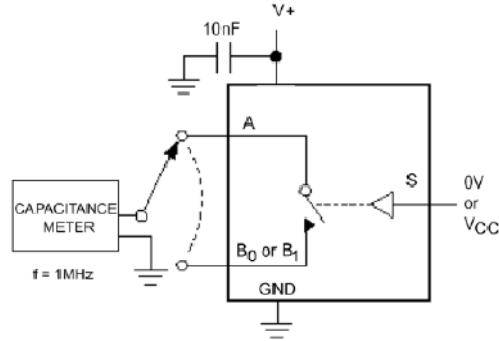


Figure 7. On / Off Capacitance Measurement Setup

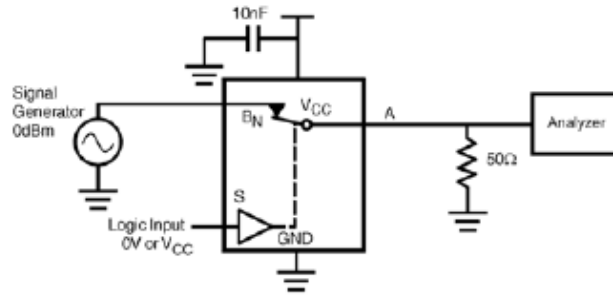
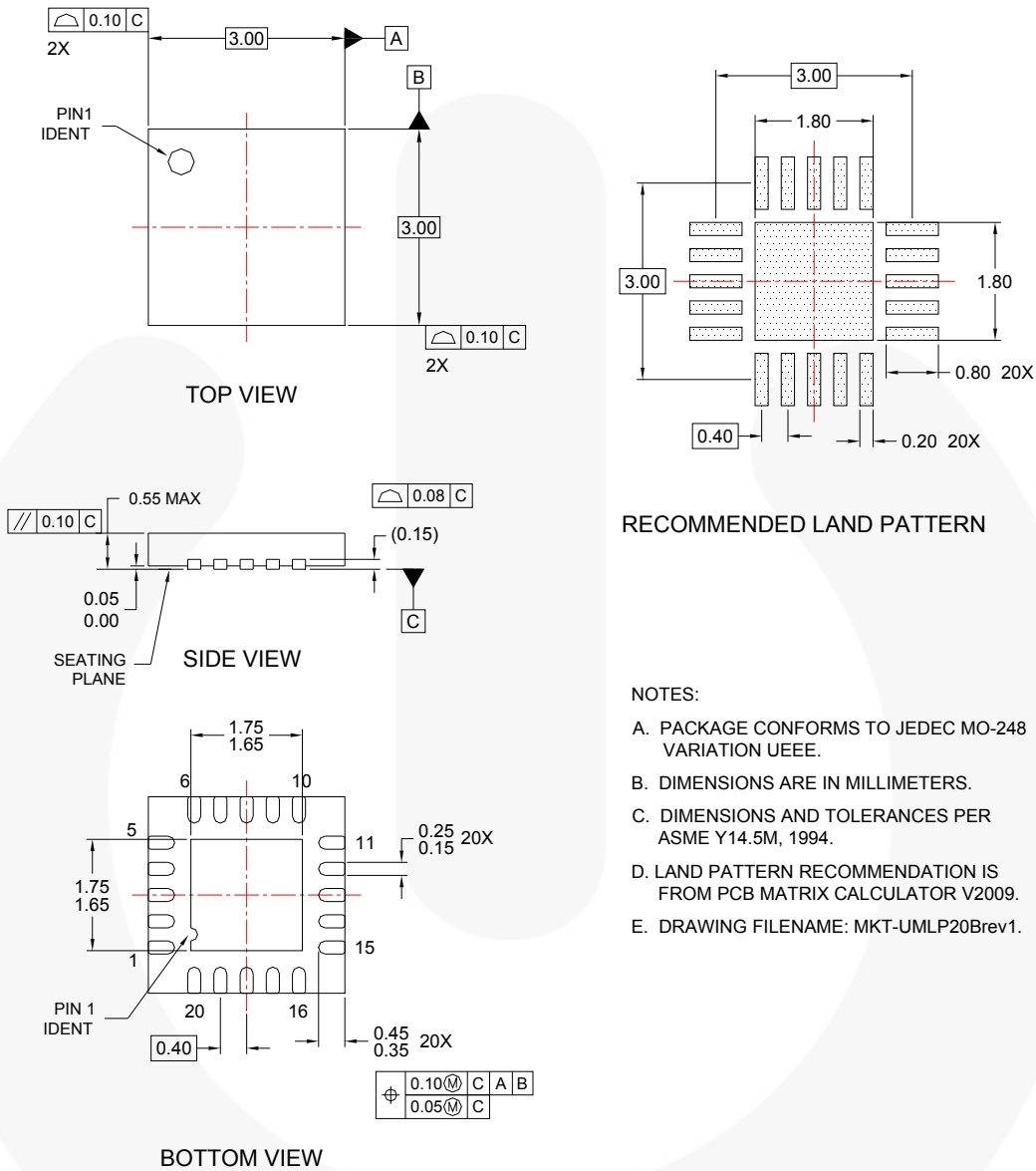


Figure 8. Bandwidth



Physical Dimensions



RECOMMENDED LAND PATTERN

- NOTES:
- A. PACKAGE CONFORMS TO JEDEC MO-248 VARIATION UEEE.
 - B. DIMENSIONS ARE IN MILLIMETERS.
 - C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
 - D. LAND PATTERN RECOMMENDATION IS FROM PCB MATRIX CALCULATOR V2009.
 - E. DRAWING FILENAME: MKT-UMLP20Brev1.

Figure 9. 20-Pin Ultrathin Molded Leadless Package (UMLP)

Order Number	Operating Temperature Range	Package Description	Packing Method
FSA2866UMX	-40 to 85°C	20-Lead Ultrathin Molded Leadless Package (UMLP)	Tape & Reel





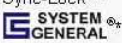
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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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