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FAIRCHILD SEMICONDUCTOR®

December 2013

FSA3157B
Low-Voltage SPDT Analog Switch or 2:1 Multiplexer / De-multiplexer Bus Switch

Features

- Useful in Both Analog and Digital Applications
- Ultra-Small, MicroPak™ Leadless Package
- Low On Resistance: <10 Ω Typical at 3.3 V V_{CC}
- Broad V_{CC} Operating Range: 1.65 V to 5.5 V
- Rail-to-Rail Signal Handling
- Power-Down, High-Impedance Control Input
- Over-Voltage Tolerance of Control Input to 7.0 V
- Break-Before-Make Enable Circuitry
- 250 MHz, 3 dB Bandwidth

Description

The FSA3157B is a high-performance, Single-Pole / Double-Throw (SPDT) analog switch or 2:1 multiplexer / de-multiplexer bus switch.

The device is fabricated with advanced sub-micron CMOS technology to achieve high-speed enable and disable times and low on resistance. The break-before-make select circuitry prevents disruption of signals on the B Port due to both switches temporarily being enabled during select pin switching. The device is specified to operate over the 1.65 to 5.5 V V_{CC} operating range. The control input tolerates voltages up to 5.5 V, independent of the V_{CC} operating range.

Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package	Packing Method
FSA3157BL6X	-40 to +85°C	7G	6-Lead, MicroPak™ 1.0 mm Wide Package	5000 Units on Tape and Reel
FSA3157BFHX	-40 to +85°C	7G	6-Lead, MicroPak2™, 1x1 mm Body, .35 mm Pitch	5000 Units on Tape and Reel

Analog Symbols

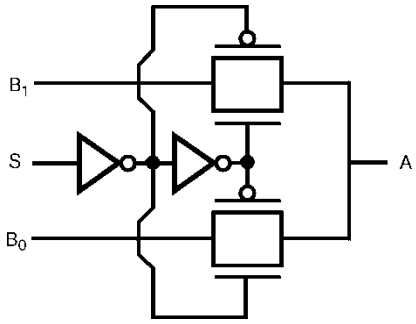


Figure 1. Logic Symbol

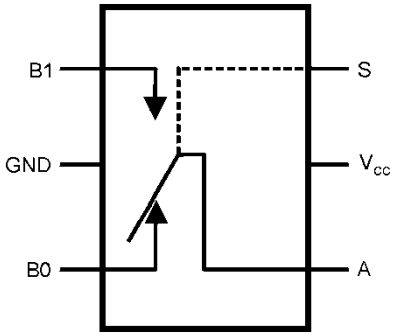


Figure 2. Analog Symbol

Pin Configuration

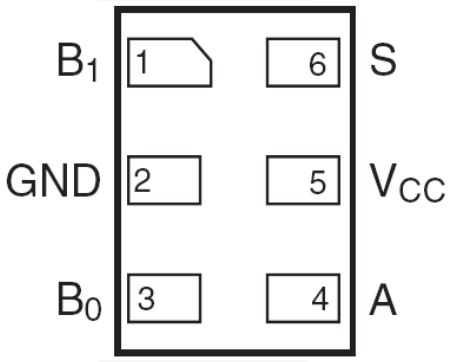


Figure 3. Pad Assignments

Function Table

Input (S)	Function
Logic Level LOW	B_0 Connected to A
Logic Level HIGH	B_1 Connected to A

Pin Descriptions

Pin#	Name	Description
1	B_1	Data Ports
2	GND	Ground
3	B_0	Data Ports
4	A	Data Ports
5	V_{CC}	Power Supply
6	S	Control Input

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage		-0.5	7.0	V
V_S	DC Switch Voltage[1]		-0.5	V_{CC}+0.5	V
V_{IN}	DC Input Voltage[1]		-0.5	7.0	V
I_{IK}	DC Input Diode Current at V_{IN} < 0 V		-50		mA
I_{OUT}	DC Output Current			128	mA
$I_{CC/IGND}$	DC V_{CC} or Ground Current			±100	mA
T_{STG}	Storage Temperature Range		-65	+150	°C
T_J	Junction Temperature Under Bias			+150	°C
T_L	Junction Lead Temperature (Soldering, 10 seconds)			+260	°C
P_D	Power Dissipation at +85°C			180	mW
ESD	Electrostatic Discharge Capability	Human Body Model, JESD22-A114		5	kV

Note:

1. Input and output negative voltage ratings may be exceeded if input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min.	Max.	Unit
V_{CC}	Supply Voltage Operating		1.65	5.50	V
V_{IN}	Control Input Voltage[2]		0	V_{CC}	V
V_{IN}	Switch Input Voltage[2]		0	V_{CC}	v
V_{OUT}	Output Voltage[2]		0	V_{CC}	V
T_A	Operating Temperature		-40	+85	°C
t_r, t_f	Input Rise and Fall Time	Control Input V_{CC}=2.3 V–3.6 V	0	10	ns/V
		Control Input V_{CC}=4.5 V–5.5 V	0	5	

Note:

2. Control input must be held HIGH or LOW; it must not float.

Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=+25°C			T_A=-40 to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage		1.65 to 1.95	0.75 V_{CC}			0.75 V_{CC}		V
			2.30 to 5.50	0.7 V_{CC}			0.7 V_{CC}		
V_{IL}	Low Level Input Voltage		1.65 to 1.95			0.25 V_{CC}		0.25 V_{CC}	V
			2.30 to 5.50			0.3 V_{CC}		0.3 V_{CC}	
I_{IN}	Input Leakage Current	0 ≤ V_{IN} ≤ 5.5 V	0 to 5.50		±0.05	±0.1		±1	µA
I_{OFF}	Off State Leakage Current	0 ≤ A, B ≤ V_{CC}	1.65 to 5.50		±0.05	±0.10		±1.00	µA
R_{ON}	Switch On Resistance(3)	V_{IN}=0 V, I_O=30 mA	4.50		3.0	7.0		7.0	Ω
		V_{IN}=2.4 V, I_O=–30 mA			5.0	12.0		12.0	
		V_{IN}=4.5 V, I_O=–30 mA			7.0	15.0		15.0	
		V_{IN}=0 V, I_O=24 mA	3.00		4.0	9.0		9.0	
		V_{IN}=3 V, I_O=–24 mA			10.0	20.0		20.0	
		V_{IN}=0 V, I_O=8 mA	2.30		5.0	12.0		12.0	
		V_{IN}=2.3 V,I_O=–8 mA			13.0	30.0		30.0	
		V_{IN}=0 V, I_O=4 mA	1.65		6.5	20.0		20.0	
		V_{IN}=1.65 V, I_O=–4 mA			17.0	50.0		50.0	
I_{CC}	Quiescent Supply Current: All Channels On or Off	V_{IN}=V_{CC} or GND I_{OUT}=0	5.50			1		10	µA
	Analog Signal Range		V_{CC}	0		V_{CC}	0	V_{CC}	V
R_{RANGE}	On Resistance Over Signal Range(3,7)	I_A=–30 mA, 0 ≤ V_{Bn} ≤ V_{CC}	4.50					25	Ω
		I_A=–24 mA, 0 ≤ V_{Bn} ≤ V_{CC}	3.00					50	
		I_A=–8 mA, 0 ≤ VBn ≤ V_{CC}	2.30					100	
		I_A=–4 mA, 0 ≤ V_{Bn} ≤ V_{CC}	1.65					300	
ΔR_{ON}	On Resistance Match Between Channels(3,4)	I_A=–30 mA, V_{Bn}=3.15	4.50		0.15				Ω
		I_A=–24 mA, V_{Bn}= 2.1	3.00		0.20				
		I_A=–8 mA, V_{Bn}=1.6	2.30		0.50				
		I_A=–4 mA, V_{Bn}=1.15	1.65		0.50				
R_{FLAT}	On Resistance Flatness(3,4,6)	I_A=–30 mA, 0 ≤ V_{Bn} ≤ V_{CC}	5.00		6				Ω
		I_A=–24 mA, 0 ≤ V_{Bn} ≤ V_{CC}	3.00		12				
		I_A=–8 mA, 0 ≤ V_{Bn} ≤ V_{CC}	2.50		28				
		I_A=–4 mA, 0 ≤ V_{Bn} ≤ V_{CC}	1.80		125				

Notes:

3. Measured by the voltage drop between the A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B Ports).
4. Parameter is characterized, but not tested in production.
5. ΔR_{ON} = R_{ON} maximum – R_{ON} minimum measured at identical V_{CC}, temperature, and voltage levels.
6. Flatness is defined as the difference between the maximum and minimum value of on resistance over the specified range of conditions.
7. Guaranteed by design.

AC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=+25°C			T_A=-40 to +85°C		Units	Figure
				Min.	Typ.	Max.	Min.	Max.		
t_{PLH}, t_{PLH}	Propagation Delay Bus-to-Bus[8]	V_{IN}=OPEN	1.65 to 1.95			3.5		3.5	ns	Figure 10 Figure 11
			2.30 to 2.70			1.2		1.2		
			3.00 to 3.60			0.8		0.8		
			4.05 to 5.50			0.3		0.3		
t_{PZL}, t_{PZH}	Output Enable Time Turn-On Time (A to B_n)	V_{IN}=2x V_{CC} for t_{PZL} V_{IN}=0 V for t_{PZH}	1.65 to 1.95	7.0		23.0		24.0	ns	Figure 10 Figure 11
			2.30 to 2.70	3.5		13.0		14.0		
			3.00 to 3.60	2.5		6.9		7.6		
			4.50 to 5.50	1.7		5.2		5.7		
t_{PLZ}, t_{PHZ}	Output Disable Time Turn-Off Time (A Port to B Port)	V_{IN}=2x V_{CC} for t_{PLZ} V_{IN}=0 V for t_{PHZ1}	1.65 to 1.95	3.0		12.5		13.0	ns	Figure 10 Figure 11
			2.30 to 2.70	2.0		7.0		7.5		
			3.00 to 3.60	1.5		5.0		5.3		
			4.50 to 5.50	0.8		3.5		3.8		
t_{BBM}	Break-Before-Make Time[9]		1.65 to 1.95	0.5			0.5		ns	Figure 12
			2.30 to 2.70	0.5			0.5			
			3.00 to 3.60	0.5			0.5			
			4.50 to 5.50	0.5			0.5			
Q	Charge Injection[9]	C_L=0.1 nF, V_{GEN}=0 V	5.00		7				pC	Figure 13
		R_{GEN}=0 Ω	3.30		3					
OIRR	Off Isolation[10]	R_L=50 Ω, f=10 MHz	1.65 to 5.50		-57				dB	Figure 14
Xtalk	Crosstalk	R_L=50 Ω, f=10 MHz	1.65 to 5.50		-54				dB	Figure 15
BW	-3 dB Bandwidth	R_L=50 Ω	1.65 to 5.50		250				MHz	Figure 18
THD	Total Harmonic Distortion[9]	R_L=600 Ω, 0.5 V_{PP}, f=600 Hz to 20 KHz	5.00		.011				%	

Notes:

8. This parameter is guaranteed by design, but not tested. The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the 50pF load capacitance when driven by an ideal voltage source (zero output impedance).
9. Guaranteed by design.
10. Off Isolation = 20 $\log_{10}$ [V_A / V_{Bn}].

Capacitance

T_A = +25°C, f=1MHz. Capacitance is characterized, but not tested in production.

Symbol	Parameter	Conditions	Typical	Unit	Figure
C_{IN}	Control Pin Input Capacitance	V_{CC}=0 V	2.3	pF	
C_{IO-B}	B Port Off Capacitance	V_{CC}=5.0 V	6.5	pF	Figure 16
C_{IOA-ON}	A Port Capacitance, Switch Enabled	V_{CC}=5.0 V	18.5	pF	Figure 17

Typical Performance Characteristics

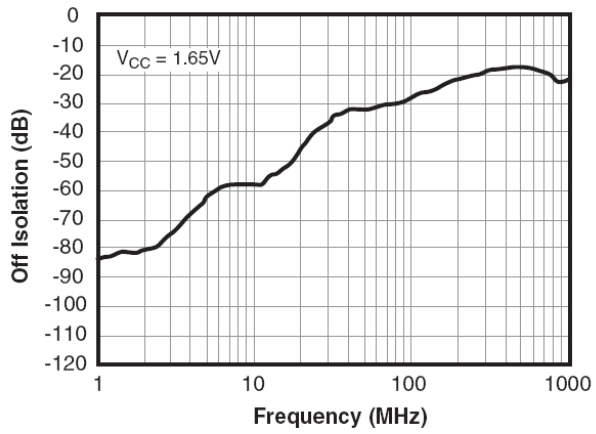


Figure 4. Off Isolation, V_{CC}-1.65 V

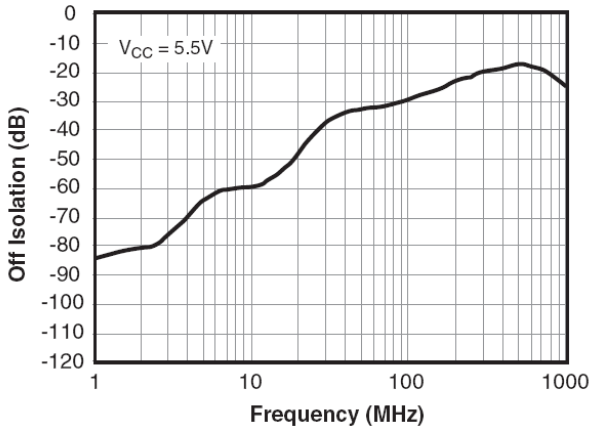


Figure 5. Off Isolation, V_{CC}-5.5 V

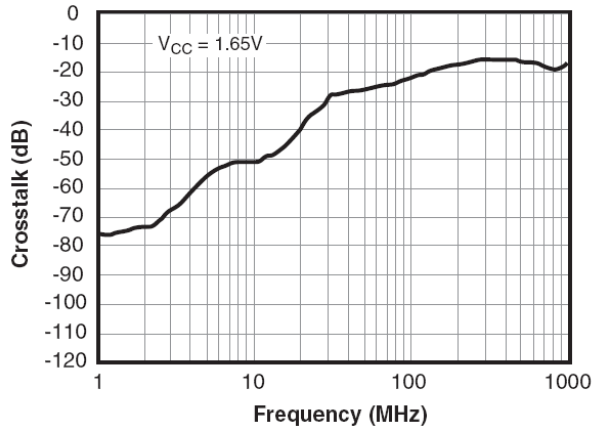


Figure 6. Crosstalk, V_{CC}=1.65 V

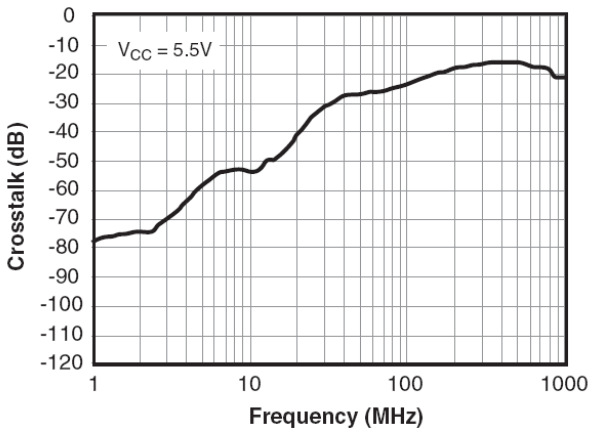


Figure 7. Crosstalk, V_{CC}=5.5 V

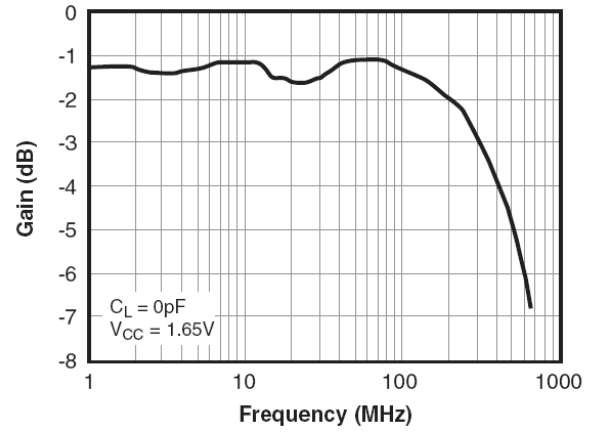


Figure 8. Bandwidth, V_{CC}=1.65 V

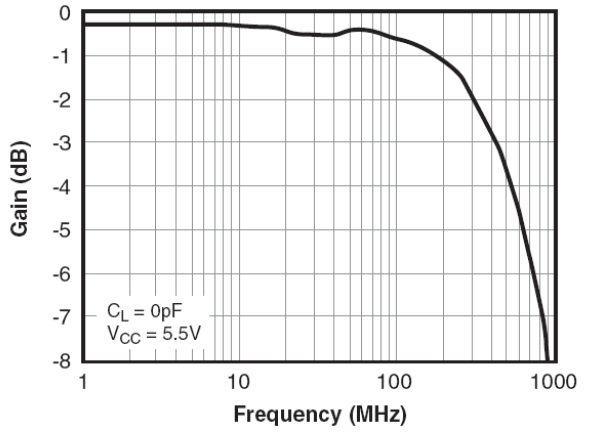
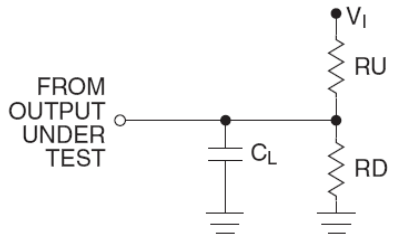


Figure 9. Bandwidth, V_{CC}=5.5 V

AC Loading and Waveforms



Notes:
Input driven by 50Ω source terminated in 50Ω
C_L includes load and stray capacitance
Input PRR = 1.0 MHz; t_W = 500 ns

Figure 10. AC Test Circuit

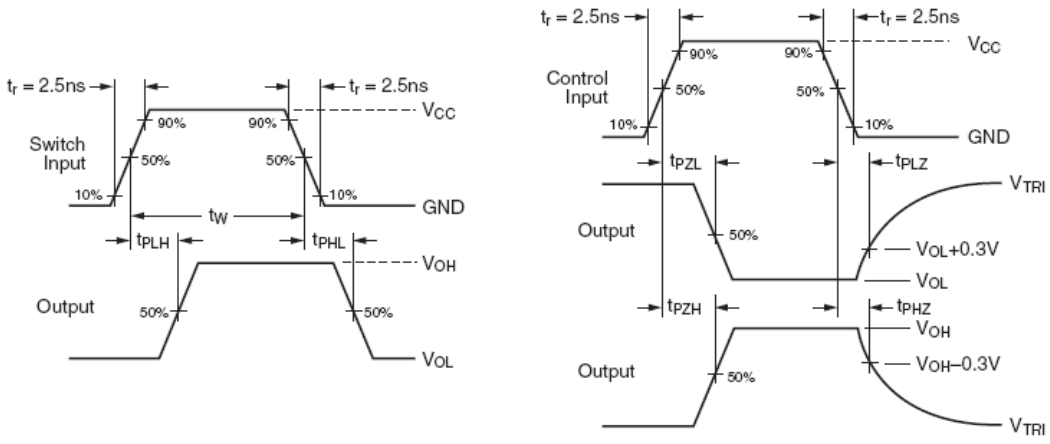


Figure 11. AC Waveforms

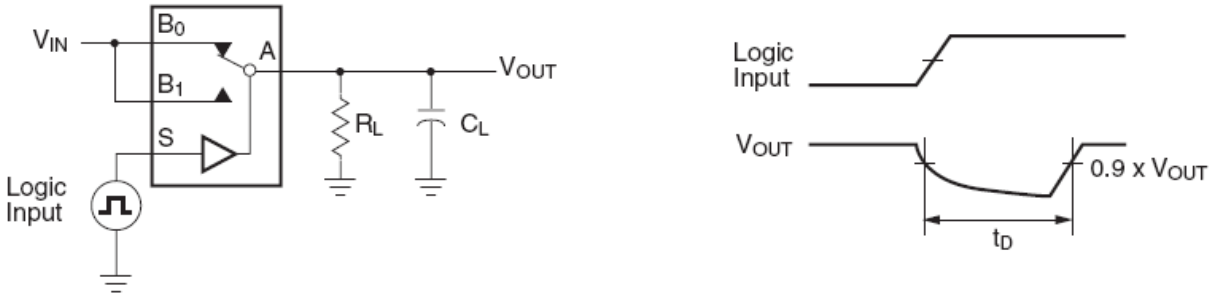


Figure 12. Break-Before-Make Interval Timing

AC Loading and Waveforms (Continued)

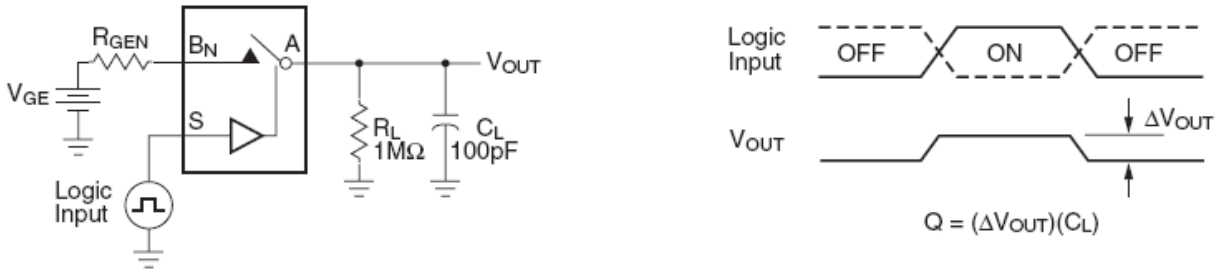


Figure 13. Charge Injection Test

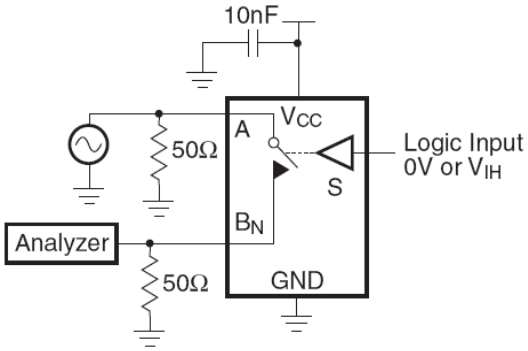


Figure 14. Off Isolation

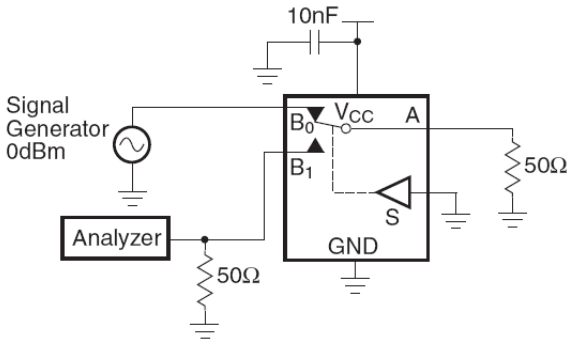


Figure 15. Crosstalk

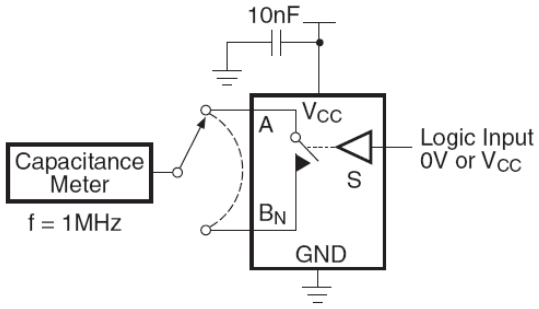


Figure 16. Channel Off Capacitance

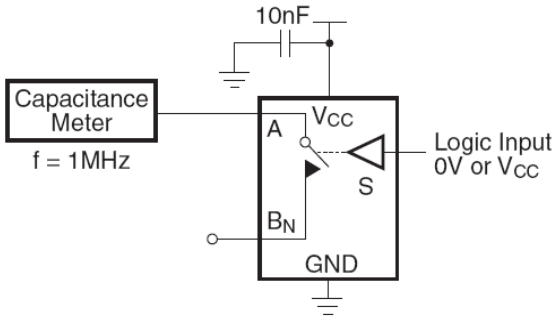


Figure 17. Channel On Capacitance

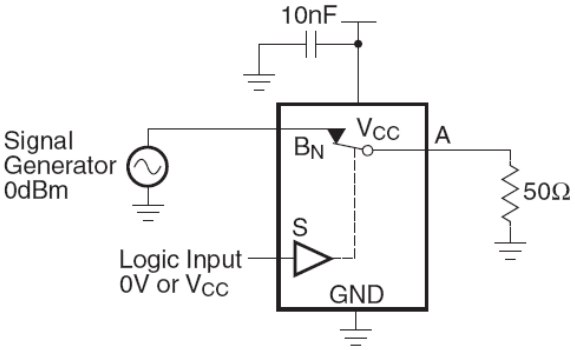
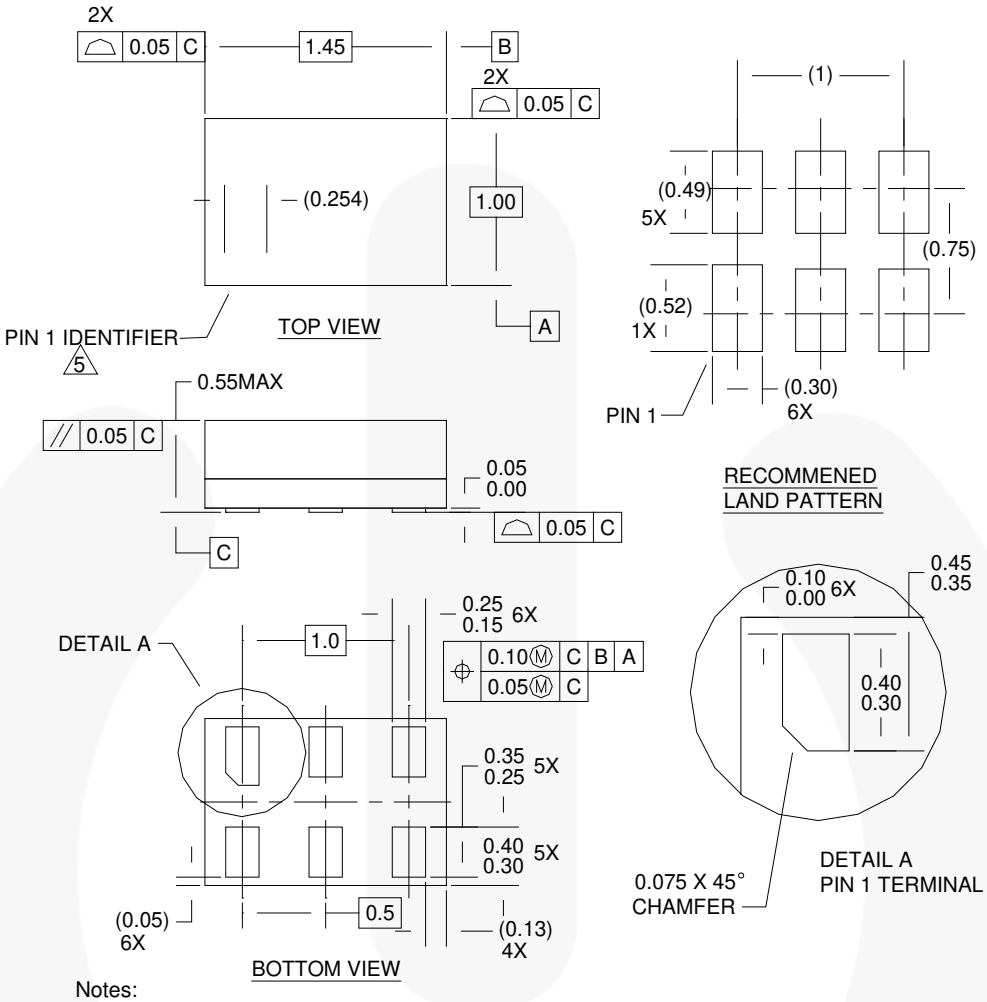


Figure 18. Bandwidth

Physical Dimensions



Notes:

1. CONFORMS TO JEDEC STANDARD M0-252 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y14.5M-1994
4. FILENAME AND REVISION: MAC06AREV4
5. PIN ONE IDENTIFIER IS 2X LENGTH OF ANY OTHER LINE IN THE MARK CODE LAYOUT.

Figure 19. 6-Lead, MicroPak™ 1.0 mm Wide Package

Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent revision. Package specifications do not expand the terms of Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

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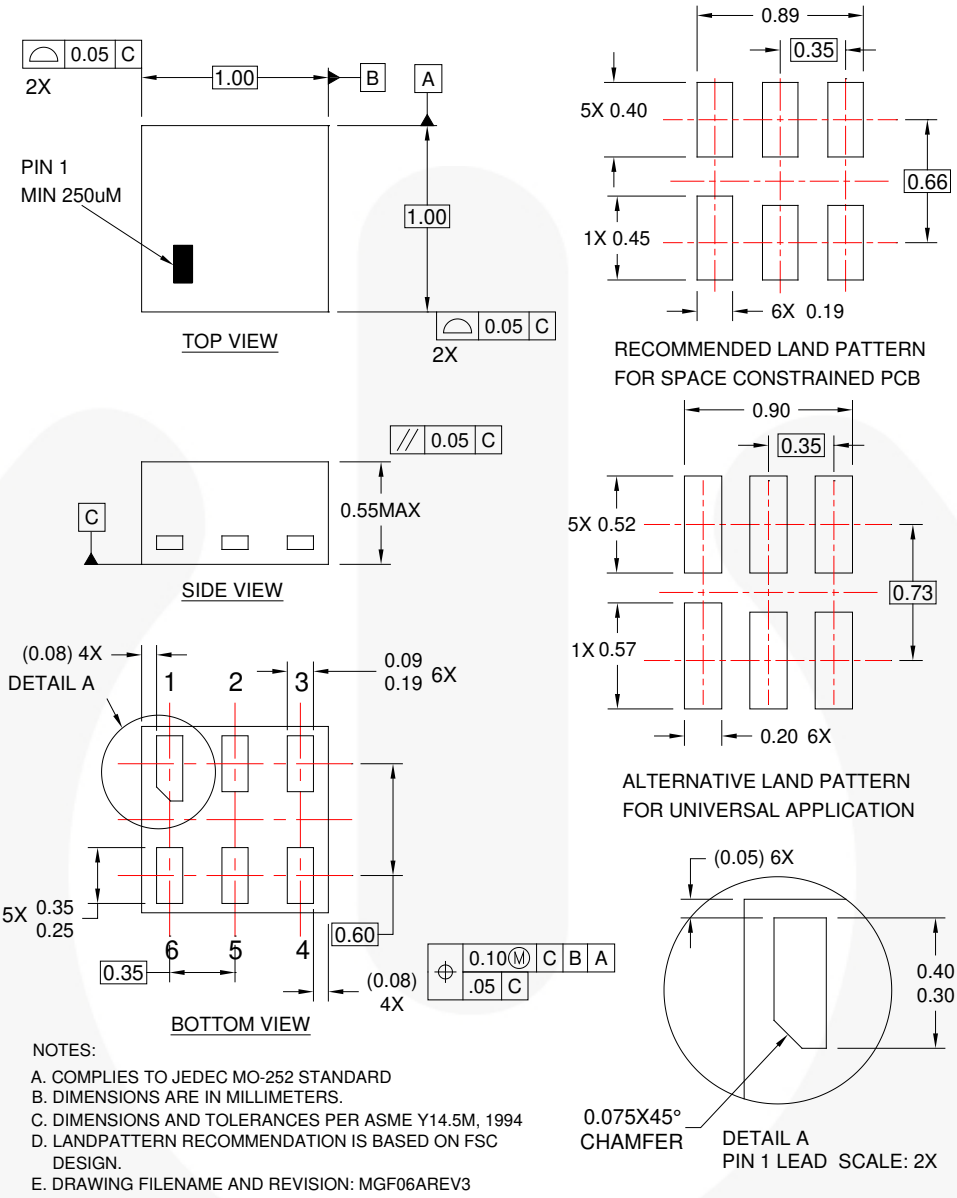
Tape and Reel Specifications

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications:
http://www.fairchildsemi.com/products/logic/pdf/micropak_tr.pdf.

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
L6X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

Physical Dimensions



NOTES:

A. COMPLIES TO JEDEC MO-252 STANDARD
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
D. LANDPATTERN RECOMMENDATION IS BASED ON FSC DESIGN.
E. DRAWING FILENAME AND REVISION: MGF06AREV3

Figure 20. 6-Lead, MicroPak2™, 1x1 mm Body, .35 mm Pitch

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Tape and Reel Specifications

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications:
http://www.fairchildsemi.com/packaging/MicroPAK2_6L_tr.pdf.

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
FHX	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

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Green FPS™
Green FPS™ e-Series™
Gmax™
GTO™
IntelliMAX™
ISOPLANAR™
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MegaBuck™
MICROCOUPLER™
MicroFET™
MicroPak™
MicroPak2™
MillerDrive™
MotionMax™
mWSaver®
OptoHiT™
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OPTOPLANAR®
PowerTrench®
PowerXS™
Programmable Active Droop™
QFET®
QS™
Quiet Series™
RapidConfigure™
Saving our world, 1mW/W/kW at a time™
SignalWise™
SmartMax™
SMART START™
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SPM®
STEALTH™
SuperFET®
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
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