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FSA9591 — USB Accessory Detection Switch with Integrated Linear Battery Charger

Features

- Detection:
 - USB Data Cable
 - UART Serial Link
 - Charger Detection (CDP, DCP)
 - Factory-Mode Cables
 - Teletype (TTY) Converter
- Linear Charger with up to 950 mA Charging Current Full-Speed and High-Speed 2.0 Compliant
- Automatic Switching with Available Interrupt
- UART: Rx/D & Tx/D
- USB: FS and HS 2.0 Compliant
- Switch Type: USB, UART

Description

The FSA9591 is a USB accessory detection switch with an integrated lithium ion (Li+) linear battery charger. The FSA9591 is capable of detecting factory test modes, car kit type 1 and travel adapter charger, USB data port, and USB chargers. Compliant with the USB battery charging rev. 1.1 specification, the FSA9591 can detect USB Standard Downstream Ports (SDP), Dedicated Charging Ports (DCP), and Charging Downstream Ports (CDP).

The integrated linear charger uses constant current, constant voltage, and thermal control loops to charge Li+ batteries and provide protection. The FSA9591 also includes two programmable LDOs, capable of supplying 300mA each, for powering other devices in mobile phones. Battery presence detection via DETBAT_N and charging current sensing through VICHG are also provided. V_{BUS_IN} pin can tolerate up to 28 V.

Applications

- Cell Phones, Smart Phones, PDAs
- Tablets, Portable Media Players
- Gaming Devices, Digital Cameras

Ordering Information

Part Number	Operating Temperature Range	Top Mark	Package
FSA9591UCX ⁽¹⁾	-40 to +85°C	NT	30-Lead WLCSP (2.38 mm x 1.98 mm x 0.625 mm, 0.4 mm Pitch)

Note:

1. Includes backside lamination.

Typical Application

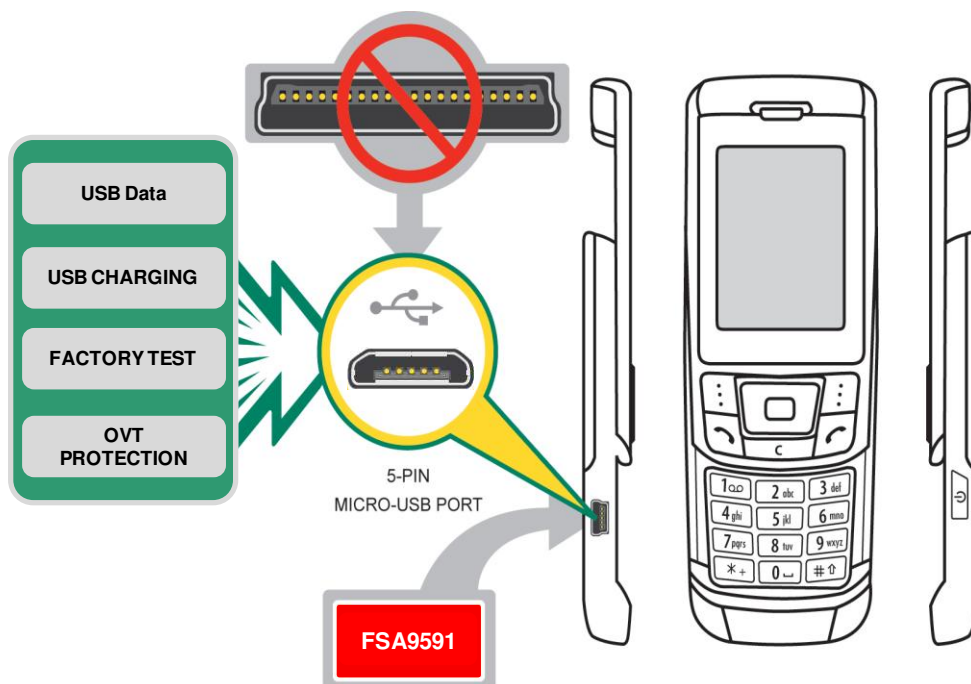


Figure 1. Mobile Phone Example

Block Diagram

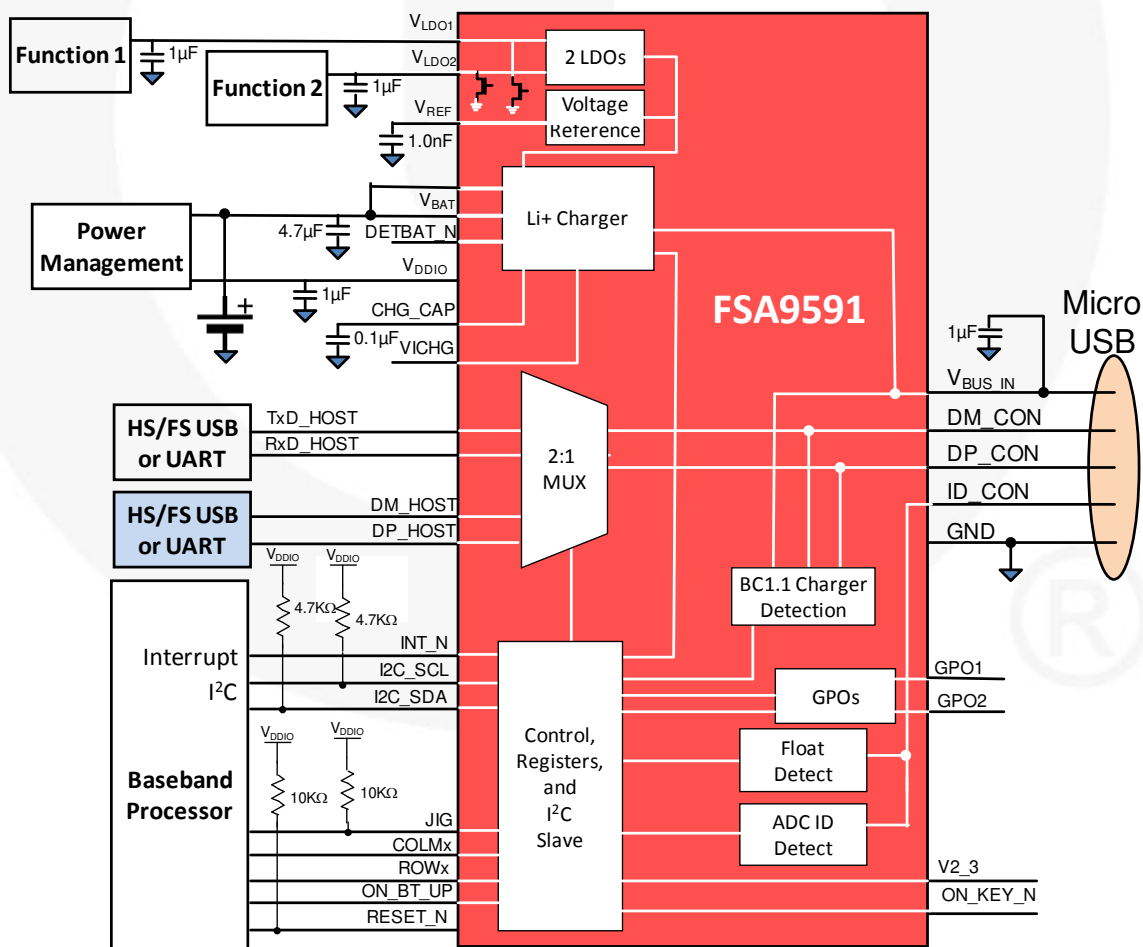


Figure 2. Block Diagram

Pin Configuration

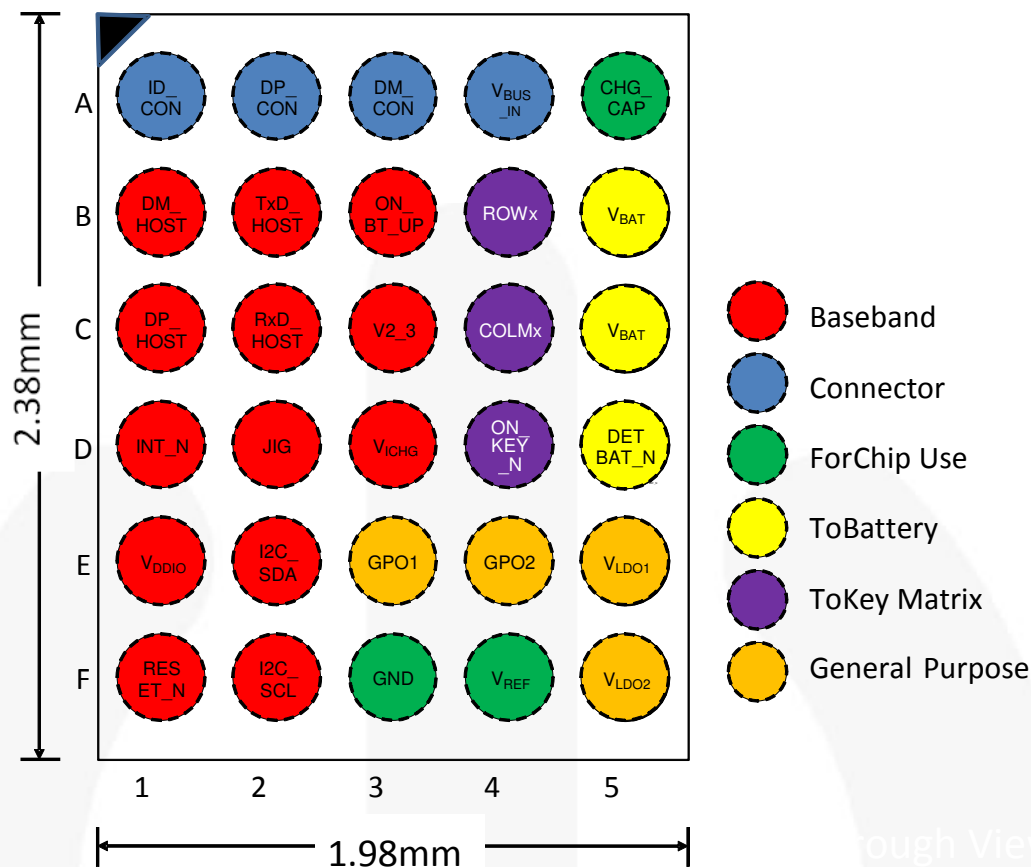


Figure 3. Pin Assignment (Top Through View)

Pin Descriptions

Name	Ball	Type	Default State	Description
USB Interface				
DP_HOST	C1	Signal Path	Open	D+ signal switch path; dedicated USB port to be connected to the USB transceiver on the phone
DM_HOST	B1	Signal Path	Open	D- signal switch path; dedicated USB port to be connected to the USB transceiver on the phone
UART Interface				
TxD_HOST	B2	Signal Path	Open	Transmitter (Tx) switch path from UART on the phone to the D- pin of the USB connector
RxD_HOST	C2	Signal Path	Open	Receiver (Rx) switch path from UART on the phone to the D+ pin of the USB connector
Connector Interface				
GND	F3	Ground	N/A	Ground
ID_CON	A1	Signal Path	Pull-Up Current	Connected to the USB connector ID pin and used for detecting accessories
DP_CON	A2	Signal Path	Open	Connected to the USB connector D+ pin; depending on the signaling mode, this pin can be switched to DP_HOST or RxD_HOST pins
DM_CON	A3	Signal Path	Open	Connected to the USB connector D- pin; depending on the signaling mode, this pin can be switched to DM_HOST or TxD_HOST pins
VBUS_IN	A4	Power Path	N/A	Input voltage supply pin to be connected to the VBUS pin of the USB connector

Name	Ball	Type	Default State	Description																			
Power Interface																							
V _{DDIO}	E1	Power	N/A	Factory and I ² C interface I/O supply pin																			
V _{BAT}	B5,C5	Power Path	N/A	Battery charger output and chip supply pin to be connected to mobile phone battery																			
V _{LDO1}	E5	Power	Hi-Z	Programmable first LDO regulator output																			
V _{LDO2}	F5	Power	Hi-Z	Programmable second LDO regulator output																			
V _{REF}	F4	Power	Hi-Z	0.6 V voltage reference for internal use. Can output a maximum of 1 mA external load. Needs to be enabled for LDO operation.																			
CHG_CAP	A5	Power	Hi-Z	Bypass capacitor for charger that forms a low-voltage power supply for internal circuitry (0.1 μF typical value)																			
V _{ICHG}	D3	Power	Hi-Z	Analog signal proportional to the charging current flowing to battery from V _{BUS_IN}																			
Other Interface																							
JIG	D2	Open-Drain Output (V _{DDIO})	Hi-Z	Output control signal driven by the FSA9591 and used by the processor for factory test modes (active LOW open drain output)																			
ON_KEY_N	D4	Input (Comparator)	N/A	Input that indicates whether the phone ON key has been pressed (active LOW)																			
ON_BT_UP	B3	Switched Path	Hi-Z	Switch connected to the V2_3 pin to boot up the processor during factory mode or when the ON_KEY_N signal is asserted																			
				VBUS	ON_KEY_N	JIG	ON_BT_UP =	Valid VBUS	X	X	V2_3	LOW	LOW	X	V2_3	LOW	HIGH	LOW	V2_3	LOW	HIGH	Hi-Z	Hi-Z
				VBUS	ON_KEY_N	JIG	ON_BT_UP =																
				Valid VBUS	X	X	V2_3																
				LOW	LOW	X	V2_3																
LOW	HIGH	LOW	V2_3																				
LOW	HIGH	Hi-Z	Hi-Z																				
V2_3	C3	Switched Path	Hi-Z	Pin switched to ON_BT_UP for realizing ON_BT_UP functionality (<i>see ON_BT_UP description</i>)																			
COLMx	C4	Switched Path	Hi-Z	Used to translate the ON key signal from a high-voltage signal into a low-voltage closed switch in the processor key matrix circuitry. Switches to ROWx.																			
				V _{BAT}	ON_KEY_N	COLMx/ROWx	LOW	X	OPEN	VALID	HIGH	OPEN	VALID	LOW	SHORT								
				V _{BAT}	ON_KEY_N	COLMx/ROWx																	
				LOW	X	OPEN																	
VALID	HIGH	OPEN																					
VALID	LOW	SHORT																					
ROWx	B4	Switched Path	Hi-Z	Used to translate ON key signal from a high-voltage signal into a low-voltage closed switch in the processor key matrix circuitry. Switches to COLMx.																			
				V _{BAT}	ON_KEY_N	COLMx/ROWx	LOW	X	OPEN	VALID	HIGH	OPEN	VALID	LOW	SHORT								
				V _{BAT}	ON_KEY_N	COLMx/ROWx																	
				LOW	X	OPEN																	
VALID	HIGH	OPEN																					
VALID	LOW	SHORT																					
RESET_N	F1	Open-Drain Output (V _{DDIO})	N/A	Output to synchronize the processor with detected accessories. The threshold is 1.4 V rising edge and 1.2 V falling edge and the pulse lasts for 250 ms.																			
GPO1	E3	Output (V _{DDIO})	N/A	General purpose; first output programmed from register bit GPO [GPO1]. This can be push/pull or open drain based on the register bit GPO [GPO1_OD].																			
GPO2	E4	Output (V _{DDIO})	N/A	General purpose; second output programmed from register bit GPO [GPO2]. This can be push/pull or open drain based on the register bit GPO [GPO2_OD].																			
DETBAT_N	D5	Input (Comparator)	N/A	Detect battery input to determine the battery presence in the phone; DETBAT_N=HIGH when battery is not present. DETBAT_N=LOW when battery is present or when charger is enabled, regardless of battery presence. Internally pulled up.																			

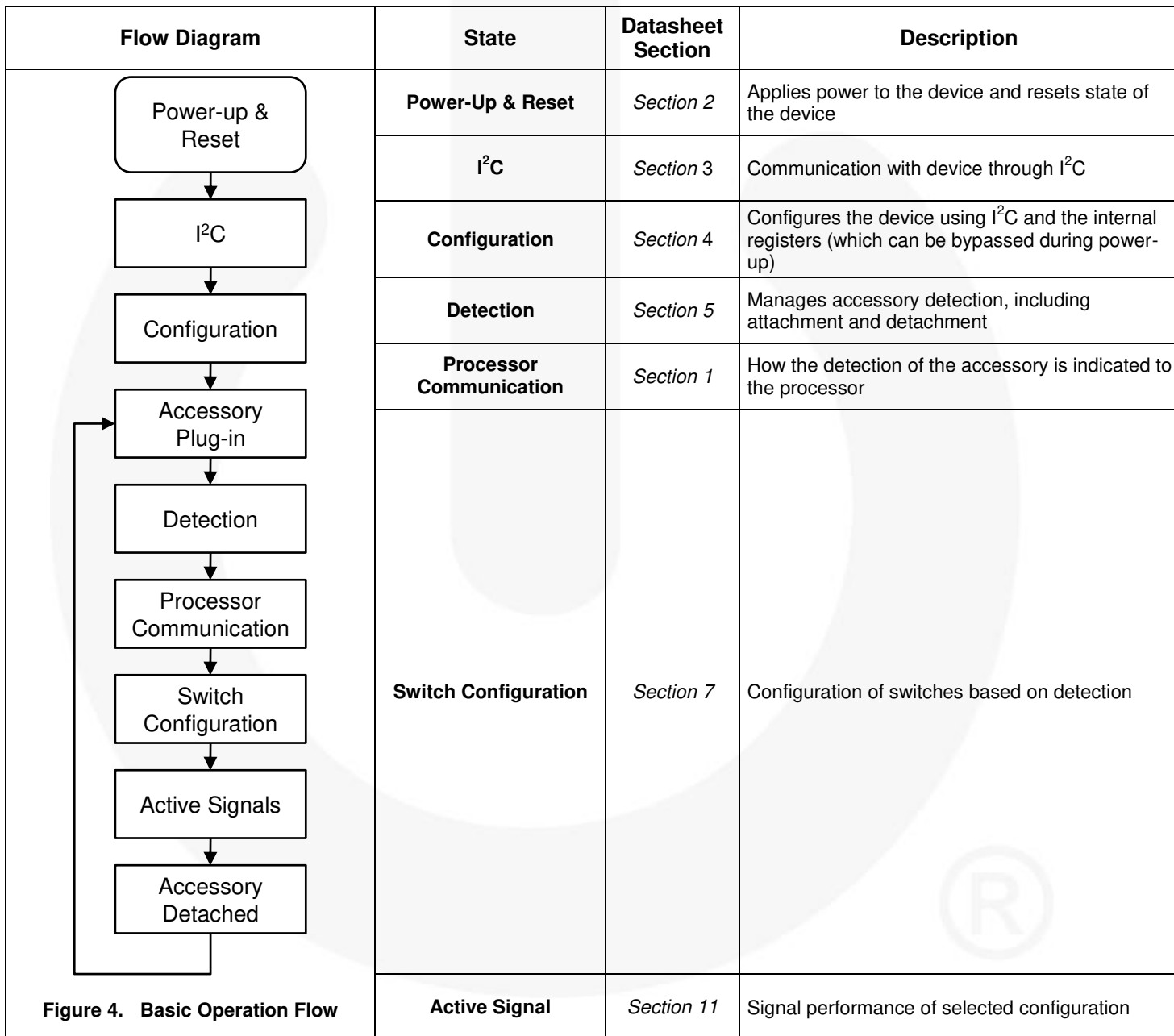
Name	Ball	Type	Default State	Description
I²C Interface				
I2C_SCL	F2	Input (V _{DDIO})	N/A	I ² C serial clock signal to be connected to the phone-based I ² C master
I2C_SDA	E2	Open-Drain I/O (V _{DDIO})	Hi-Z	I ² C serial data signal to be connected to the phone-based I ² C master
INT_N	D1	CMOS Output (V _{DDIO})	Low	Interrupt active LOW output used to prompt the phone baseband processor to read the I ² C register bits or indicate a change in ID_CON pin status or accessories' attach status

1. Functionality

The FSA9591 is USB port accessory detector and switch with integrated 28 V over-voltage tolerance. Fully controlled using I²C, FSA9591 enables high-speed USB 2.0 Standard Downstream Port (SDP), USB Charging Downstream Port (CDP) battery charger, USB Dedicated Charging Port (DCP) charger data cables to use a common connector micro or mini USB 2.0 port. Factory-mode cables can be detected and switched to use either the UART or USB data path. The FSA9591 can be programmed for manual switching or automatic switching of data paths.

1.1. Functional Overview

The FSA9591 is designed for minimal software requirements for proper operation. The flow diagram in Figure 4 walks through the fundamental steps of operation and contains references to more detailed information.



2. Power-Up & Reset

The FSA9591 does not need special power sequencing for correct operation. The main power for accessory detection is provided by V_{BAT} only. V_{DDIO} is only used for I²C interface and interrupt processing. The linear charger power is provided by V_{BUS_IN} .

Table 1 summarizes the enabled features of each power state. The valid voltages levels for each power supply can be found in Section 12.2

Table 1. Power States Summary

Valid V_{BUS_IN}	Valid V_{BAT}	Valid $V_{DDIO}^{(2)}$	Power State	Enabled Functionality			
				Processor Communication (I ² C & Interrupts)	Detection/ Switching	Charging	LDO
N	N	N	Power Down	NO			
N	N	Y ⁽³⁾	Not Typical	Illegal State			
N	Y	N	Detection/Switching Active	NO	YES	NO	YES
N	Y	Y	Detection/Switching Active	YES	YES	NO	YES
Y	N	N	Charging Only	NO	NO	YES	NO
Y	N	Y ⁽³⁾	Not Typical	NO	NO	YES	NO
Y	Y	N	Powered On State	NO	YES	YES	YES
Y	Y	Y	Powered On State	YES	YES	YES	YES

Notes:

- V_{DDIO} is expected to be the same supply used by the baseband I/Os.
- Typically V_{DDIO} is only present when V_{BAT} is valid.
- X=Don't care.

2.1. Reset

When the device is reset, all the registers are initialized to the default values shown in Section 12.14 and all switch paths are open. After reset or power up, FSA9591 enters Standby Mode and is ready to detect accessories sensed on the V_{BUS_IN} or ID_CON pins.

2.1.1. Hardware Reset

Power-On Reset (POR) is caused by the initial rising edge of V_{BAT} or V_{BUS_IN} .

2.1.2. Software Reset

The device can be reset through software by writing to the Reset bit in the Register (1BH).

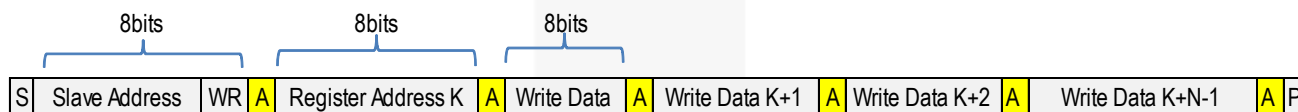
3. I²C

The FSA9591 integrates a full fast-mode I²C slave controller compliant with the I²C specification version 2.1. The FSA9591 I²C interface runs up to 400 kHz.

The slave address is shown in Table 2. Status information and configuration occurs via the I²C interface. *Please see Section 12.12 for more information.*

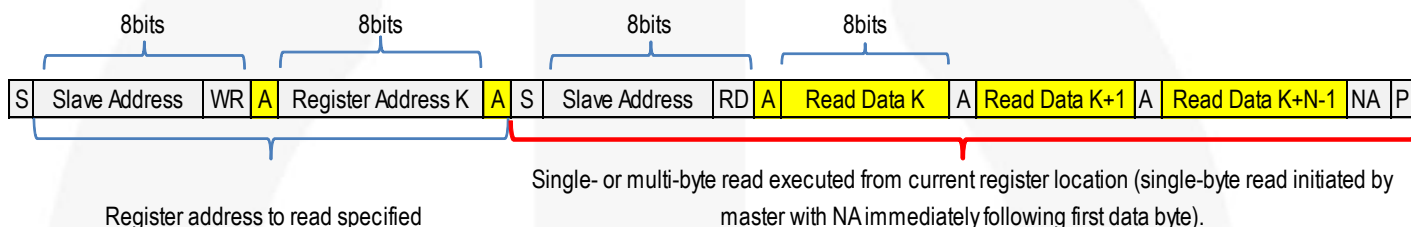
Table 2. I²C Slave Address

Name	Size (Bits)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Slave Address	8	0	1	0	0	1	0	1	Read / Write



Note: A single-byte write is initiated by the master with P immediately following first data byte.

Figure 5. I²C Write Sequence



Note: If no register specified, master reads from the current register. In this case, only sequence in red bracket is needed.

Figure 6. I²C Read Sequence

Legend

	From Master to Slave	S	Start Condition	NA	NOT Acknowledge (SDA HIGH)	RD	Read=1
	From Slave to Master	A	Acknowledge (SDA LOW)	WR	Write=0	P	Stop Condition

4. Configuration

FSA9591 requires minimal configuration for proper detection, charging and reporting. Follow these steps for full configuration:

- Write Control register (02h) to configure manual or automatic switching modes.
 - If using manual switching modes, write Manual SW 1 register (13h) to configure switches.

- Write Control register (02h) to clear INT Mask bit. This enables interrupts to the baseband.

The linear charger defaults to automatic charging at either 90mA or 450mA based on the accessory that was detected.

5. Detection

The FSA9591 monitors both V_{BUS_IN} and ID_CON to detect accessories. The ID_CON detection is a “resistive detection” that reads the resistance to GND on the ID_CON pin to determine the accessory attached. Table 3 shows assignment of accessories based on resistor values. FSA9591 can also detect accessories

with ID resistances outside the specified ranges; these are detected in the same manner as the defined accessories. FSA9591 interrupts the baseband processor and provides the correct ADC value, as shown in Table 3.

Table 3. ID_CON Accessory Detection

ADC Code					Equivalent $R_{ID}^{(6)}$			Description
4	3	2	1	0	Min.	Target	Max.	
1	0	1	0	1	117.4 k Ω	121 k Ω	124.6 k Ω	Unknown Accessory
1	0	1	1	0	145.5 k Ω	150 k Ω	154.5 k Ω	Unknown Accessory
1	0	1	1	1	176.4 k Ω	200 k $\Omega^{(5)}$	206.0 k Ω	Travel Adapter (TA) or Car Kit Type 1 Charger
1	1	0	0	0	247.3 k Ω	255 k Ω	262.7 k Ω	Factory Mode Boot OFF-USB
1	1	0	0	1	291.9 k Ω	301 k Ω	310.1 k Ω	Factory Mode Boot ON-USB
1	1	0	1	0	354.0 k Ω	365 k Ω	375.9 k Ω	Unknown Accessory
1	1	0	1	1	428.7 k Ω	442 k $\Omega^{(5)}$	455.3 k Ω	Unknown Accessory
1	1	1	0	0	507.3 k Ω	523 k Ω	538.7 k Ω	Factory Mode Boot OFF-UART
1	1	1	0	1	600.4 k Ω	619 k Ω	637.6 k Ω	Factory Mode Boot ON-UART
1	1	1	1	0	750.0 k Ω	1000 k Ω	1030.0 k Ω	Unknown Accessory
Not 'h1F or any code above					3 M Ω	None of the above ranges		Unknown Accessory

Note:

- These accessories need V_{BUS} to be valid to be detected since they are charger accessories.
- For resistances between the defined regions, the FSA9591 detects the ADC value above OR below the given resistance.

Factory modes are initiated with the attachment of special test hardware, called a “JIG box,” for factory testing. The FSA9591 automatically configures switch paths to any of the factory-mode accessories when the appropriate resistor is sensed on the ID_CON pin. A change of resistor on the ID_CON pin dynamically switches between factory modes and auto-configures the appropriate switch paths without detaching and attaching the cable.

The different factory mode accessories with the associated resistor values (1% standard resistors) on the ID_CON pin and The switch paths for factory modes are listed in Table 4. The FSA9591 allows HS USB, FS USB, and UART signals to be passed on both ports with equal performance. This allows greater flexibility when designing with the FSA9591.

Table 4. ID_CON Factory Cable Detection

Configuration Type		DP_CON	DM_CON	ID_CON		
Factory Mode Jig: UART	Boot_On	DP_HOST1	DM_HOST1	600 k Ω	619 k Ω	637 k Ω
	Boot_Off	DP_HOST1	DM_HOST1	507 k Ω	523 k Ω	538 k Ω
Factory Mode Jig: USB	Boot_On	DP_Host	DM_Host	292 k Ω	301 k Ω	310 k Ω
	Boot_Off	DP_Host	DM_Host	247 k Ω	255 k Ω	262 k Ω

The FSA9591 detection algorithms monitor both the V_{BUS} and ID pins of the USB interface. Based on the detection results, multiple registers are updated and the INTB pin is asserted to indicate to the baseband processor that an accessory was detected and to read the registers for the complete information. The detection algorithm allows the application to control the timing of the detection algorithm and the configuration of the internal switches. The flow diagram in Figure 8 shows the operation of the detection algorithm.

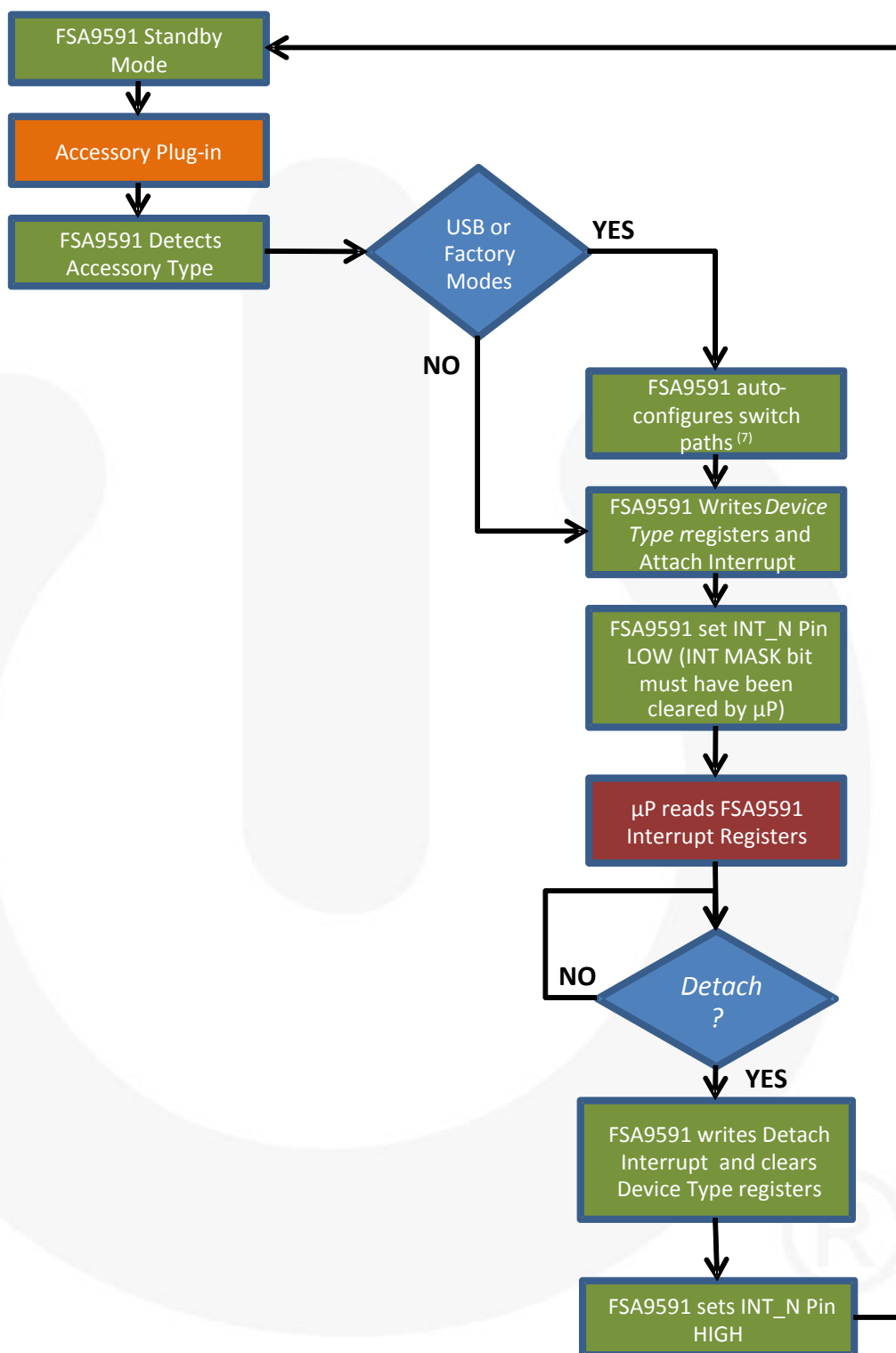


Figure 7. Factory Cable Detection

Note:

7. Factory modes require V_{DDIO} =HIGH before configuring the switches. Refer to the factory mode flow diagram in Figure 8 for details.

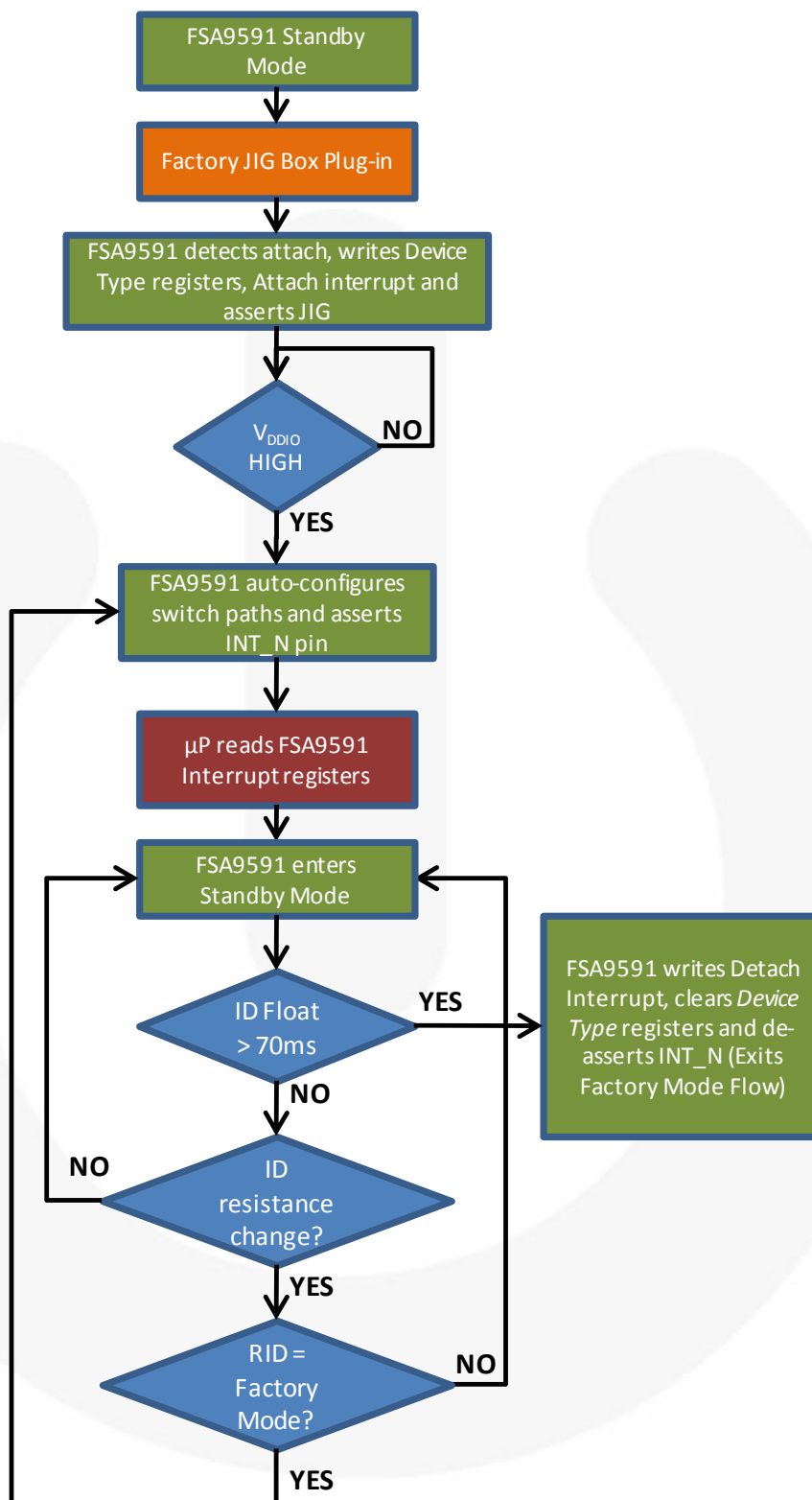


Figure 8. Factory Cable Detection Flow Chart

5.1. USB Port Detection

The types of USB 2.0 ports the FSA9591 can detect are summarized in Table 5.

Table 5. ID_CON and VBUS Detection Table for USB Devices

V _{BUS_IN}	DP_CON	DM_CON	ID_CON Resistance to GND			Accessory Detected ⁽⁸⁾
			Min.	Typ.	Max.	
5V	Not Checked	Not Checked	174.6 kΩ	200 kΩ	206 kΩ	TA (Travel Adapter) Charger (180 kΩ) and Car Kit Charger Type 1 only (200 kΩ) ⁽⁹⁾
5V	Shorted to DM_CON	Shorted to DP_CON	3 MΩ	Open	Open	USB Dedicated Charging Port, Travel Adapter or Dedicated Charger (DCP) ⁽⁹⁾
5V	DP_HOST	DM_HOST	3 MΩ	Open	Open	USB Charging Downstream Port (CDP) ⁽⁹⁾
5V	DP_HOST	DM_HOST	3 MΩ	Open	Open	USB Standard Downstream Port (SDP) ⁽⁹⁾

Notes:

8. The accessory type is reported in the Device Type 1 (0Ah) register for each valid accessory detected.
9. The FSA9591 follows the battery charging 1.1 specification, which uses DP_CON and DM_CON to determine the USB accessory attached. *Refer to Battery Charging 1.1 specification for further details.*

For SDP and CDP USB accessories, the following pin mapping is automatically configured:

- DP_HOST=DP_CON
- DM_HOST=DM_CON

For DCP charger, the DP_HOST and DM_HOST switches are open. For all USB accessories, V_{BUS_IN} has Over-Voltage Tolerance (OVT) up to 28 V.

6. Processor Communication

Typical communication steps between the processor and the FSA9591 during accessory detection are:

1. INTB is asserted LOW, indicating a change in accessory detection.
2. Processor reads the Interrupt 1 (03h) register to determine if an attach or detach event was detected.
3. Processor reads the Status registers to determine the exact accessory detected.
 - a. Device Type 1 (09h): Indicates which USB, Car Kit CDP, or DCP accessory was detected.
 - b. Device Type 2 (0Ah): Indicates which factory mode or unknown accessory was detected.

7. Switch Configuration

FSA9591 devices have two methods of configuring the internal switches: it can auto-configure the switches or the switches can be configured manually by the processor. Typical applications use Auto-Configuration Mode and do not require interaction with the baseband to configure the switches correctly.

7.1. Manual Switching

Manual switching is enabled by writing the following registers:

- Manual Switch (13h): Configures the switches for DM_CON and DP_CON in addition to manual control of the JIG output.

8. GPOs

The FSA9591 has two general-purpose outputs (GPOs) that typically turn on the functionality powered by the LDOs. The default state for the GPOs is push-pull outputs with GPO1_OD and GPO2_OD set LOW. If open-drain outputs are required, GPO1_OD and GPO2_OD should be set HIGH.

9. LDOs

The two Low Drop Out (LDO) regulators, which are powered from V_{BAT}, are programmable from 1.8 V to 3.6 V in increments of 100 mV. A 0.6 V reference on VREF must be enabled by writing the register bit GPO[REF_EN] to turn it on. This reference needs to turn on at least 20ms prior to the LDOs turning on to allow time to stabilize the reference if 0.1 nF bypass capacitance is used.

10. ON_KEY Keypad Functionality

The functionality of ON_BT_UP is described in Table 6.

Table 6. ON_KEY_N and ON_BT_UP Truth Table

VBUS	ON_KEY_N	JIG	ON_BT_UP
Valid VBUS	X	X	V2_3
LOW	LOW	X	V2_3
LOW	HIGH	LOW	V2_3
LOW	HIGH	Hi-Z	Hi-Z

How to translate ON_KEY_N to a position in the row and column matrix of the processor keypad is shown in Figure 9.

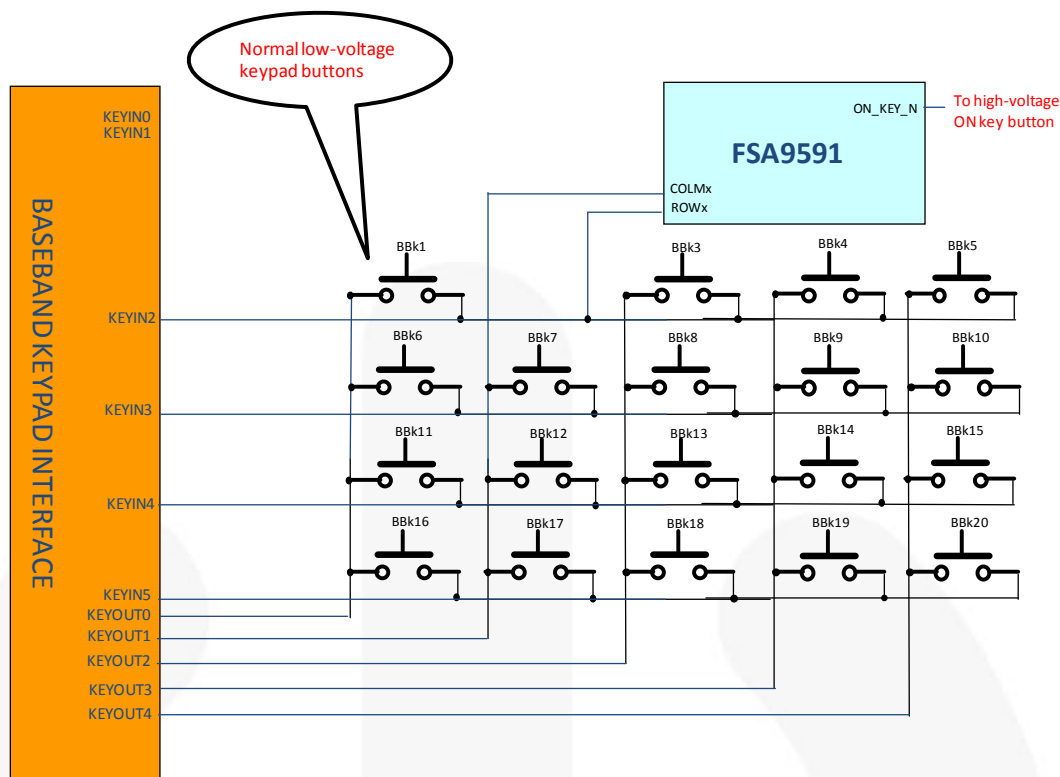


Figure 9. On Key to COLMx and ROWx Mappings

This is the way the FSA9591 translates the ON_KEY_N pin, where the COLMx and ROWx create a virtual button that would have occupied the missing BBk2 switch in the matrix above. Internal to the FSA9591, there is an analog switch that connects COLMx to ROWx based on ON_KEY_N as outlined in Table 7. With ON_KEY_N pulled HIGH to V_{BAT} , a valid V_{BAT} must be present for the keypad functionality to work properly.

Table 7. COLMx/ROWx Truth Table

V_{BAT}	ON_KEY_N	COLMx/ROWx
LOW	X	OPEN
VALID	HIGH	OPEN
VALID	LOW	SHORT

11. Linear Charger

11.1. Charging

Figure 10 shows the different stages of the Li+ linear charger when a charger is connected to the USB pins and a battery is present and discharged below 2.5 V. Generally, the prequalification (called "PRE-CHARGE" in Figure 10) stage is when the battery voltage is below 2.5 V when an I_{SHORT} current of 90 mA charges the battery to V_{SHORT} voltage of 2.5 V. Then the Fast Charge stage starts if a battery charger is detected and the current is increased considerably to a programmable I_{CHARGE} level ("CURRENT REGULATION" in Figure 10). The battery voltage climbs quickly based on the drop caused by the current across the load elements of the battery. Then the voltage climbs linearly until the constant voltage stage is reached at the programmable voltage of V_{OREG} . The current is monitored during this stage ("VOLTAGE REGULATION" in the figure) and, when it reaches the end of current I_{TERM} , charging either halts or progresses to the top off charging if enabled.

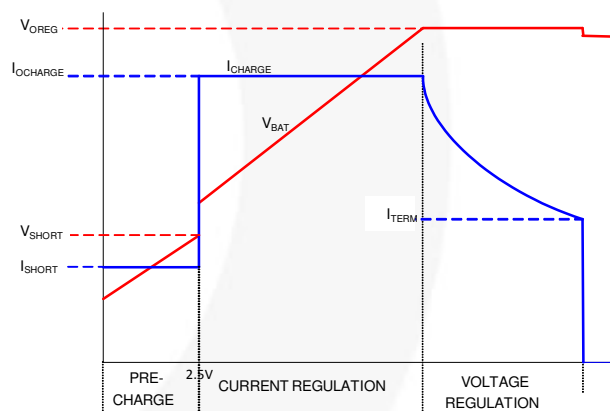


Figure 10. Default Charging Profile

11.1.1. Pre-Qualification Charging Stage

A typical battery has a protection circuit within the battery pack to disconnect the terminals below 2.7 V external to the FSA9591. If it gets below 2.7 V, the battery pack terminals are disconnected externally with the load switch within the battery pack, causing battery voltage V_{BAT} to decay quickly to ground since all that is holding V_{BAT} up is the decoupling capacitors externally. Another way that V_{BAT} can get so low is if V_{BAT} is shorted to ground accidentally. Both of these occurrences are very rare in a typical system since a dead battery is typically above 3 V and only goes below 3V over a long period of time via leakage.

When V_{BUS_IN} is first detected as being within its valid range, two timers are started, a 30-minute timer for the dead battery provision (if that is enabled) via the Charger Ctrl1[DBP_EN] bit (enabled by default since the processor is usually not operating at this low battery voltage range) and a programmable timer for total charging elapsed time enabled (enabled by default as a 5-hour timer via the Charger Ctrl1 [TC_EN] and Charger Ctrl1 [TC_Time] bits).

The linear charger is expected to always take its power from VBUS_IN while monitoring V_{BAT} to determine the optimal charging profile for the shortest charging cycle.

If VBUS_IN is detected when V_{BAT} is below 2.5 V, a charging current of 90mA is used to trickle charge the battery. If it is not a short circuit, V_{BAT} should recover very quickly above 2.5 V since it is only charging decoupling capacitors. V_{DDIO} and V_{BAT} are below the operational voltage of the detection portion, so detection is not performed, nor does FSA9591 communicate over the I²C lines as the linear charger charges the battery above the pre-qualification stage.

If there is a short circuit and the charger Ctrl1 [DBP_EN] bit is enabled (default case), the timer continues up to 30 minutes and expires, shutting down the charger. This limits the short-circuit current of 90mA to be drawn only for 30 minutes. The only way to recover from this fault condition is to remove the short circuit. If the short circuit is not removed, detaching and re-attaching the charger restarts the dead battery provision timer for another 30 minutes before shutting off again.

11.1.2. Constant Current/Constant Voltage Charging Stage

In this stage, V_{BAT} is above the pre-qualification voltage of 2.5 V, but below the programmed Charger Ctrl5 [CV_Voltage] value. The charger detection interrogates the DP_CON, DM_CON, and ID_CON lines to determine if a Dedicated Charger Port (DCP), Charging Downstream Port (CDP), car kit charger (200 kΩ on ID_CON), or a Travel Adapter (TA, 180 kΩ on ID_CON) has been detected. If a charger is detected, the default charging current stays at the fast charge current of 450 mA (default) specified in Charger Ctrl3 [FC_Current] bits. Soft-start techniques are used to gradually increase current to minimize undesirable transients. If a charger is not detected and a USB Standard Downstream Port (SDP) is detected, the fast charge current drops to 90 mA like the pre-qualification current and continues to charge up the battery. This is summarized in Table 8.

Table 8. Default Charging Currents

FC_Override	Auto_FC	Accessory Detected	Fast Charge Current
1	X	X	FC_Current
0	0	X	90 mA
0	1	CDP / DCP/ Car Kit Type 1	FC_Current
0	1	SDP / Unknown / Factory	90mA

Thermal issues are also considered (*see Thermal Regulation section below*) since this is the stage when there is the maximum voltage difference between VBUS_IN and V_{BAT}. Similar to the pre-qualification stage, communication with the baseband is not possible, at least initially, when V_{BAT} is between 2.5 V and the weak-battery threshold (Charger Ctrl2 [WB_Threshold]) so the FSA9591 must be able to charge the battery properly without interaction with the baseband. The 30-minute dead-battery provision timer continues during this stage. When this timer expires and V_{BAT} does not exceed the weak battery threshold, the charger is disabled in compliance with the Battery Charging USB specifications for Dead Battery Provision (DBP). If the processor wakes up prior to the weak-battery threshold, it can change the weak-battery threshold via the Charger Ctrl2 [WB_Threshold] bits to a value consistent with actual wake up voltage and/or disable the dead battery timer via the Charger Ctrl1 [DBP_EN] bit.

Beyond the weak-battery threshold, the processor is expected to be up and controlling the charging process. The constant current is expected to be increased to match the battery charge capacity and the timers for total elapsed charging time can be changed accordingly. The constant voltage threshold is also expected to be set based on battery type and battery temperature, which should be monitored by the processor via separate controls. Thermal regulation within the FSA9591 may have little correlation to the battery temperature since the heat dissipation of the PCB that the FSA9591 is soldered to may be completely different from the heat dissipation within the battery pack.

When the programmed constant voltage threshold (programmed by Charger Ctrl5 [CV_Voltage] bits) is approached, the fast charging current loop is gradually changed to a constant voltage loop where the current is allowed to decay. Charging continues until the end of charge current (set by Charger Ctrl4 [EC_Current] bits) is crossed.

If the top-off timer (set by Charger Ctrl1 [TopOff_EN] bit) is disabled and Charger Ctrl1 [AutoStop] bit is set, all charging stops and the charger monitors V_{BAT}. If V_{BAT} falls 150 mV below the programmed constant voltage, the fast charge charging cycle starts again. A debounce time of 60 ms prior to restarting this cycle prevents glitches or temporary GSM current load of up to 2 A for <1 ms. If the top-off timer is enabled and the AutoStop bit is set; for 30 minutes after the end of charge current threshold has been crossed, the constant voltage charge cycle continues. After that, all charging is stopped and V_{BAT} is monitored again for a drop of 150 mV. If the Charger Ctrl1 [AutoStop] bit is not set, the constant voltage state is never left and the charger keeps trickle charging the battery to keep the voltage at the programmed Charger Ctrl5 [CV_Voltage] voltage.

The FSA9591 maintains this constant voltage with $\pm 0.5\%$ at room temperature to ensure optimal battery performance. The timer measuring the total charging elapsed time continues until the end of charge current threshold is crossed and does not include the top-off timer. If the total time exceeds the time in the Charger Ctrl2 [TC_Time] bits, charging is stopped and the processor (if the voltage is high enough for the processor to function) can interrogate the source of the problem, correct it, then disables and re-enables the charger again to restart charging. If the voltage is not high enough for the processor to function, the problem with the battery needs to be solved and the USB cable needs to be unplugged and plugged back in again.

11.1.3. Timers

The FSA9591 contains multiple timers to ensure that the battery is safely charged under all conditions. These timers include the dead-battery provision timer of 30 minutes, the total-charge timer of 5 to 7 hours, and the top-off timer of 30 minutes. Each timer can be enabled or disabled through I²C register accesses. The total-charge timer value can be programmed through I²C also.

The timers do not reset when an OVP event occurs. If V_{BAT} is above the weak-battery threshold and the baseband is active, the FSA9591 causes an interrupt when the OVP occurs and when the OVP event is disabled. This allows the baseband to control the timers based on the system needs. When OVP is detected, charging stops until the OVP event has recovered.

If V_{BAT} is below the weak-battery threshold and the dead-battery timer is active, FSA9591 takes the most conservative approach and keeps the DBP timer running when OVP is detected.

11.1.4. Thermal Regulation

The FSA9591 contains a thermal regulation loop that is enabled when the junction temperature exceeds 120°C. When this temperature is exceeded, the FSA9591 starts to regulate the current to lower the temperature. It does this by reducing the fast charge current to 90 mA (it is most likely to be in the fast charge cycle since that is when there's maximum power consumption by the linear charger), waits 1 ms, increases the current to 200 mA, waits 1ms, continues along the fast charge currents specified in the Charger Ctrl3 [FC_Current] where the wait between fast charge current steps is 1ms. This algorithm allows for the fastest recovery from a thermal regulation event while still averaging a current that keeps the temperature below 120°C.

The FSA9591 also terminates charging completely if the junction temperature exceeds 140°C. In both cases, the FSA9591 indicates which temperature event occurred via the Interrupt 1 [TREG_EN] and Interrupt 1 [TSD_EN] bits and indicates the removal of these conditions via the Interrupt2 [TREG_DIS] and Interrupt2 [TSD_DIS] bits. Temperature is continuously monitored whenever the charger is enabled.

11.1.5. OVP, OCP, VBUS_IN Regulation

The FSA9591 contains programmable over-voltage protection (OVP) on VBUS_IN, ranging from 6.5 V to 8.0 V, as specified in the Charger Ctrl2 [OVP_Threshold] bits with the default setting of 7 V. If OVP is detected, the FSA9591 terminates charging functionality if charging is active when OVP is detected. The FSA9591 interrupts the processor when the OVP event via the Interrupt 1 [OVP_EN] bit is detected and when the OVP event is removed via the Interrupt 1 [OVP_DIS] bit. The FSA9591 VBUS_IN can tolerate voltages up to 28 V to handle the worst-case automotive scenarios for USB VBUS voltage.

VBUS_IN is typically 5 V \pm 5-10%, depending on the charging current. If the FSA9591 linear charger is programmed to a higher current than the charger can support, a VBUS_IN control loop actively regulates the charging current to maintain at least 4.3 V (typical) on VBUS_IN. The FSA9591 attempts to lower the charger current to allow VBUS_IN to recover to at least 4.3 V. In cases where the charger VBUS_IN is not limited by the charger current, the FSA9591 attempts to lower the current until it reaches the minimum current level and then disables the charger. This VBUS_IN regulation loop is enabled by default and controlled by the Vbus_Reg_Dis bit in the Charger_Ctrl1 register.

If the VBUS_IN regulation loop is disabled, the charging cycle is stopped when VBUS_IN falls below the VBUS_IN valid falling threshold of 3.5 V. Charging remains stopped until the VBUS_IN voltage rises above the rising VBUS_IN valid threshold of 3.7 V and stays above this threshold.

11.2. VICHG

The VICHG is utilized by the host system to identify the amount of current flowing through the charger FET. VICHG is enabled by writing the VICHG_EN bit in the register. When disabled, VICHG has an internal pull-down of 15 k Ω . VICHG should not exceed 2.0 V when enabled.

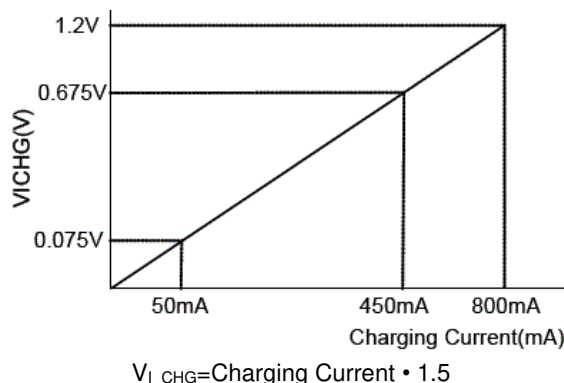


Figure 11. VI_CHG Characteristic

11.3. DETBAT_N

For a typical battery pack, there is an extra terminal with a thermistor NTC resistor between this terminal and ground, which is expected to be much less than 100 k Ω . This terminal is tied to the DETBAT_N pin for a system to disable the charger whenever a battery is not present. DETBAT_N internally has a current source that detects the absence of any path to ground that is >100 k Ω on the DETBAT_N pin. Once a HIGH is detected on DETBAT_N, the charger is immediately disabled.

Some systems, for factory operation or other uses, may leave the charger enabled regardless of whether the battery pack is present or not. In these systems, it is expected that DETBAT_N is tied LOW — always with a resistance to ground of 10 k Ω .

11.4. RESET_N

RESET_N output is used as a system-level Power-On Reset (POR) triggered when VDDIO is above 1.4 V. This RESET_N open-drain output is pulled-down upon FSA9591 power up and released to HIGH after 250 ms (typically from when VDDIO crosses 1.4 V on its rising edge). RESET_N requires a valid VBAT for RESET_N to be actively pulled LOW after power up. This is a tight threshold comparator of VDDIO with a hysteresis of 200 mV to accommodate a slowly rising signal. When VDDIO falls below 1.2 V, RESET_N is pulled LOW again. This timing is shown in Figure 12. RESET_N is not reset on a software reset and is not intended to be a system-level reset, but a POR on VDDIO. The 250 ms timer is reset if VDDIO triggers the falling-edge reset.

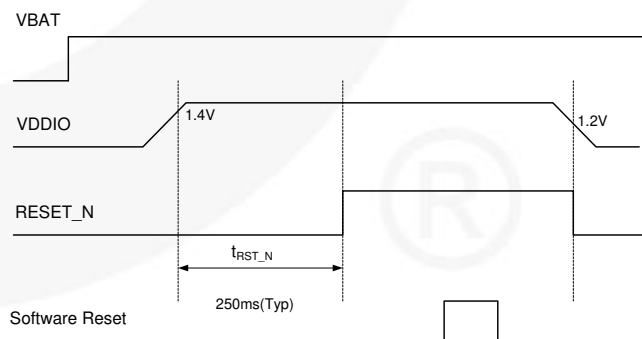


Figure 12. RESET_N Timing

12. Product Specifications

12.1. Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter		Min.	Max.	Unit
V _{BAT}	Supply Voltage from Battery		-0.5	6.0	V
V _{BUS_IN}	Supply Voltage from USB Connector		-0.5	28.0	V
V _{DDIO}	Supply Voltage from Baseband		-0.5	6.0	V
V _{SW}	Switch I/O Voltage	USB	-1.0	6.0	V
		UART	-1.0	6.0	
V _{IO}	I/O Voltage	I2C_SDA, I2C_SCL, INT_N, GPO1, GPO2, RESET_N	-0.3	V _{DDIO} + 0.3	V
		JIG, DETBAT_N, ON_KEY_N	-0.3	V _{BAT} + 0.3	V
I _{IK}	Input Clamp Diode Current		-50		mA
I _{SW}	Switch I/O Current (Continuous)	USB at T _A =85°C		25	mA
		UART at T _A =85°C		12	
I _{SWPEAK}	Peak Switch Current (Pulsed at 1ms Duration, <10% Duty Cycle)			150	mA
T _{STG}	Storage Temperature Range		-65	+150	°C
T _J	Maximum Junction Temperature			+150	°C
T _L	Lead Temperature (Soldering, 10 Seconds)			+260	°C
ESD	IEC 61000-4-2 System	USB Connector Pins (DP_CON, DM_CON, V _{BUS_IN} , ID_CON) to GND	Air Gap	15.0	kV
			Contact	8.0	
	Human Body Model, JEDEC JESD22-A114		USB Pins	4.0	
	Charged Device Model, JEDEC JESD22-C101		All Others	2.0	
Surge	IEC 61000-4-5 Surge Test ⁽¹⁰⁾		All Pins	1.5	V
			V _{BUS_IN}	24	
			DP_CON/DM_CON	10	

Note:

10. Modified voltage requirements: voltage impulse into an open-circuit with a 1.2 μs ramp-up rate and a 50 μs ramp-down rate.

12.2. Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter		Min.	Typ.	Max.	Unit
V _{BAT}	Battery Supply Voltage		2.7		4.4	V
V _{BUSIN_DET}	V _{BUS_IN} Voltage for Valid Detection		4.0	5.0	6.0	V
V _{BUSIN_CHG}	V _{BUS_IN} Voltage for Valid Charging		4.35	5.00	6.00	V
V _{BUS-VBAT}	V _{BUS_IN} – V _{BAT} Voltage for Valid Charging		200			mV
V _{DDIO}	I/O Supply Voltage		1.6	1.8	3.6	V
V _{SW}	Switch I/O Voltage	USB Path Active	0		3.6	V
		UART Path Active	0		3.6	
ID _{CAP}	Capacitive Load on ID_CON Pin for Reliable Accessory Detection				1.0	nF
T _A	Operating Temperature		-40		+85	°C
T _J	Junction Temperature		-40		+125	°C
Θ _{JA}	Thermal Resistance Junction-to-Ambient			60		°C/W

12.3. Switch Path DC Electrical Characteristics

Unless otherwise specified, recommended T_A and T_J temperature ranges ($T_A=-40$ to $+85^\circ\text{C}$, $T_J=-40$ to $+125^\circ\text{C}$). All typical values are at $T_A=25^\circ\text{C}$ unless otherwise specified.

12.3.1. IO Specifications

Symbol	Parameter	Voltage	Conditions	Min.	Typ.	Max.	Unit
INT_N (Push-Pull)		V_{DDIO} (V)					
V_{OH}	Output High Voltage	1.6 to 3.6	$I_{OH}=-3\text{ mA}$	$0.8 \cdot V_{DDIO}$			V
V_{OL}	Output Low Voltage	1.6 to 3.6	$I_{OL}=3\text{ mA}$			$0.2 \cdot V_{DDIO}$	V
JIG, RESET_N (Open-Drain)		V_{DDIO} (V)					
V_{OL}	Output Low Voltage	1.6 to 3.6	$I_{OL}=3\text{ mA}$			$0.2 \cdot V_{DDIO}$	V
RESET_N Generation		V_{BAT} (V)					
V_{RSTN}	V_{DDIO} Threshold for Generating RESET_N Output	3.0 to 4.4			$0.2 \cdot V_{BAT}$		V
t_{RSTN}	RESET_N Active Timeout Period; from $V_{DDIO} \geq 1.4\text{ V}$ to RESET_N=HIGH ⁽¹¹⁾	3.0 to 4.4	RST_TO=00	200	250	300	ms
General-Purpose Outputs (GPO1 and GPO2)		V_{DDIO} (V)					
V_{OH}	Output High Voltage, GPO [GPOx_OD]=0	1.6 to 3.6	$I_{OH}=-3\text{ mA}$	$0.8 \cdot V_{DDIO}$			V
V_{OL}	Output Low Voltage, GPO [GPOx_OD]=X	1.6 to 3.6	$I_{OL}=3\text{ mA}$			$0.2 \cdot V_{DDIO}$	V
Comparator Input (ON_KEY_N)		V_{BAT} (V)					
V_{IH}	High-Level Input Voltage	3.0 to 4.4		1.1			V
V_{IL}	Low-Level Input Voltage	3.0 to 4.4				0.4	V
I²C Interface Pins – Fast Mode (I2C_SDA, I2C_SCL)		V_{DDIO} (V)					
V_{IL}	Low-Level Input Voltage	1.6 to 3.6				$0.3 \cdot V_{DDIO}$	V
V_{IH}	High-Level Input Voltage	1.6 to 3.6		$0.7 \cdot V_{DDIO}$			V
V_{HYS}	Hysteresis of Schmitt Trigger Inputs	1.6 to 3.6	$V_{DDIO} > 2\text{ V}$	$0.05 \cdot V_{DDIO}$			V
			$V_{DDIO} < 2\text{ V}$	$0.1 \cdot V_{DDIO}$			V
I_{I2C}	Input Current of I2C_SDA and I2C_SCL Pins	1.6 to 3.6	Input Voltage 0.26 V to 2.34 V	-10		10	μA
V_{OL1}	Low-Level Output Voltage at 3 mA Sink Current (Open-Drain)	3.0 to 4.4	$V_{DDIO} > 2\text{ V}$	0		0.4	V
			$V_{DDIO} < 2\text{ V}$			$0.2 V_{DDIO}$	V

12.4. Switches

Symbol	Parameter	V _{BAT} (V)	Conditions	T _A =-40 to +85°C, T _J =-40 to +125°C			Unit
				Min.	Typ.	Max.	
I _{OFF}	Power-Off Leakage Current	0	All Data Ports, V _{SW} =1 V to 4.4 V			10	μA
I _{NO(OFF)}	Off Leakage Current	4.4	I/O pins=0.3 V, 4.1 V, or Floating	-0.100	0.006	0.100	μA
I _{IDSHRT}	Short Circuit Current ⁽¹¹⁾	3.0 to 4.4	Current Limit if ID_CON=0 V		20		μA
USB Switch ON Path							
USB Analog Signal Range		3.0 to 4.4		0		3.6	V
R _{ONUSB}	USB Switch On Resistance ⁽¹²⁾	3.0 to 4.4	HS-USB V _{D+/D-} =0 V, 0.4 V, I _{ON} =8 mA,		8.0	16.0	Ω
			FS-USB V _{SW} =0 V, 3.6 V, I _{ON} =24 mA		11.5	19.0	
UART Switch ON Paths							
V _{AR}	Analog Signal Range	3.0 to 4.4		0		3.6	V
R _{ONUART}	UART Switch On Resistance ⁽¹²⁾	3.0 to 4.4	HS-USB V _{D+/D-} =0 V, 0.4 V, I _{ON} =8 mA		8.0	16.0	Ω
			FS-USB V _{SW} =0 V, 3.6 V, I _{ON} =24 mA		11.5	19.0	
ON_BT_UP to V2_3 Switch and COLMx to ROWx Switch Characteristics							
R _{ONMISC}	Switch On Resistance ⁽¹²⁾	3.0 to 4.4	V _{SW} =0V to 4.4 V, I _{ON} =1 mA		36		Ω

Notes:

11. Limits based on electrical characterization data.

12. On resistance is the voltage drop between the two terminals at the indicated current through the switch.

12.5. LDOs

Symbol	Parameter	V _{BAT} (V)	Conditions	T _A =-40 to +85°C, T _J =-40 to +125°C			Unit
				Min.	Typ.	Max.	
V _{LDO}	LDO Output Voltage Programmable Range	3.0 to 4.4	I _{LDO} =300 mA	1.8		3.6	V
V _{STEP}	LDO Voltage Steps	3.0 to 4.4	See LDOx_Ctrl [LDOx_Voltage] for Exact Values		100		mV
V _{DROP}	Dropout Voltage	3.0 to 4.4	I _{LDO} =300 mA		250		mV
I _{LDMIN}	Minimum Output Current	3.0 to 4.4		0			mA
I _{LDO MAX}	Maximum Output Current	3.0 to 4.4		300			mA
d _{VLDOR}	Output Voltage Accuracy	3.0 to 4.4	Over Range of LDO Output Voltage at T _A =25°C	-2.0		2.0	%
d _{VLD OF}	Output Voltage Accuracy Over Full Range	3.0 to 4.4	Over Range of LDO Output Voltage	-3.0		3.0	%
d _{LINE}	Line Regulation ⁽¹³⁾	See Conditions	V _{BAT} =V _{LDO1(NOM)} +0.5 V to 3.6 V, I _{LDO} =1 mA		0.15	3.00	%/V
d _{LOAD}	Load Regulation ⁽¹³⁾	3.8	I _{LDO} =1 mA to 300 mA		12	70	μV/mA
I _{LDO_SC}	Maximum Current Limit	3.0 to 4.4	Short-Circuit Current Limit or Startup Peak Current		620	900	mA
PSRR	Power Supply Rejection Ratio ⁽¹³⁾	3.0 to 4.4	f=1 kHz		50		dB
e _N	Output Noise Voltage ⁽¹³⁾	3.0 to 4.4	f=10 Hz to 100 kHz		100		μV _{RMS}
t _{ON}	Turn-On Time	3.0 to 4.4	From LDOx_EN I ² C Command to Start Ramp, GPO[REF_EN]=1		100		μs

Continued on the following page...

Symbol	Parameter	V _{BAT} (V)	Conditions	T _A =-40 to +85°C, T _J =-40 to +125°C			Unit
				Min.	Typ.	Max.	
V _{OST}	Startup Overshoot ⁽¹³⁾	3.0 to 4.4	I _{LDO} =1 mA		0		%
PKV _{LINE}	Line Transient Response ⁽¹³⁾	3.0 to 4.4	600 mV, Rise=Fall=30 μs		±85		mV
PKV _{LOAD}	Load Transient Response ⁽¹³⁾	3.0 to 4.4	I _{LDO} =1-300 mA-1 mA, Rise=Fall=1 μs		±200		mV
V _{REF}	Reference Output Voltage for Internal Use	3.0 to 4.4	I _{REF} <1 μA		0.6		V
R _{DSCHG}	Discharge Programmable Turn-On Resistor	3.0 to 4.4	LDOx_ctrl [LDOx_DSCHG]=1		100		Ω
			LDOx_ctrl [LDOx_DSCHG]=0	3.4	4.8		MΩ
T _{SHTDN}	Thermal Shutdown Temperature ⁽¹³⁾	3.0 to 4.4			148		°C
			Hysteresis		12		°C

Note:

13. Limits based on electrical characterization data.

12.6. Power Path

Symbol	Parameter		T _A =-40 to +85°C, T _J =-40 to +125°C			Unit
			Min.	Typ.	Max.	
V _{BUS_REG}	V _{BUS_IN} Threshold for Active V _{BUS_IN} Regulation		4.1	4.3	4.7	V
V _{BUSVTR}	V _{BUS_IN} Valid Rising Threshold for Charging when V _{BUS_IN} Regulation is Disabled		3.4	3.7	4.0	V
V _{BUSVTF}	V _{BUS_IN} Valid Falling Threshold for Charging when V _{BUS_IN} Regulation is Disabled			3.6		V
V _{BUSOVP}	V _{BUS_IN} Over-Voltage Protection (Programmable OVP = 7.0 V)		6.5	7.0	7.6	V
	Hysteresis (Programmable OVP = 7.0 V)			150		mV
I _{VBUS}	V _{BUS_IN} Current	V _{BUS} =5.5 V, Charger Ctrl1[Charger_EN]=0, LDO1_Ctrl[LDO1_EN]=0, LDO2_Ctrl[LDO2_EN]=0			1000	μA

12.7. Linear Charger

Symbol	Parameter	Conditions	T _A =-40 to +85°C, T _J =-40 to +125°C			Unit
			Min.	Typ.	Max.	
V _{OREG}	Constant Voltage Regulation Accuracy	T _A =25°C	-1.0		1.0	%
		T _A =-40°C to 85°C	-2.0		2.0	%
	Constant Voltage Regulation Range		4.00		4.35	V
I _{SHORT}	Pre-Charge Accuracy		-15		15	%
	Pre-Charge Current		65		98	mA
V _{SHORT}	Pre-Charge Termination Voltage	V _{BAT} Rising	2.2	2.5	2.8	V
	Pre-Charge Hysteresis			150		mV
t _{OCHG}	Soft-Start Ramp Time	Pre-qualified Current of 90 mA to Fast Charge Current		1.2		ms
I _{CHARGE}	Fast Charge Current at Low Current	Charger Ctrl3[Auto_FC]=0	80	92	108	mA
	Fast Charge Current Accuracy		-10		10	%
	Fast Charge Current Range	Charger Ctrl3[Auto_FC]=1 Charger Ctrl3[FC_Current] Bit's Control Current	200		950	mA

Symbol	Parameter	Conditions	T _A =-40 to +85°C, T _J =-40 to +125°C			Unit
			Min.	Typ.	Max.	
I _{TERM}	End of Charge Current Accuracy Based on Fast Charge Current setting	EOC>120 mA	-1		1	%
V _{TERM}	Recharge Threshold, V _{BAT} – V _{OREG}	Charger Ctrl1[Recharge]=1		-150		mV
t _{TERM}	Recharge Debounce Time	Charger Ctrl1[Recharge]=1		60		ms
t _{ACC}	Timer Tolerance		-10		+10	%
t _{TOPOFF}	Top-Off Timer	Charger Ctrl2[TopOff_EN]=1		30		min
t _{DBP}	Dead-Battery Provision Timer	Charger Ctrl1[DBP_EN]=1		30	45	min
t _{ELAPSED}	Total Elapsed Charging Time	Charger Ctrl2[TC_Time]=00		5		hrs
		TC_Time=01		6		hrs
		TC_Time=10		7		hrs
		TC_Time=11		Disabled		
V _{WB}	Weak-Battery Threshold	Charger Ctrl2[WB_Threshold]=001	2.5	2.7	2.9	V
		Charger Ctrl2[WB_Threshold]=010	2.7	2.9	3.1	
		Charger Ctrl2[WB_Threshold]=011 (Default Setting)	2.9	3.1	3.3	
		Charger Ctrl2[WB_Threshold]=100	3.1	3.3	3.5	
		Charger Ctrl2[WB_Threshold]=101	3.3	3.5	3.7	
		Charger Ctrl2[WB_Threshold]=110	3.5	3.7	3.9	
T _{SHUTDOWN}	Thermal Shutdown ⁽¹⁴⁾			145		°C
	Hysteresis ⁽¹⁴⁾			5		°C
T _{REG}	Thermal Regulation ⁽¹⁴⁾			120		°C
R _{VICHG}	VICHG Internal Resistance			15		kΩ
I _{VICHG}	VBUS Current-to-Voltage Translation for VICHG	I _{BAT} =50 mA		88		mV
		I _{BAT} =500 mA		875		mV

Note:

14. Limits based on electrical characterization data.

12.8. Current Consumption

Symbol	Parameter	V _{BAT} (V)	Conditions	T _A =-40 to +85°C			Unit
				Min.	Typ.	Max.	
I _{BATS}	Battery Supply Standby Mode Current	3.0 to 4.4	No Accessory Attached, V _{BUS} =0 V, LDO1_EN=0, LDO2_EN=0, REF_EN=0		15	25	μA
I _{BATSA}	Battery Supply Standby Mode Current with Accessory Attached	3.8	ID Not Floating, No VBUS, LDOs Off, GPOs Off, All Switches Open, Accessory Attached (Excluding Factory Modes)		30		μA
I _{BATSL}	Battery Supply Standby Mode Current with One LDO On	3.8	ID Floating, No VBUS, One LDO On (3.3 V), Other LDO Off, GPOs Off, All Switches Open, No Accessory Attached		65		μA

12.9. Timing

Symbol	Parameter	Reference Diagram	$T_A = -40$ to $+85^{\circ}\text{C}$, $T_J = -40$ to $+125^{\circ}\text{C}$			Unit
			Min.	Typ.	Max.	
t_{SW}	Time After <i>INT Mask</i> Cleared to “0” until <i>INT_N</i> Goes LOW to Signal the Interrupt after Interruptible Event while <i>INT Mask</i> Bit Set to 1	Figure 7, Figure 8		10		ms
t_{SDPDET}	Time from $V_{\text{BUS_IN}}$ Valid to USB Switches Closed for USB Standard Downstream Port	Figure 13		130		ms
t_{IDDET}	Time from ID Based Accessory Attached to <i>INT_N</i> Driven LOW			5		ms
$t_{\text{CHRG_DET}}$	Time from $V_{\text{BUS_IN}}$ Valid to USB Switches Closed for USB Charging Downstream Port (CDP)	Figure 14		170		ms
$t_{\text{VBUS_CHG}}$	Time from $V_{\text{BUS_IN}}$ Valid to Charger Active, Assuming Charger Enabled	Figure 14	150			ms
$t_{\text{CHG_EN}}$	Time from <i>Charger_EN</i> =1 to Charger Active with V_{BUS} Valid			20		ms
t_{DCD}	Time from $V_{\text{bus_valid}}$ to DCD Detection Complete, Assuming Contact	Figure 14		20		ms
$t_{\text{CHRG_FLOW}}$	Time from DCD Complete to Charger Detection Complete	Figure 14		150		ms
$t_{\text{ID_FLOW}}$	Time from DCD Complete to ID Detection Complete			200		ms
t_{JIGVBUS}	Time from $V_{\text{BUS_IN}}$ Valid to JIG LOW for Both Factory Mode Operation with $V_{\text{BUS_IN}}$ Present	Figure 15		200		ms
$t_{\text{JIGNOVBUS}}$	Time from ID Attach to JIG LOW for Factory Mode Operation without $V_{\text{BUS_IN}}$ Present	Figure 16		200		ms

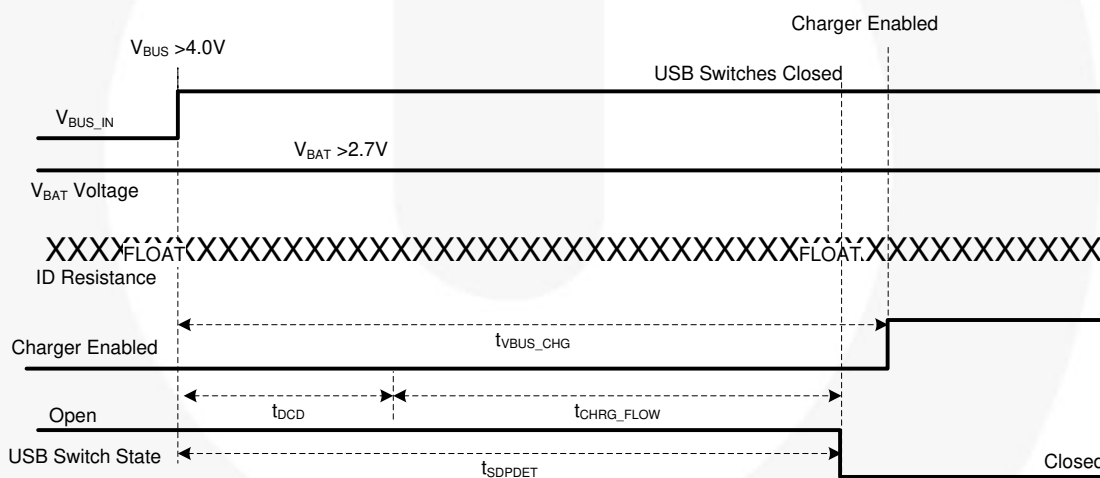


Figure 13. USB Standard Downstream Port Attach Timing

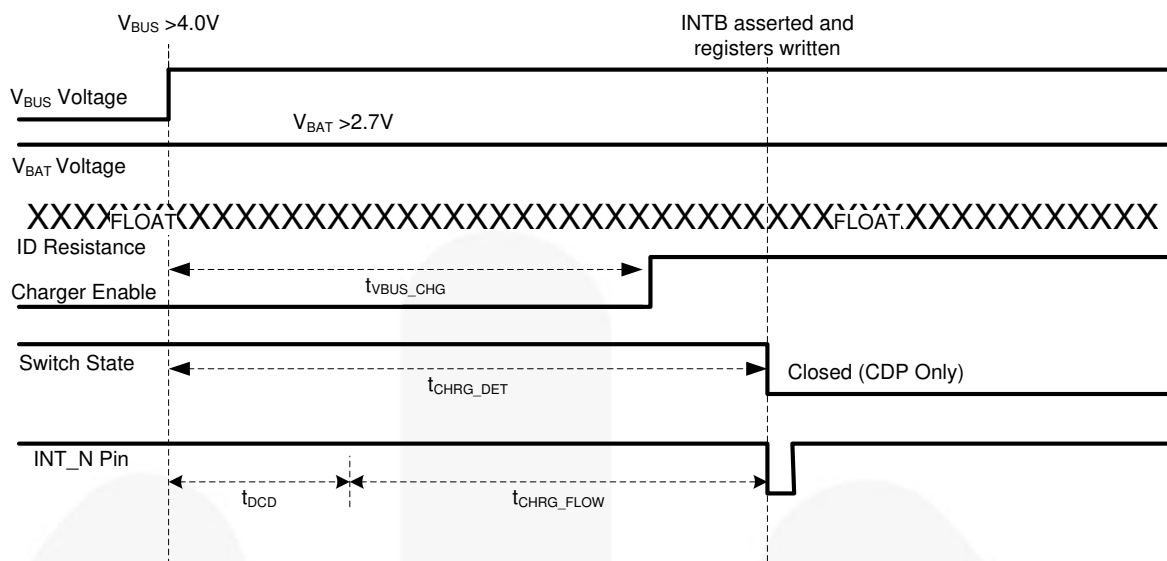


Figure 14. USB Charging Ports (DCP, CDP) Attach Timing

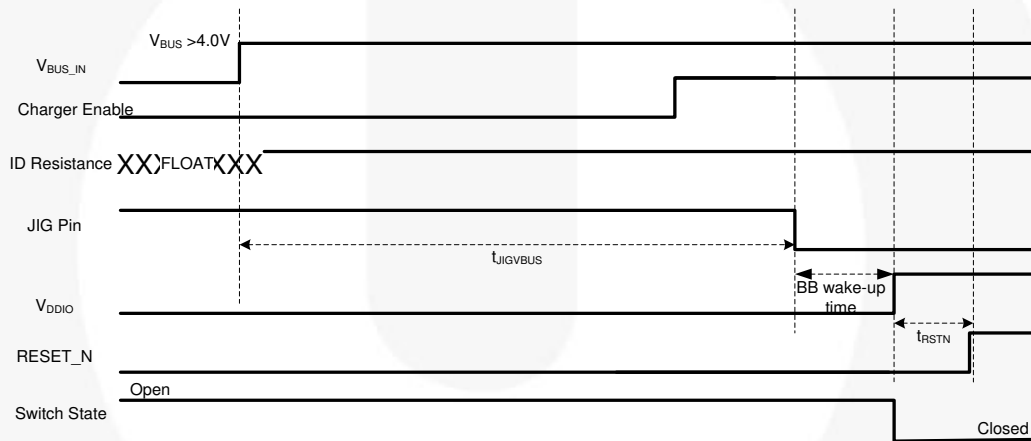


Figure 15. Jig Box Attach Timing (V_{bus_IN} Valid)



Figure 16. JIG Box Attach Timing without V_{BUS_IN}

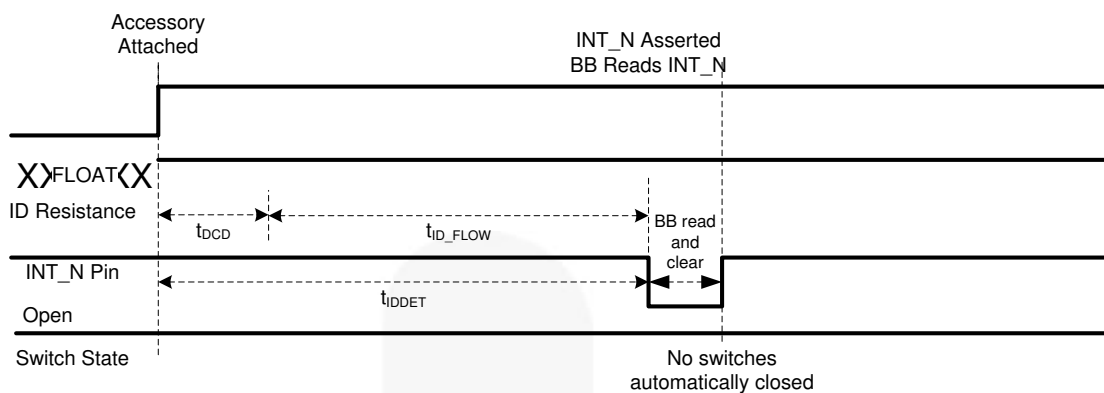


Figure 17. Unknown ID Timing

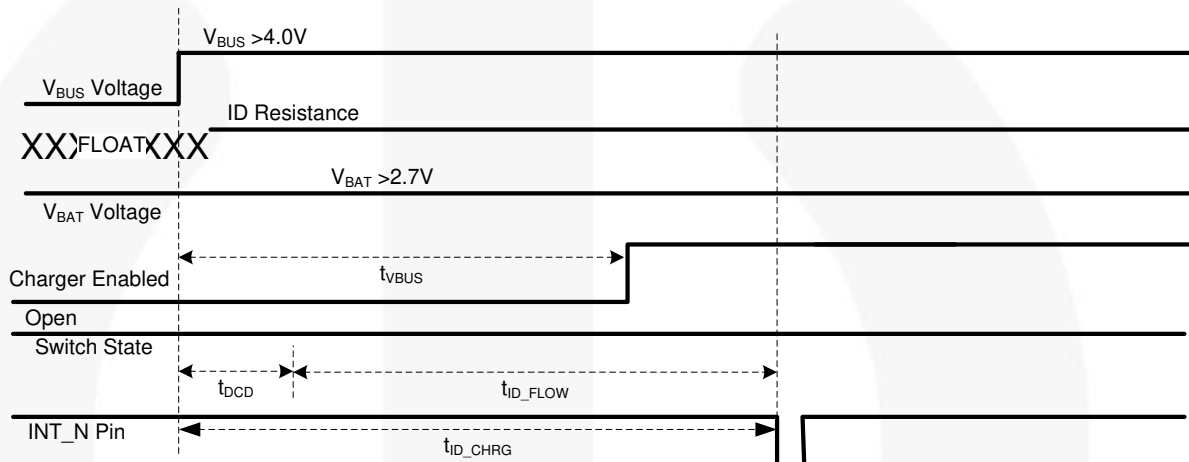


Figure 18. Car Kit Charger and TA Timing

12.10. AC Characteristics

Unless otherwise specified: recommended T_A and T_J temperature ranges. All typical values are at $T_A=25^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	$T_A=-40$ to $+85^\circ\text{C}$			Unit
			Min.	Typ.	Max.	
Xtalk	Active Channel Crosstalk DP_CON to DM_CON ⁽¹⁵⁾	$f=1\text{ MHz}$, $R_T=50\ \Omega$, $C_L=0\text{ pF}$		-60		dB
		$f=240\text{ MHz}$, $R_T=50\ \Omega$, $C_L=0\text{ pF}$		-30		
O_{IRR}	Off Isolation Rejection Ratio, DM_HOST to DM_CON, DP_HOST to DP_CON ⁽¹⁵⁾	$f=1\text{ MHz}$, $R_T=50\ \Omega$, $C_L=0\text{ pF}$		-60		dB
		$f=240\text{ MHz}$, $R_T=50\ \Omega$, $C_L=0\text{ pF}$		-30		

Note:

15. Limits based on electrical characterization data.

12.11. Capacitance

Symbol	Parameter	$V_{BAT}\text{ (V)}$	Conditions	$T_A=-40$ to $+85^\circ\text{C}$			Unit
				Min.	Typ.	Max.	
C_{ONUSB}	DP_CON, DM_CON ON Capacitance (USB Mode) ⁽¹⁶⁾	3.8	$V_{BIAS}=0.2\text{ V}$, $f=1\text{ MHz}$		8		pF
		3.8	$V_{BIAS}=0.2\text{ V}$, $f=240\text{ MHz}$		8		pF
C_I	Capacitance for Each I/O Pin ⁽¹⁶⁾	3.8	$f=1\text{ MHz}$		5		pF

Note:

16. Limits based on electrical characterization data.

12.12. I²C AC Electrical Characteristics

Symbol	Parameter	Fast Mode		Unit
		Min.	Max.	
f _{SCL}	I2C_SCL Clock Frequency	0	400	kHz
t _{HD;STA}	Hold Time (Repeated) START Condition	0.6		μs
t _{LOW}	LOW Period of I2C_SCL Clock	1.3		μs
t _{HIGH}	HIGH Period of I2C_SCL Clock	0.6		μs
t _{SU;STA}	Set-up Time for Repeated START Condition	0.6		μs
t _{HD;DAT}	Data Hold Time	0	0.9	μs
t _{SU;DAT}	Data Set-up Time ⁽¹⁷⁾	100		ns
t _r	Rise Time of I2C_SDA and I2C_SCL Signals ^(17,18)	20+0.1C _b	300	ns
t _f	Fall Time of I2C_SDA and I2C_SCL Signals ^(17,18)	20+0.1C _b	300	ns
t _{SU;STO}	Set-up Time for STOP Condition	0.6		μs
t _{BUF}	BUS-Free Time between STOP and START Conditions	1.3		μs
t _{SP}	Pulse Width of Spikes that Must Be Suppressed by the Input Filter	0	50	ns

Notes:

17. A fast-mode I²C Bus[®] device can be used in a Standard-Mode I²C Bus system, but the requirement t_{SU;DAT} ≥ 250 ns must be met. This is automatically the case if the device does not stretch the LOW period of the I2C_SCL signal. If a device does stretch the LOW period of the I2C_SCL signal, it must output the next data bit to the I2C_SDA line t_{r,max} + t_{SU;DAT} = 1000 + 250 = 1250 ns (according to the Standard-Mode I²C bus specification) before the I2C_SCL line is released.
18. C_b equals the total capacitance of one bus line in pF. If mixed with high-speed devices, faster fall times are allowed by the I²C specification.

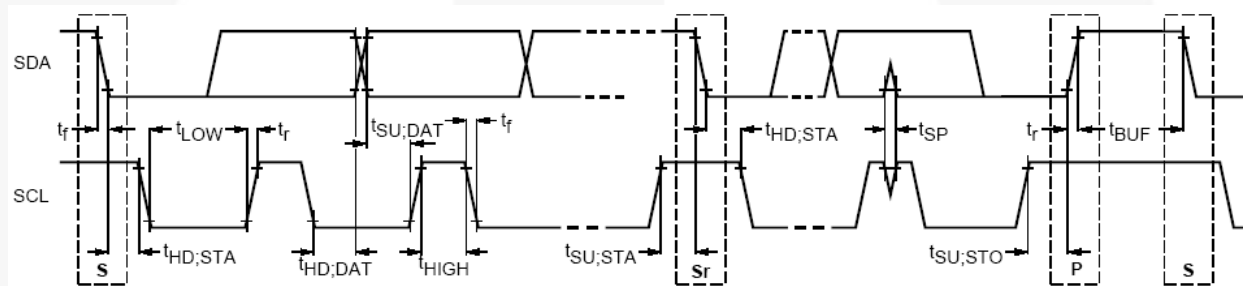


Figure 19. Definition of Timing for Full-Speed Mode Devices on the I2C Bus[®]

Table 9. I²C Slave Address

Name	Size (Bits)	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Slave Address	8	0	1	0	0	1	0	1	R/W