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Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China



# NC7SBU3157, FSAU3157

## Low-Voltage SPDT Analog Switch or 2:1 Multiplexer / De-multiplexer Bus Switch

### Features

- Analog and digital applications
- Space-saving, SC70 6-lead, surface-mount package
- Low on resistance: <math><10\Omega</math> on typical at 3.3V  $V_{CC}$
- Broad  $V_{CC}$  operating range: 1.65V to 5.5V
- Rail-to-rail signal handling
- Power-down, high-impedance control input
- Over-voltage tolerance of control input to 7.0V
- Break-before-make enable circuitry
- 250 MHz, 3dB bandwidth

### General Description

The NC7SBU3157 / FSAU3157 is a high-performance, single-pole / double-throw (SPDT) analog switch or 2:1 multiplexer / de-multiplexer bus switch.

The device is fabricated with advanced sub-micron CMOS technology to achieve high-speed enable and disable times and low on resistance. The break-before-make select circuitry prevents disruption of signals on the B port due to both switches temporarily being enabled during select pin switching. The device is specified to operate over the 1.65 to 5.5V  $V_{CC}$  operating range. The control input tolerates voltages up to 5.5V, independent of the  $V_{CC}$  operating range.

Fairchild's integrated Undershoot Hardened Circuit (UHC®) senses undershoot at the I/Os, and responds by preventing voltage differentials from developing and turning the switch on.

### Ordering Information

Part Number	Top Mark	Operating Temperature Range	Package Description	Packing Method
NC7SBU3157P6X	B7A	-40 to +85°C	6-Lead, SC70, EIAJ SC88, 1.25mm Wide Package	3000 Units Tape and Reel
FSAU3157P6X	B7A	-40 to +85°C	6-Lead, SC70, EIAJ SC88, 1.25mm Wide Package	3000 Units Tape and Reel



All packages are lead free per JEDEC: J-STD-020B standard.

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### Logic Symbol

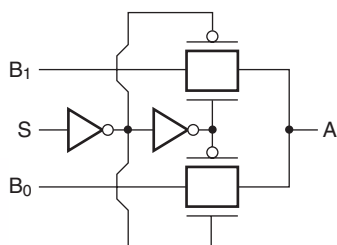
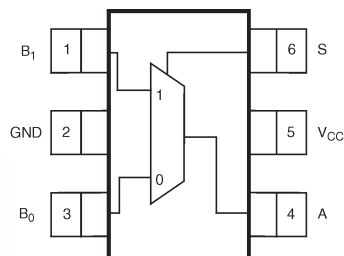


Figure 1. Logic Symbol

### Connection Diagrams



2. Pin Assignments SC70

### Analog Symbol

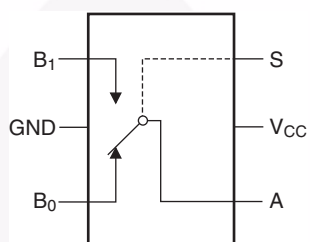


Figure 3. Analog Symbol

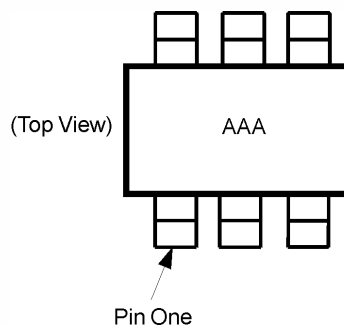


Figure 4. Pin One Orientation

*Note:*

Orientation of top mark determines pin one location. Read the top mark left to right and pin one is the lower left pin (see Figure 4).

### Function Table

Input (S)	Function
Logic Level Low	B <sub>0</sub> Connected to A
Logic Level High	B <sub>1</sub> Connected to A

### Pin Descriptions

Pin Names	Description
A, B <sub>0</sub> , B <sub>1</sub>	Data Ports
S	Control Input

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only

Symbol	Parameter	Min.	Max.	Units
$V_{CC}$	Supply Voltage	-0.5	+7.0	V
$V_S$	DC Switch Voltage <sup>(1)</sup>	-0.5	$V_{CC} + 0.5$	V
$V_{IN}$	DC Input Voltage <sup>(1)</sup>	-0.5	+7.0	V
$I_{IK}$	DC Input Diode Current at $V_{IN} < 0V$		-50	mA
$I_{OUT}$	DC Output Current		128	mA
$I_{CC}/I_{GND}$	DC $V_{CC}$ or Ground Current		±100	mA
$T_{STG}$	Storage Temperature Range	-65	+150	°C
$T_J$	Junction Temperature Under Bias		+150	°C
$T_L$	Junction Lead Temperature (Soldering, 10 seconds)		+260	°C
$P_D$	Power Dissipation at +85°C		180	mW

**Note:**

1. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max	Units	
$V_{CC}$	Supply Voltage Operating	1.65	5.50	V	
$V_{IN}$	Control Input Voltage <sup>(2)</sup>	0	$V_{CC}$	V	
$V_{IN}$	Switch Input Voltage <sup>(2)</sup>	0	$V_{CC}$	V	
$V_{OUT}$	Output Voltage <sup>(2)</sup>	0	$V_{CC}$	V	
$T_A$	Operating Temperature	-40	+85	°C	
$t_r, t_f$	Input Rise and Fall Time	Control Input $V_{CC}=2.3V-3.6V$	0	10	ns/V
		Control Input $V_{CC}=4.5V-5.5V$	0	5	ns/V
$\theta_{JA}$	Thermal Resistance		350	°C/W	

**Note:**

2. Control input must be held HIGH or LOW; it must not float.

## DC Electrical Characteristics

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
V <sub>IH</sub>	High Level Input Voltage		1.65 to 1.95	0.75 V <sub>CC</sub>			0.75 V <sub>CC</sub>		V
			2.3 to 5.5	0.7 V <sub>CC</sub>			0.7 V <sub>CC</sub>		
V <sub>IL</sub>	Low Level Input Voltage		1.65 to 1.95			0.25 V <sub>CC</sub>		0.25 V <sub>CC</sub>	V
			2.3 to 5.5			0.3 V <sub>CC</sub>		0.3 V <sub>CC</sub>	
I <sub>IN</sub>	Input Leakage Current	0 ≤ V <sub>IN</sub> ≤ 5.5V	0 to 5.5		±0.05	±0.1		±1	μA
I <sub>OFF</sub>	Off State Leakage Current	0 ≤ A, B ≤ V <sub>CC</sub>	1.65 to 5.5		±0.05	±0.1		±1	μA
R <sub>ON</sub>	Switch On Resistance <sup>(3)</sup>	V <sub>IN</sub> =0V, I <sub>O</sub> =30mA	4.5			3.0		15.0	Ω
		V <sub>IN</sub> =2.4V, I <sub>O</sub> =-30mA				5.0		15.0	
		V <sub>IN</sub> =4.5V, I <sub>O</sub> =-30mA				7.0		15.0	
		V <sub>IN</sub> =0V, I <sub>O</sub> =24mA	3.0			4.0		20.0	
		V <sub>IN</sub> =3V, I <sub>O</sub> =-24mA				10.0		20.0	
		V <sub>IN</sub> =0V, I <sub>O</sub> =8mA	2.3			5.0		30.0	
		V <sub>IN</sub> =2.3V, I <sub>O</sub> =-8mA				13.0		30.0	
		V <sub>IN</sub> =0V, I <sub>O</sub> =4mA	1.65			6.5		50.0	
V <sub>IN</sub> =1.65V, I <sub>O</sub> =-4mA				17.0		50.0			
I <sub>CC</sub>	Quiescent Supply Current; All Channels On or Off	V <sub>IN</sub> =V <sub>CC</sub> or GND I <sub>OUT</sub> =0	5.5			1		10	μA
	Analog Signal Range		V <sub>CC</sub>	0		V <sub>CC</sub>	0	V <sub>CC</sub>	V
R <sub>RANGE</sub>	On Resistance Over Signal Range <sup>(3, 7)</sup>	I <sub>A</sub> =-30mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	4.5					25.0	Ω
		I <sub>A</sub> =-24mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	3.0				50.0		
		I <sub>A</sub> =-8mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	2.3				100		
		I <sub>A</sub> =-4mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	1.65				300		
ΔR <sub>ON</sub>	On Resistance Match Between-Channels <sup>(3, 4, 5)</sup>	I <sub>A</sub> =-30mA, V <sub>Bn</sub> =3.15	4.5		0.15			Ω	
		I <sub>A</sub> =-24mA, V <sub>Bn</sub> 2.1	3.0		0.2				
		I <sub>A</sub> =-8mA, V <sub>Bn</sub> =1.6	2.3		0.5				
		I <sub>A</sub> =-4mA, V <sub>Bn</sub> =1.15	1.65		0.5				
V <sub>IKU</sub>	Voltage Under-shoot	0.0mA ≤ I <sub>IN</sub> ≤ -50, OE 5.5v	5.5					-2	V
R <sub>flat</sub>	On Resistance Flatness <sup>(3, 4, 6)</sup>	I <sub>A</sub> =-30mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	5.0		6.0			Ω	
		I <sub>A</sub> =-24mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	3.3		12.0				
		I <sub>A</sub> =-8mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	2.5		28.0				
		I <sub>A</sub> =-4mA, 0 ≤ V <sub>Bn</sub> ≤ V <sub>CC</sub>	1.8		125				

### Notes:

- Measured by the voltage drop between A and B pins at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B Ports).
- Parameter is characterized, but not tested in production.
- ΔR<sub>ON</sub> = R<sub>ON</sub> max – R<sub>ON</sub> minimum measured at identical V<sub>CC</sub>, temperature, and voltage levels.
- Flatness is defined as the difference between the maximum and minimum value of on resistance over the specified range of conditions.
- Guaranteed by design.

## AC Electrical Characteristics

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		Units	Figure
				Min.	Typ.	Max.	Min.	Max.		
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Bus-to-Bus <sup>(8)</sup>	V <sub>I</sub> = OPEN	1.65 to 1.95					ns	Figure 7 Figure 8	
			2.3 to 2.7			1.2	1.2			
			3.0 to 3.6			0.8	0.8			
			4.5 to 5.5			0.3	0.3			
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time Turn-On Time (A to B <sub>n</sub> )	V <sub>I</sub> = 2 x V <sub>CC</sub> for t <sub>PZL</sub> V <sub>I</sub> = 0V for t <sub>PZH</sub>	1.65 to 1.95	7.0		23.0	7.0	ns	Figure 7 Figure 8	
			2.3 to 2.7	3.5		13.0	3.5			14.0
			3.0 to 3.6	2.5		6.9	2.5			7.6
			4.5 to 5.5	1.7		5.2	1.7			5.7
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Output Disable Time Turn-Off Time (A Port to B Port)	V <sub>I</sub> = 2 x V <sub>CC</sub> for t <sub>PLZ</sub> V <sub>I</sub> = 0V for t <sub>PHZ</sub>	1.65 to 1.95	3.0		12.5	3.0	ns	Figure 7 Figure 8	
			2.3 to 2.7	2.0		7.0	2.0			7.5
			3.0 to 3.6	1.5		5.0	1.5			5.3
			4.5 to 5.5	0.8		3.5	0.8			3.8
t <sub>BBM</sub>	Break-Before-Make Time <sup>(9)</sup>		1.65 to 1.95	0.5		0.5		ns	Figure 9	
			2.3 to 2.7	0.5		0.5				
			3.0 to 3.6	0.5		0.5				
			4.5 to 5.5	0.5		0.5				
Q	Charge Injection <sup>(9)</sup>	C <sub>L</sub> = 0.1nF, V <sub>GEN</sub> = 0V,	5.0		7.0		pC	Figure 10		
		R <sub>GEN</sub> = 0Ω	3.3		3.0					
OIRR	Off Isolation <sup>(10)</sup>	R <sub>L</sub> = 50Ω, f = 10MHz	1.65 to 5.5		-57.0		dB	Figure 11		
Xtalk	Crosstalk	R <sub>L</sub> = 50Ω, f = 10MHz	1.65 to 5.5		-54.0		dB	Figure 12		
BW	-3dB Bandwidth	R <sub>L</sub> = 50Ω	1.65 to 5.5		250		MHz	Figure 15		
THD	Total Harmonic Distortion <sup>(9)</sup>	R <sub>L</sub> = 600Ω, 0.5V <sub>PP</sub> , f = 20Hz to 20KHz	5.0		.011		%			

### Notes:

8. This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the on resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).
9. Guaranteed by design.
10. Off Isolation = 20 log<sub>10</sub> [V<sub>A</sub> / V<sub>Bn</sub>].

## Capacitance

T<sub>A</sub> = +25°C, f = 1MHz. Capacitance is characterized, but not tested in production.

Symbol	Parameter	Conditions	Typ.	Max.	Units	Figure
C <sub>IN</sub>	Control Pin Input Capacitance	V <sub>CC</sub> = 0V	2.3		pF	
C <sub>IO-B</sub>	B Port Off Capacitance	V <sub>CC</sub> = 5.0V	6.5		pF	Figure 13
C <sub>IOA-ON</sub>	A Port Capacitance When Switch Is Enabled	V <sub>CC</sub> = 5.0V	18.5		pF	Figure 14

## Undershoot Characteristic

Symbol	Parameter	Min.	Typ.	Units	Figure
$V_{OUTU}$	Output Voltage During Undershoot	2.5	$V_{OH} - 0.3$	V	Figure 5

**Note:**

11. This test is intended to characterize the device's protective capabilities by maintaining output signal integrity during an input transient voltage undershoot event.

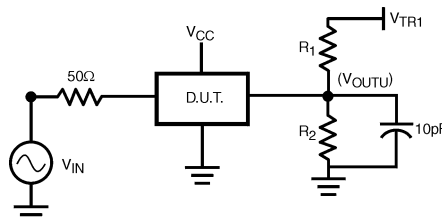


Figure 5. Output Voltage During Undershoot

## Device Test Conditions

Parameter	Value	Units
$V_{IN}$	see Figure 6	V
$R_1 = R_2$	100	K $\Omega$
$V_{TRI}$	7.0	V
$V_{CC}$	5.5	V

## Transient Input Voltage ( $V_{IN}$ ) Waveform

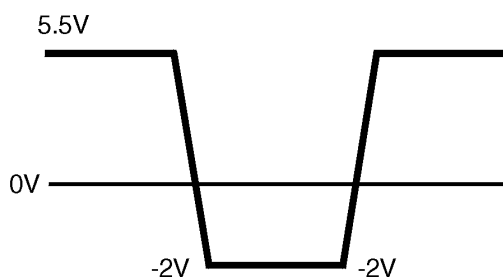
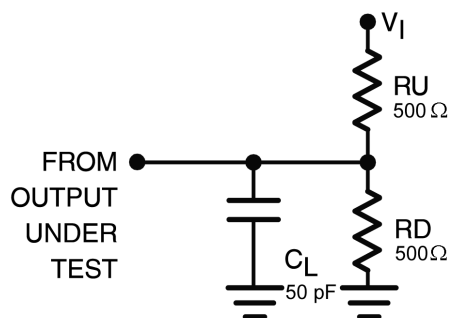


Figure 6. Transient Input Voltage Waveform

## AC Loading and Waveforms



Notes:  
 Input driven by 50Ω source terminated in 50Ω.  
 $C_L$  includes load and stray capacitance.  
 Input PRR=1.0MHz;  $t_w = 500\text{ns}$ .

Figure 7. AC Test Circuit

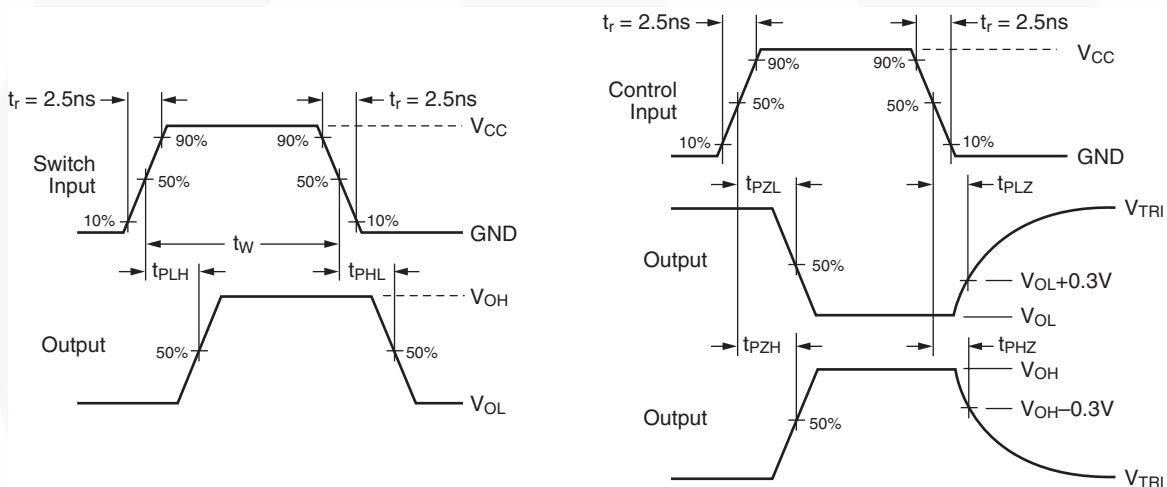


Figure 8. AC Waveforms

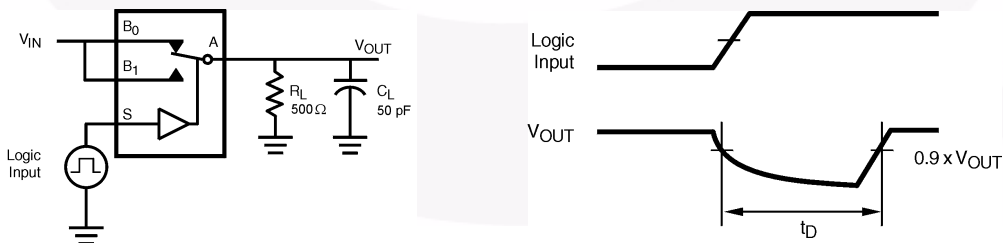
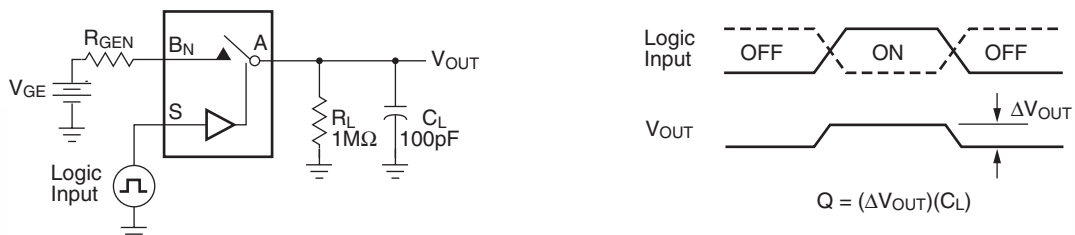


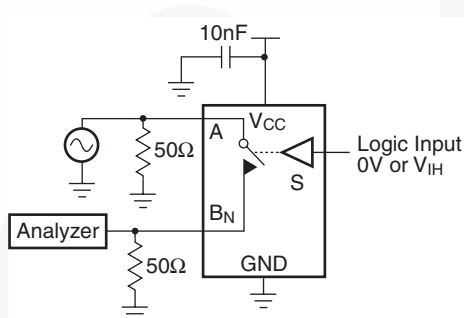
Figure 9. Break-Before-Make Interval Timing



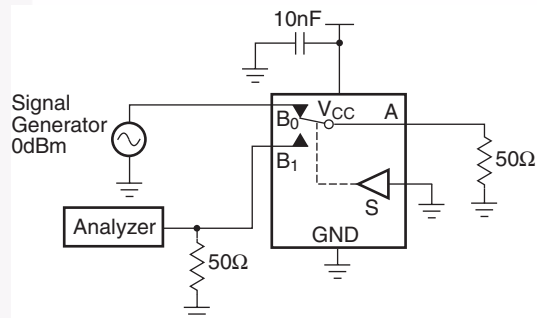
### AC Loading and Waveforms (continued)



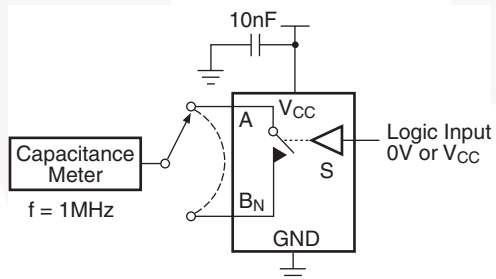
**Figure 10. Charge Injection Test**



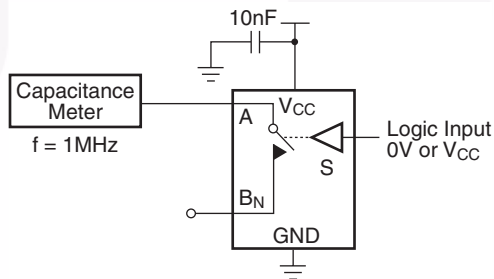
**Figure 11. Off Isolation**



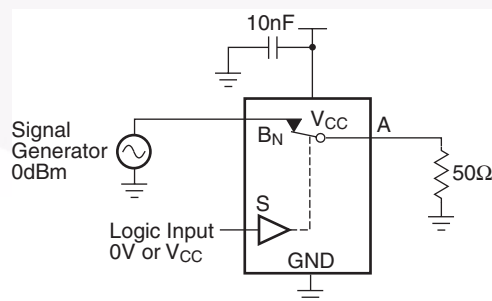
**Figure 12. Crosstalk**



**Figure 13. Channel Off Capacitance**

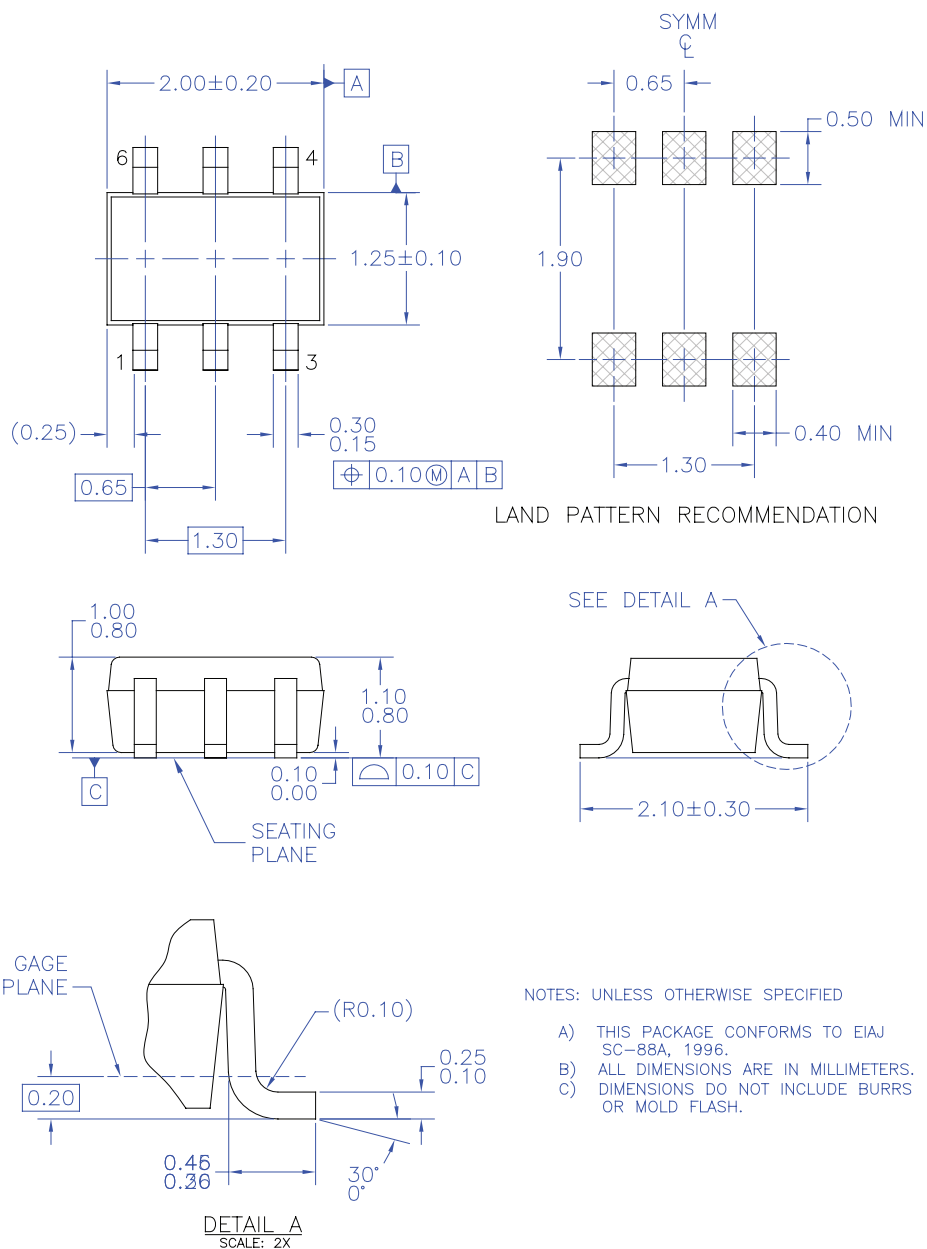


**Figure 14. Channel On Capacitance**



**Figure 15. Bandwidth**

## Physical Dimensions



MAA06AREV5

**Figure 16. 6-Lead, SC70, EIAJ SC88, 1.25mm Wide Package**

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| FACT <sup>®</sup>   | Motion-SPM <sup>™</sup>                       | SuperSOT <sup>™</sup> .6  | VCX <sup>™</sup>  |
| FAST <sup>®</sup>   | OPTOLOGIC <sup>®</sup>                        | SuperSOT <sup>™</sup> .8  | VisualMax <sup>™</sup>  |
| FastvCore <sup>™</sup>  | OPTOPLANAR <sup>®</sup>                       | SupreMOS <sup>™</sup>   |   |
| FlashWriter <sup>®</sup> *  |   | SyncFET <sup>™</sup>  |   |
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**Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	This datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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