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FAIRCHILD SEMICONDUCTOR®

February 2009

FSB50550U

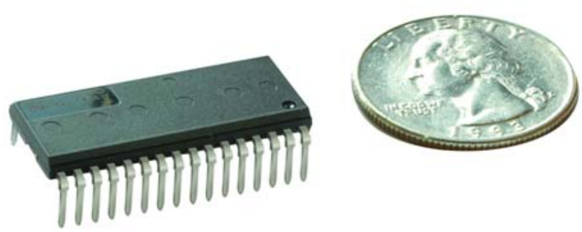
Smart Power Module (SPM®)

Features

- 500V $R_{DS(on)}$=1.4Ω(max) 3-phase FRFET inverter including high voltage integrated circuit (HVIC)
- 3 divided negative dc-link terminals for inverter current sensing applications
- HVIC for gate driving and undervoltage protection
- 3/5V CMOS/TTL compatible, active-high interface
- Optimized for low electromagnetic interference
- Isolation voltage rating of 1500Vrms for 1min.

General Description

FSB50550U is a tiny smart power module (SPM®) based on FRFET technology as a compact inverter solution for small power motor drive applications such as fan motors and water suppliers. It is composed of 6 fast-recovery MOSFET (FRFET), and 3 half-bridge HVICs for FRFET gate driving. FSB50550U provides low electromagnetic interference (EMI) characteristics with optimized switching speed. Moreover, since it employs FRFET as a power switch, it has much better ruggedness and larger safe operation area (SOA) than that of an IGBT-based power module or one-chip solution. The package is optimized for the thermal performance and compactness for the use in the built-in motor application and any other application where the assembly space is concerned. FSB50550U is the most solution for the compact inverter providing the energy efficiency, compactness, and low electromagnetic interference.



Absolute Maximum Ratings

Symbol	Parameter	Conditions	Rating	Units
V_{PN}	DC Link Input Voltage, Drain-source Voltage of each FRFET		500	V
I_{D25}	Each FRFET Drain Current, Continuous	T_C = 25°C	2.0	A
I_{D80}	Each FRFET Drain Current, Continuous	T_C = 80°C	1.5	A
I_{DP}	Each FRFET Drain Current, Peak	T_C = 25°C, PW < 100μs	5	A
P_D	Maximum Power Dissipation	T_C = 25°C, Each FRFET	14.5	W
V_{CC}	Control Supply Voltage	Applied between V_{CC} and COM	20	V
V_{BS}	High-side Bias Voltage	Applied between $V_{B(U)}$-U, $V_{B(V)}$-V, $V_{B(W)}$-W	20	V
V_{IN}	Input Signal Voltage	Applied between IN and COM	-0.3 ~ VCC+0.3	V
T_J	Operating Junction Temperature		-40 ~ 150	°C
T_{STG}	Storage Temperature		-50 ~ 150	°C
$R_{\theta JC}$	Junction to Case Thermal Resistance	Each FRFET under inverter operating condition (Note 1)	8.6	°C/W
V_{ISO}	Isolation Voltage	60Hz, Sinusoidal, 1 minute, Connection pins to heatsink	1500	V_{rms}

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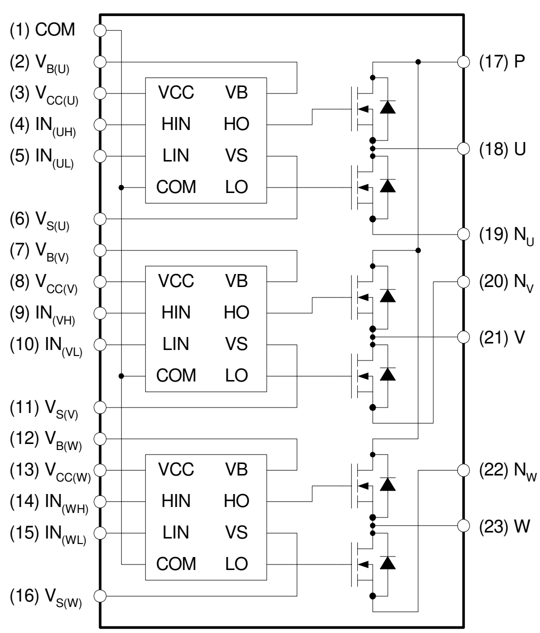
Pin Descriptions

Pin Number	Pin Name	Pin Description
1	COM	IC Common Supply Ground
2	$V_{B(U)}$	Bias Voltage for U Phase High Side FRFET Driving
3	$V_{CC(U)}$	Bias Voltage for U Phase IC and Low Side FRFET Driving
4	$IN_{(UH)}$	Signal Input for U Phase High-side
5	$IN_{(UL)}$	Signal Input for U Phase Low-side
6	$V_{S(U)}$	Bias Voltage Ground for U Phase High Side FRFET Driving
7	$V_{B(V)}$	Bias Voltage for V Phase High Side FRFET Driving
8	$V_{CC(V)}$	Bias Voltage for V Phase IC and Low Side FRFET Driving
9	$IN_{(VH)}$	Signal Input for V Phase High-side
10	$IN_{(VL)}$	Signal Input for V Phase Low-side
11	$V_{S(V)}$	Bias Voltage Ground for V Phase High Side FRFET Driving
12	$V_{B(W)}$	Bias Voltage for W Phase High Side FRFET Driving
13	$V_{CC(W)}$	Bias Voltage for W Phase IC and Low Side FRFET Driving
14	$IN_{(WH)}$	Signal Input for W Phase High-side
15	$IN_{(WL)}$	Signal Input for W Phase Low-side
16	$V_{S(W)}$	Bias Voltage Ground for W Phase High Side FRFET Driving
17	P	Positive DC–Link Input
18	U	Output for U Phase
19	N_U	Negative DC–Link Input for U Phase
20	N_V	Negative DC–Link Input for V Phase
21	V	Output for V Phase
22	N_W	Negative DC–Link Input for W Phase
23	W	Output for W Phase



Note:
Source terminal of each low-side MOSFET is not connected to supply ground or bias voltage ground inside SPM®. External connections should be made as indicated in Figure 2 and 5.

Figure 1. Pin Configuration and Internal Block Diagram (Bottom View)

Electrical Characteristics (T_J = 25°C, V_{CC}=V_{BS}=15V Unless Otherwise Specified)

Inverter Part (Each FRFET Unless Otherwise Specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
BV_{DSS}	Drain-Source Breakdown Voltage	V_{IN}= 0V, I_D = 250μA (Note 2)	500	-	-	V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250μA, Referenced to 25°C	-	0.53	-	V
I_{DSS}	Zero Gate Voltage Drain Current	V_{IN}= 0V, V_{DS} = 500V	-	-	250	μA
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{CC} = V_{BS} = 15V, V_{IN} = 5V, I_D = 1.2A	-	1.0	1.4	Ω
V_{SD}	Drain-Source Diode Forward Voltage	V_{CC} = V_{BS} = 15V, V_{IN} = 0V, I_D = -1.2A	-	-	1.2	V
t_{ON}	Switching Times	V_{PN} = 300V, V_{CC} = V_{BS} = 15V, I_D = 1.2A V_{IN} = 0V ↔ 5V Inductive load L=3mH High- and low-side FRFET switching (Note 3)	-	600	-	ns
t_{OFF}			-	500	-	ns
t_{rr}			-	100	-	ns
E_{ON}			-	60	-	μJ
E_{OFF}			-	10	-	μJ
RBSOA	Reverse-bias Safe Operating Area	V_{PN} = 400V, V_{CC} = V_{BS} = 15V, I_D = I_{DP}, V_{DS}=BV_{DSS}, T_J = 150°C High- and low-side FRFET switching (Note 4)	Full Square			

Control Part (Each HVIC Unless Otherwise Specified)

Symbol	Parameter	Conditions		Min	Typ	Max	Units
I_{QCC}	Quiescent V_{CC} Current	V_{CC}=15V, V_{IN}=0V	Applied between V_{CC} and COM	-	-	160	μA
I_{QBS}	Quiescent V_{BS} Current	V_{BS}=15V, V_{IN}=0V	Applied between $V_{B(U)}$-U, $V_{B(V)}$-V, $V_{B(W)}$-W	-	-	100	μA
UV_{CCD}	Low-side Undervoltage Protection (Figure 6)	V_{CC} Undervoltage Protection Detection Level		7.4	8.0	9.4	V
UV_{CCR}		V_{CC} Undervoltage Protection Reset Level		8.0	8.9	9.8	V
UV_{BSD}	High-side Undervoltage Protection (Figure 7)	V_{BS} Undervoltage Protection Detection Level		7.4	8.0	9.4	V
UV_{BSR}		V_{BS} Undervoltage Protection Reset Level		8.0	8.9	9.8	V
V_{IH}	ON Threshold Voltage	Logic High Level	Applied between IN and COM	3.0	-	-	V
V_{IL}	OFF Threshold Voltage	Logic Low Level		-	-	0.8	V
I_{IH}	Input Bias Current	V_{IN} = 5V	Applied between IN and COM	-	10	20	μA
I_{IL}		V_{IN} = 0V		-	-	2	μA

Note:

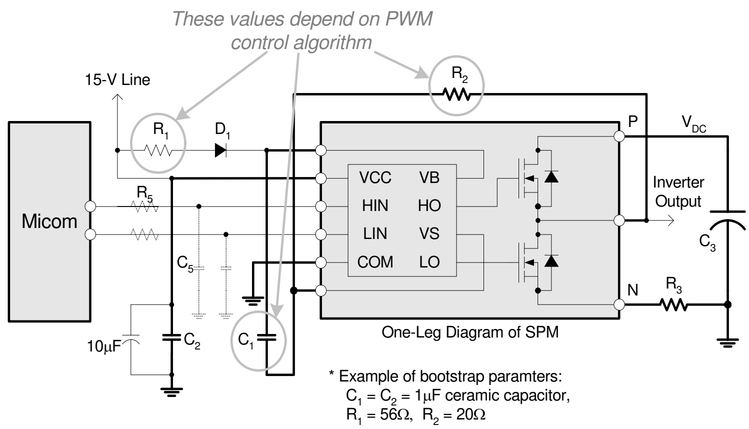
1. For the measurement point of case temperature T_C, please refer to Figure 3 in page 4.
2. BV_{DSS} is the absolute maximum voltage rating between drain and source terminal of each FRFET inside SPM®. V_{PN} should be sufficiently less than this value considering the effect of the stray inductance so that V_{DS} should not exceed BV_{DSS} in any case.
3. t_{ON} and t_{OFF} include the propagation delay time of the internal drive IC. Listed values are measured at the laboratory test condition, and they can be different according to the field applcations due to the effect of different printed circuit boards and wirings. Please see Figure 4 for the switching time definition with the switching test circuit of Figure 5.
4. The peak current and voltage of each FRFET during the switching operation should be included in the safe operating area (SOA). Please see Figure 5 for the RBSOA test circuit that is same as the switching test circuit.

Package Marking & Ordering Information

Device Marking	Device	Package	Reel Size	Packing Type	Quantity
FSB50550U	FSB50550U	SPM23-AD	_	_	15

Recommended Operating Conditions

Symbol	Parameter	Conditions	Value			Units
			Min.	Typ.	Max.	
V_{PN}	Supply Voltage	Applied between P and N	-	300	400	V
V_{CC}	Control Supply Voltage	Applied between V_{CC} and COM	13.5	15	16.5	V
V_{BS}	High-side Bias Voltage	Applied between V_B and output(U, V, W)	13.5	15	16.5	V
$V_{IN(ON)}$	Input ON Threshold Voltage	Applied between IN and COM	3.0	-	V_{CC}	V
$V_{IN(OFF)}$	Input OFF Threshold Voltage		0	-	0.6	V
t_{dead}	Blanking Time for Preventing Arm-short	V_{CC}=V_{BS}=13.5 ~ 16.5V, $T_J \leq 150°C$	1.0	-	-	µs
f_{PWM}	PWM Switching Frequency	$T_J \leq 150°C$	-	15	-	kHz



HIN	LIN	Output	Note
0	0	Z	Both FRFET Off
0	1	0	Low-side FRFET On
1	0	V_{DC}	High-side FRFET On
1	1	Forbidden	Shoot-through
Open	Open	Z	Same as (0, 0)

Note:

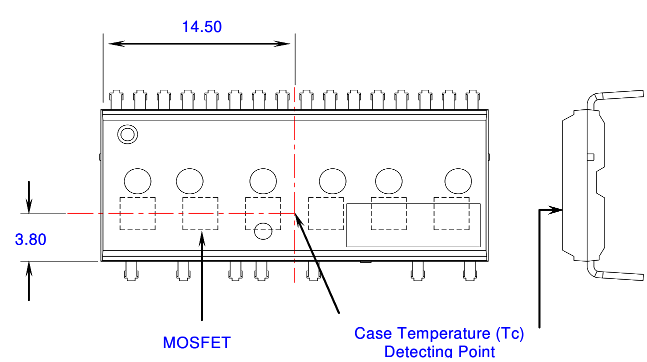
(1) It is recommended the bootstrap diode D_1 to have soft and fast recovery characteristics with 600-V rating

(2) Parameters for bootsrap circuit elements are dependent on PWM algorithm. For 15 kHz of switching frequency, typical example of parameters is shown above.

(3) RC coupling(R_5 and C_5) at each input (indicated as dotted lines) may be used to prevent improper input signal due to surge noise. Signal input of SPM®is compatible with standard CMOS or LSTTL outputs.

(4) Bold lines should be short and thick in PCB pattern to have small stray inductance of circuit, which results in the reduction of surge voltage. Bypass capacitors such as C_1, C_2 and C_3 should have good high-frequency characteristics to absorb high-frequency ripple current.

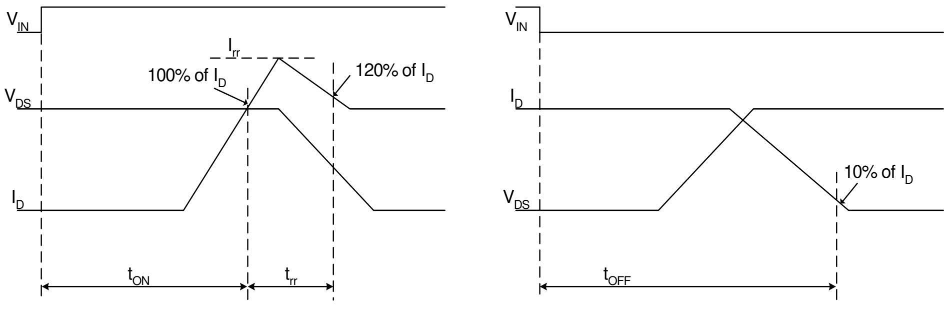
Figure 2. Recommended CPU Interface and Bootstrap Circuit with Parameters



Note:

Attach the thermocouple on top of the heatsink-side of SPM® (between SPM® and heatsink if applied) to get the correct temperature measurement.

Figure 3. Case Temperature Measurement



(a) Turn-on (b) Turn-off

Figure 4. Switching Time Definition

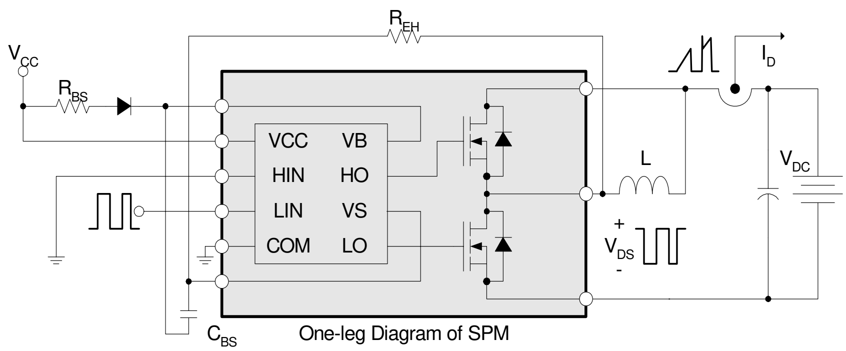


Figure 5. Switching and RBSOA(Single-pulse) Test Circuit (Low-side)

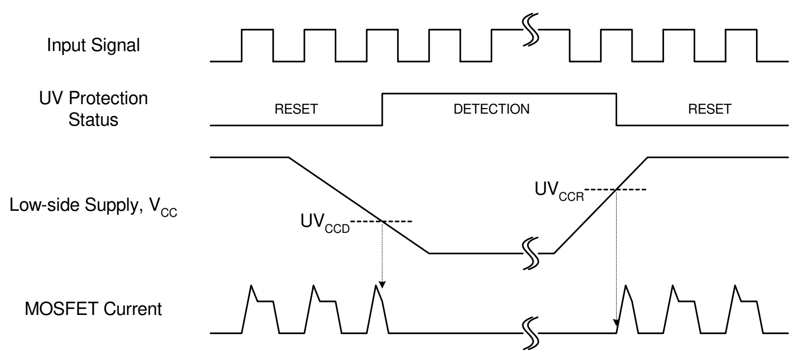


Figure 6. Undervoltage Protection (Low-side)

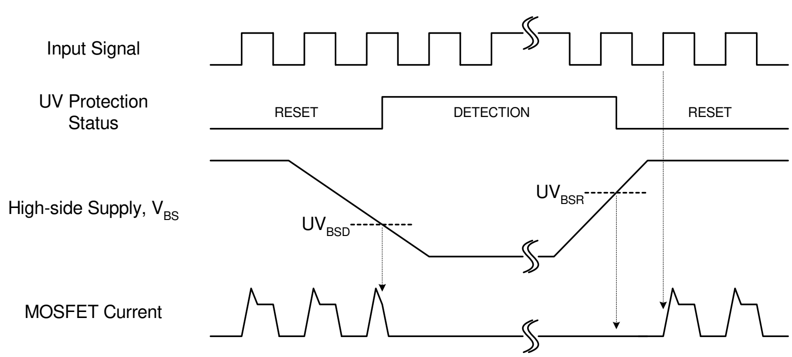


Figure 7. Undervoltage Protection (High-side)

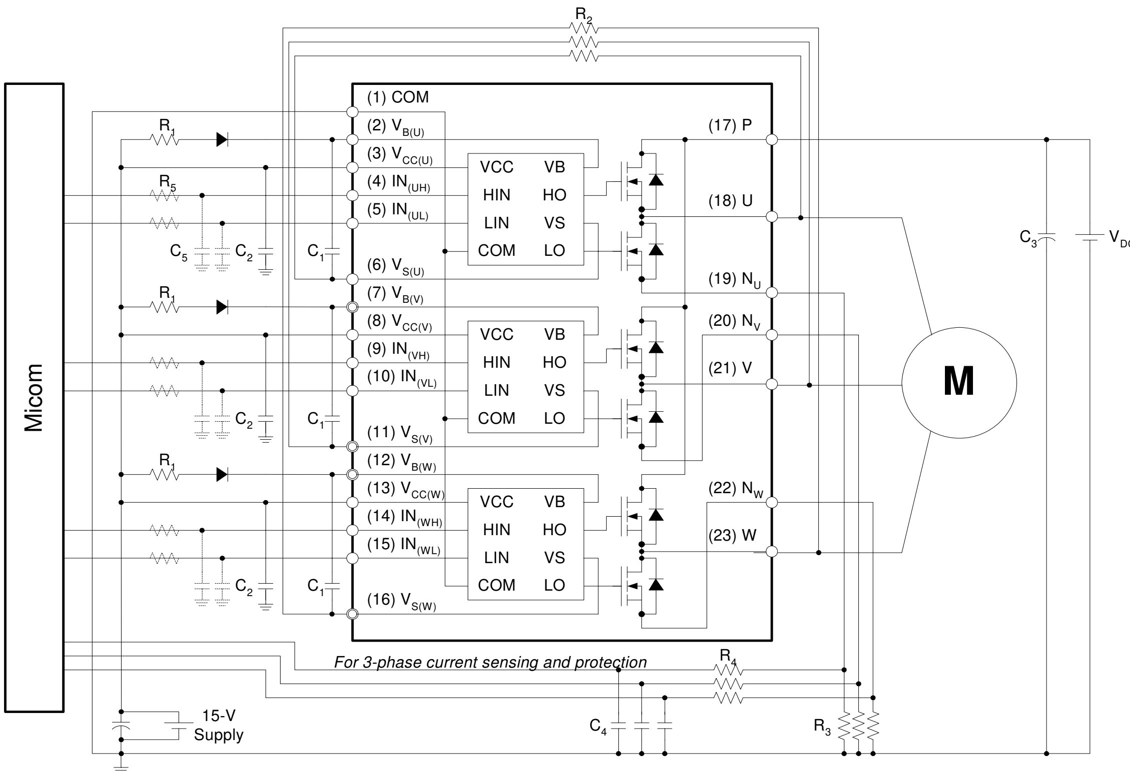
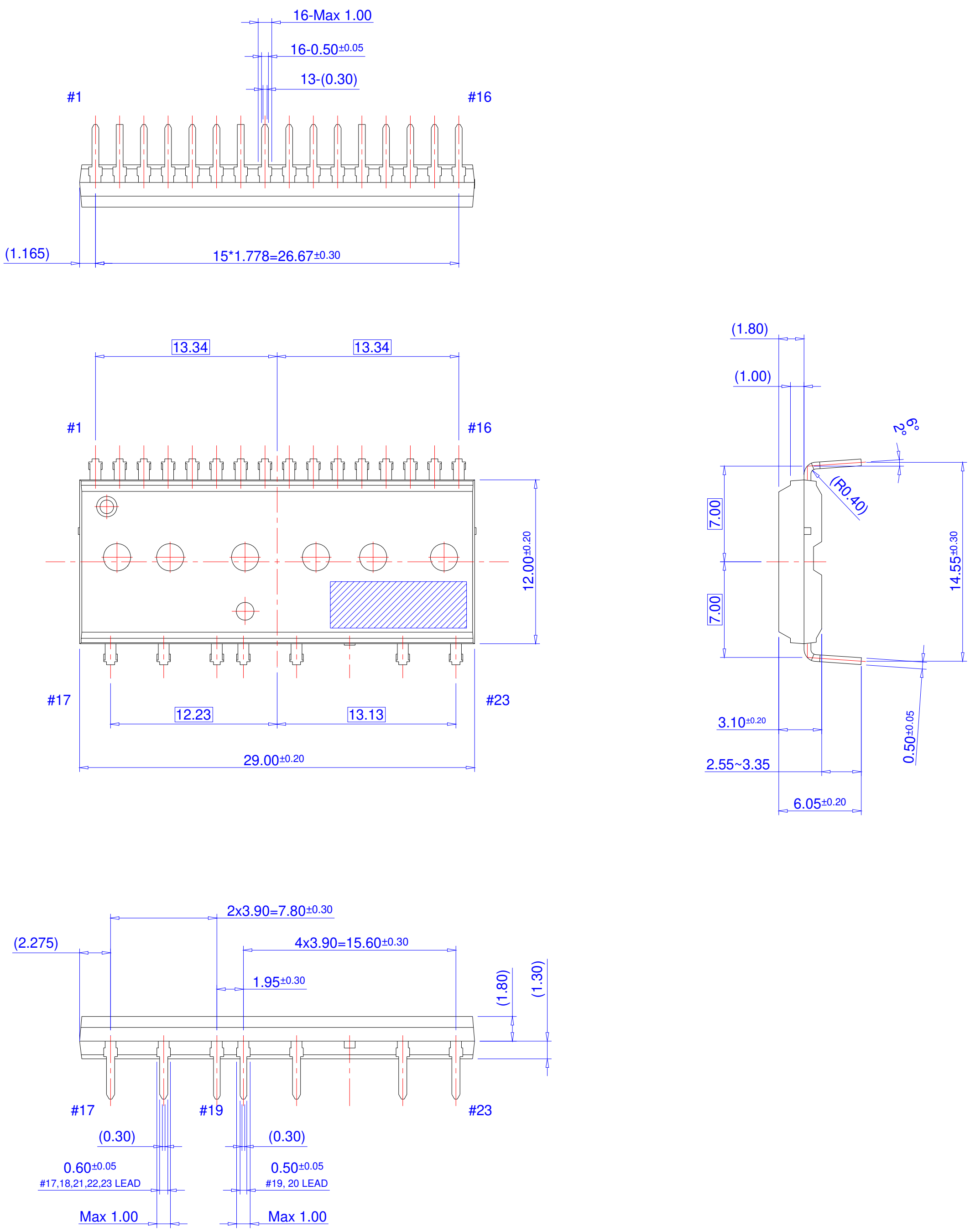


Figure 8. Example of Application Circuit

Detailed Package Outline Drawings



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