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FAIRCHILD
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June 2007

Motion-SPM™

# FSBB15CH60B
# Smart Power Module

## Features

- UL Certified No.E209204(SPM27-CC package)
- Very low thermal resistance due to using DBC
- Easy PCB layout due to built in bootstrap diode
- 600V-15A 3-phase IGBT inverter bridge including control ICs for gate driving and protection
- Divided negative dc-link terminals for inverter current sensing applications
- Single-grounded power supply due to built-in HVIC
- Isolation rating of 2500Vrms/min.

## Applications

- AC 100V ~ 253V three-phase inverter drive for small power ac motor drives
- Home appliances applications like air conditioner and washing machine

## General Description

It is an advanced motion-smart power module (Motion-SPM™) that Fairchild has newly developed and designed to provide very compact and high performance ac motor drives mainly targeting low-power inverter-driven application like air conditioner and washing machine. It combines optimized circuit protection and drive matched to low-loss IGBTs. System reliability is further enhanced by the integrated under-voltage lock-out and short-circuit protection. The high speed built-in HVIC provides opto-coupler-less single-supply IGBT gate driving capability that further reduce the overall size of the inverter system design. Each phase current of inverter can be monitored separately due to the divided negative dc terminals.

**Top View** **Bottom View**

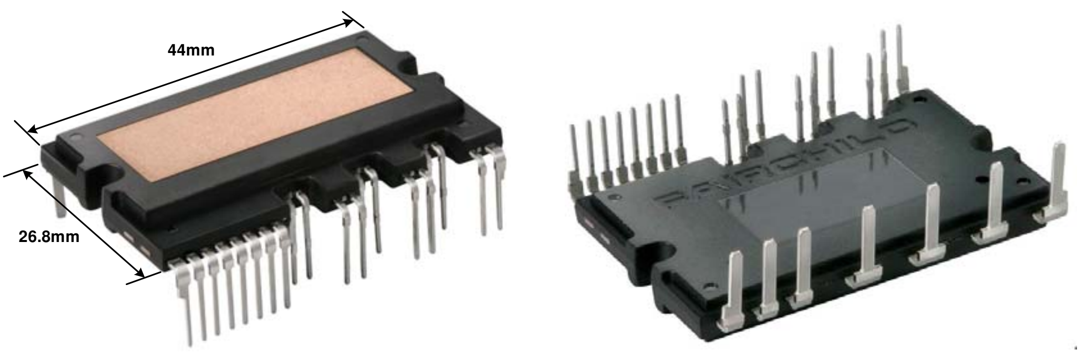



**Figure 1.**

## Integrated Power Functions

- 600V-15A IGBT inverter for three-phase DC/AC power conversion (Please refer to Figure 3)

## Integrated Drive, Protection and System Control Functions

- For inverter high-side IGBTs: Gate drive circuit, High voltage isolated high-speed level shifting
  Control circuit under-voltage (UV) protection
  Note) Available bootstrap circuit example is given in Figures 12 and 13.
- For inverter low-side IGBTs: Gate drive circuit, Short circuit protection (SC)
  Control supply circuit under-voltage (UV) protection
- Fault signaling: Corresponding to UV (Low-side supply) and SC faults
- Input interface: 3.3/5V CMOS/LSTTL compatible, Schmitt trigger input

## Pin Configuration

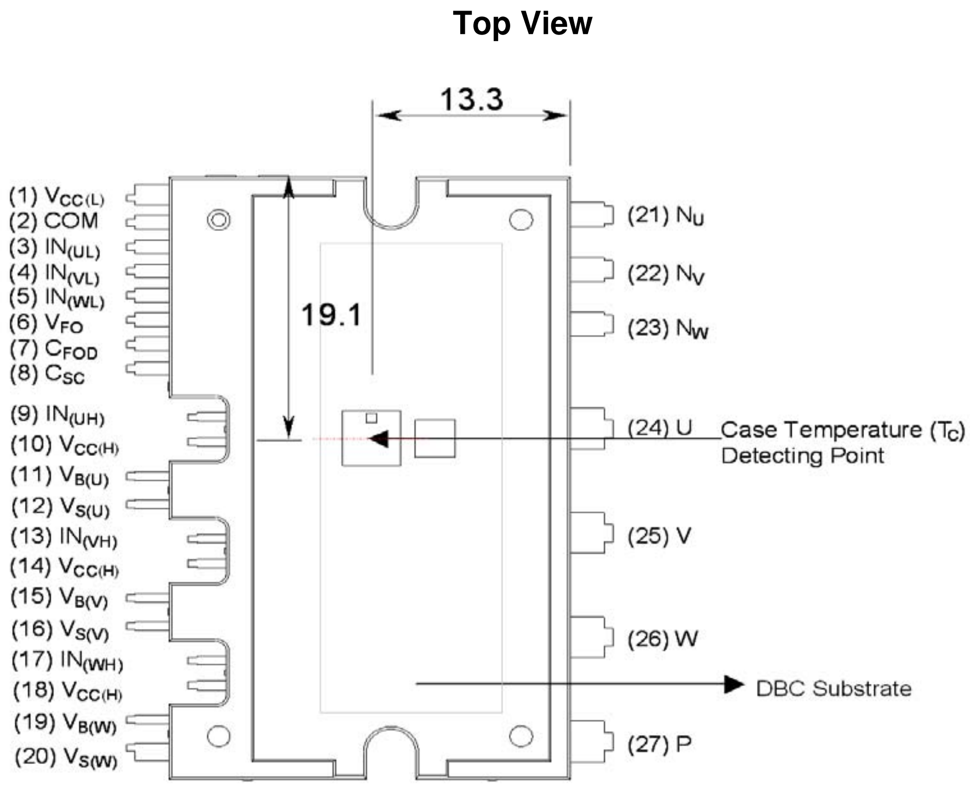
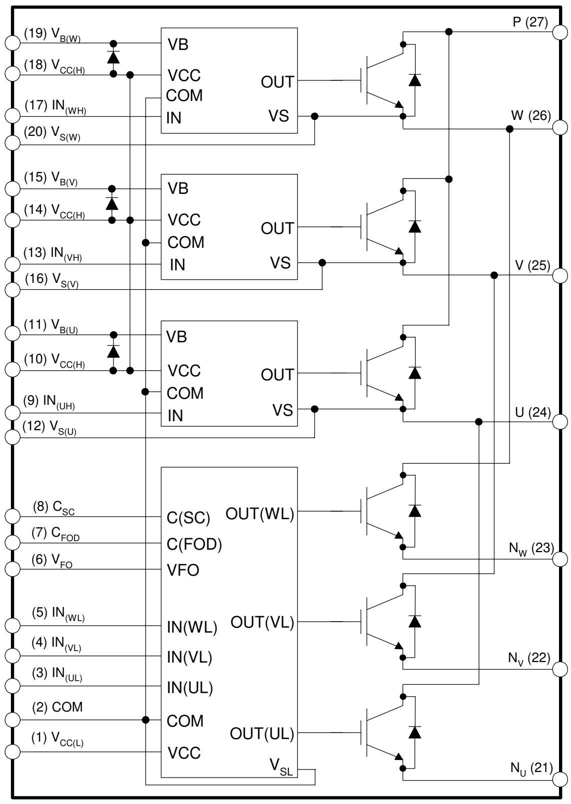



**Figure 2.**

## Pin Descriptions

| Pin Number | Pin Name | Pin Description |
|---|---|---|
| 1 | $V_{CC(L)}$ | Low-side Common Bias Voltage for IC and IGBTs Driving |
| 2 | COM | Common Supply Ground |
| 3 | $IN_{(UL)}$ | Signal Input for Low-side U Phase |
| 4 | $IN_{(VL)}$ | Signal Input for Low-side V Phase |
| 5 | $IN_{(WL)}$ | Signal Input for Low-side W Phase |
| 6 | $V_{FO}$ | Fault Output |
| 7 | $C_{FOD}$ | Capacitor for Fault Output Duration Time Selection |
| 8 | $C_{SC}$ | Capacitor (Low-pass Filter) for Short-Current Detection Input |
| 9 | $IN_{(UH)}$ | Signal Input for High-side U Phase |
| 10 | $V_{CC(H)}$ | High-side Common Bias Voltage for IC and IGBTs Driving |
| 11 | $V_{B(U)}$ | High-side Bias Voltage for U Phase IGBT Driving |
| 12 | $V_{S(U)}$ | High-side Bias Voltage Ground for U Phase IGBT Driving |
| 13 | $IN_{(VH)}$ | Signal Input for High-side V Phase |
| 14 | $V_{CC(H)}$ | High-side Common Bias Voltage for IC and IGBTs Driving |
| 15 | $V_{B(V)}$ | High-side Bias Voltage for V Phase IGBT Driving |
| 16 | $V_{S(V)}$ | High-side Bias Voltage Ground for V Phase IGBT Driving |
| 17 | $IN_{(WH)}$ | Signal Input for High-side W Phase |
| 18 | $V_{CC(H)}$ | High-side Common Bias Voltage for IC and IGBTs Driving |
| 19 | $V_{B(W)}$ | High-side Bias Voltage for W Phase IGBT Driving |
| 20 | $V_{S(W)}$ | High-side Bias Voltage Ground for W Phase IGBT Driving |
| 21 | $N_U$ | Negative DC–Link Input for U Phase |
| 22 | $N_V$ | Negative DC–Link Input for V Phase |
| 23 | $N_W$ | Negative DC–Link Input for W Phase |
| 24 | U | Output for U Phase |
| 25 | V | Output for V Phase |
| 26 | W | Output for W Phase |
| 27 | P | Positive DC–Link Input |

## Internal Equivalent Circuit and Input/Output Pins




**Note:**

1. Inverter low-side is composed of three IGBTs, freewheeling diodes for each IGBT and one control IC. It has gate drive and protection functions.
2. Inverter power side is composed of four inverter dc-link input terminals and three inverter output terminals.
3. Inverter high-side is composed of three IGBTs, freewheeling diodes and three drive ICs for each IGBT.

**Figure 3.**

# Absolute Maximum Ratings ($T_J$ = 25°C, Unless Otherwise Specified)

## Inverter Part

| Symbol | Parameter | Conditions | Rating | Units |
|---|---|---|---|---|
| $V_{PN}$ | Supply Voltage | Applied between P- $N_U$, $N_V$, $N_W$ | 450 | V |
| $V_{PN(Surge)}$ | Supply Voltage (Surge) | Applied between P- $N_U$, $N_V$, $N_W$ | 500 | V |
| $V_{CES}$ | Collector-emitter Voltage | | 600 | V |
| $\pm I_C$ | Each IGBT Collector Current | $T_C$ = 25°C | 15 | A |
| $\pm I_{CP}$ | Each IGBT Collector Current (Peak) | $T_C$ = 25°C, Under 1ms Pulse Width | 30 | A |
| $P_C$ | Collector Dissipation | $T_C$ = 25°C per One Chip | 55 | W |
| $T_J$ | Operating Junction Temperature | (Note 1) | -40 ~ 150 | °C |

**Note:**
1. The maximum junction temperature rating of the power chips integrated within the SPM is 150°C(@$T_C \le$ 125°C).

## Control Part

| Symbol | Parameter | Conditions | Rating | Units |
|---|---|---|---|---|
| $V_{CC}$ | Control Supply Voltage | Applied between $V_{CC(H)}$, $V_{CC(L)}$ - COM | 20 | V |
| $V_{BS}$ | High-side Control Bias Voltage | Applied between $V_{B(U)}$ - $V_{S(U)}$, $V_{B(V)}$ - $V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$ | 20 | V |
| $V_{IN}$ | Input Signal Voltage | Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ - COM | -0.3~17 | V |
| $V_{FO}$ | Fault Output Supply Voltage | Applied between $V_{FO}$ - COM | -0.3~$V_{CC}$+0.3 | V |
| $I_{FO}$ | Fault Output Current | Sink Current at $V_{FO}$ Pin | 5 | mA |
| $V_{SC}$ | Current Sensing Input Voltage | Applied between $C_{SC}$ - COM | -0.3~$V_{CC}$+0.3 | V |

## Bootstrap Diode Part

| Symbol | Parameter | Conditions | Rating | Units |
|---|---|---|---|---|
| $V_{RRM}$ | Maximum Repetitive Reverse Voltage | | 600 | V |
| $I_F$ | Forward Current | $T_C$ = 25°C | 0.5 | A |
| $I_{FP}$ | Forward Current (Peak) | $T_C$ = 25°C, Under 1ms Pulse Width | 2 | A |
| $T_J$ | Operating Junction Temperature | | -40 ~ 150 | °C |

## Total System

| Symbol | Parameter | Conditions | Rating | Units |
|---|---|---|---|---|
| $V_{PN(PROT)}$ | Self Protection Supply Voltage Limit (Short Circuit Protection Capability) | $V_{CC} = V_{BS}$ = 13.5 ~ 16.5V<br>$T_J$ = 150°C, Non-repetitive, less than 2μs | 400 | V |
| $T_C$ | Module Case Operation Temperature | -40°C≤ $T_J \le$ 150°C, See Figure 2 | -40 ~ 125 | °C |
| $T_{STG}$ | Storage Temperature | | -40 ~ 150 | °C |
| $V_{ISO}$ | Isolation Voltage | 60Hz, Sinusoidal, AC 1 minute, Connection Pins to heat sink plate | 2500 | $V_{rms}$ |

## Thermal Resistance

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $R_{th(j-c)Q}$ | Junction to Case Thermal Resistance | Inverter IGBT part (per 1/6 module) | - | - | 2.27 | °C/W |
| $R_{th(j-c)F}$ | | Inverter FWD part (per 1/6 module) | - | - | 3.0 | °C/W |

**Note:**
2. For the measurement point of case temperature($T_C$), please refer to Figure 2.

# Electrical Characteristics ($T_J$ = 25°C, Unless Otherwise Specified)

## Inverter Part

| Symbol | | Parameter | Conditions | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| $V_{CE(SAT)}$ | | Collector-Emitter Saturation Voltage | $V_{CC}$ = $V_{BS}$ = 15V<br>$V_{IN}$ = 5V | $I_C$ = 15A, $T_J$ = 25°C | - | - | 2.0 | V |
| $V_F$ | | FWD Forward Voltage | $V_{IN}$ = 0V | $I_F$ = 15A, $T_J$ = 25°C | - | - | 2.2 | V |
| HS | $t_{ON}$ | Switching Times | $V_{PN}$ = 300V, $V_{CC}$ = $V_{BS}$ = 15V<br>$I_C$ = 15A<br>$V_{IN}$ = 0V ↔ 5V, Inductive Load<br>(Note 3) | | - | 0.80 | - | μs |
| | $t_{C(ON)}$ | | | | - | 0.20 | - | μs |
| | $t_{OFF}$ | | | | - | 0.65 | - | μs |
| | $t_{C(OFF)}$ | | | | - | 0.10 | - | μs |
| | $t_{rr}$ | | | | - | 0.10 | - | μs |
| LS | $t_{ON}$ | | $V_{PN}$ = 300V, $V_{CC}$ = $V_{BS}$ = 15V<br>$I_C$ = 15A<br>$V_{IN}$ = 0V ↔ 5V, Inductive Load<br>(Note 3) | | - | 0.50 | - | μs |
| | $t_{C(ON)}$ | | | | - | 0.30 | - | μs |
| | $t_{OFF}$ | | | | - | 0.65 | - | μs |
| | $t_{C(OFF)}$ | | | | - | 0.15 | - | μs |
| | $t_{rr}$ | | | | - | 0.10 | - | μs |
| $I_{CES}$ | | Collector-Emitter Leakage Current | $V_{CE}$ = $V_{CES}$ | | - | - | 1 | mA |

**Note:**

3. $t_{ON}$ and $t_{OFF}$ include the propagation delay time of the internal drive IC. $t_{C(ON)}$ and $t_{C(OFF)}$ are the switching time of IGBT itself under the given gate driving condition internally. For the detailed information, please see Figure 4.

## Control Part

| Symbol | Parameter | Conditions | | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|---|
| $I_{QCCL}$ | Quiescent $V_{CC}$ Supply Current | $V_{CC}$ = 15V<br>$IN_{(UL, VL, WL)}$ = 0V | $V_{CC(L)}$ - COM | - | - | 23 | mA |
| $I_{QCCH}$ | | $V_{CC}$ = 15V<br>$IN_{(UH, VH, WH)}$ = 0V | $V_{CC(H)}$ - COM | - | - | 600 | μA |
| $I_{QBS}$ | Quiescent $V_{BS}$ Supply Current | $V_{BS}$ = 15V<br>$IN_{(UH, VH, WH)}$ = 0V | $V_{B(U)}$ - $V_{S(U)}$, $V_{B(V)}$ -$V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$ | - | - | 500 | μA |
| $V_{FOH}$ | Fault Output Voltage | $V_{SC}$ = 0V, $V_{FO}$ Circuit: 4.7kΩ to 5V Pull-up | | 4.5 | - | - | V |
| $V_{FOL}$ | | $V_{SC}$ = 1V, $V_{FO}$ Circuit: 4.7kΩ to 5V Pull-up | | - | - | 0.8 | V |
| $V_{SC(ref)}$ | Short Circuit Trip Level | $V_{CC}$ = 15V (Note 4) | | 0.45 | 0.5 | 0.55 | V |
| TSD | Over-temperature protection | Temperature at LVIC | | - | 160 | - | °C |
| ΔTSD | Over-temperature protection hysterisis | Temperature at LVIC | | - | 5 | - | °C |
| $UV_{CCD}$ | Supply Circuit Under-Voltage Protection | Detection Level | | 10.7 | 11.9 | 13.0 | V |
| $UV_{CCR}$ | | Reset Level | | 11.2 | 12.4 | 13.4 | V |
| $UV_{BSD}$ | | Detection Level | | 10 | 11 | 12 | V |
| $UV_{BSR}$ | | Reset Level | | 10.5 | 11.5 | 12.5 | V |
| $t_{FOD}$ | Fault-out Pulse Width | $C_{FOD}$ = 33nF (Note 5) | | 1.0 | 1.8 | - | ms |
| $V_{IN(ON)}$ | ON Threshold Voltage | Applied between $IN_{(UH)}$, $IN_{(VH)}$, $IN_{(WH)}$, $IN_{(UL)}$, $IN_{(VL)}$, $IN_{(WL)}$ - COM | | 2.8 | - | - | V |
| $V_{IN(OFF)}$ | OFF Threshold Voltage | | | - | - | 0.8 | V |

**Note:**

4. Short-circuit current protection is functioning only at the low-sides.

5. The fault-out pulse width $t_{FOD}$ depends on the capacitance value of $C_{FOD}$ according to the following approximate equation : $C_{FOD} = 18.3 \times 10^{-6} \times t_{FOD}$[F]

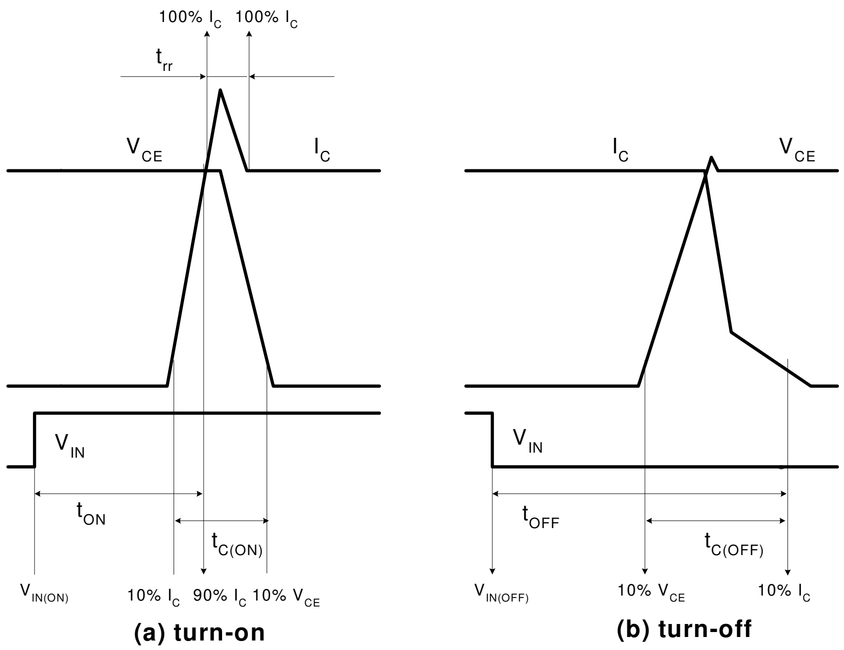



**Figure 4. Switching Time Definition**

## Switching Loss (Typical)

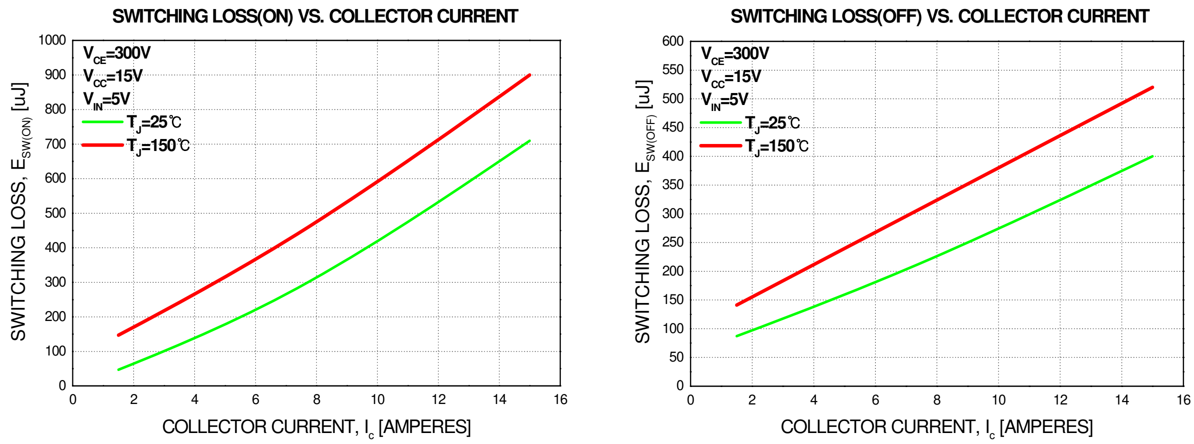
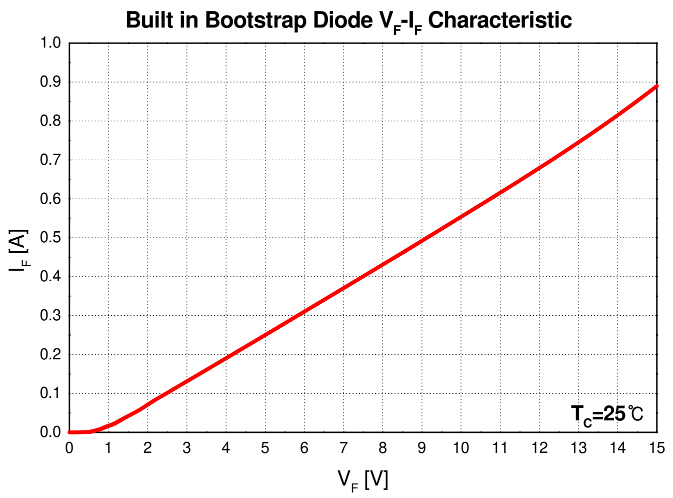



**Figure 5. Switching Loss Characteristics**

### Bootstrap Diode Part

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|---|
| $V_F$ | Forward Voltage | $I_F$ = 0.1A, $T_C$ = 25°C | - | 2.5 | - | V |
| $t_{rr}$ | Reverse Recovery Time | $I_F$ = 0.1A, $T_C$ = 25°C | - | 80 | - | ns |




**Note:**

6. Built in bootstrap diode includes around 15Ω resistance characteristic.

**Figure 6. Built in Bootstrap Diode Characteristics**

## Recommended Operating Conditions

| Symbol | Parameter | Conditions | Value | | | Units |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| $V_{PN}$ | Supply Voltage | Applied between P - $N_U$, $N_V$, $N_W$ | - | 300 | 400 | V |
| $V_{CC}$ | Control Supply Voltage | Applied between $V_{CC(H)}$, $V_{CC(L)}$- COM | 13.5 | 15 | 16.5 | V |
| $V_{BS}$ | High-side Bias Voltage | Applied between $V_{B(U)}$ - $V_{S(U)}$, $V_{B(V)}$ - $V_{S(V)}$, $V_{B(W)}$ - $V_{S(W)}$ | 13.0 | 15 | 18.5 | V |
| $dV_{CC}/dt$, $dV_{BS}/dt$ | Control supply variation | | -1 | - | 1 | V/µs |
| $t_{dead}$ | Blanking Time for Preventing Arm-short | For Each Input Signal | 2.0 | - | - | µs |
| $f_{PWM}$ | PWM Input Signal | -40°C ≤ $T_C$ ≤ 125°C, -40°C ≤ $T_J$ ≤ 150°C | - | - | 20 | kHz |
| $V_{SEN}$ | Voltage for Current Sensing | Applied between $N_U$, $N_V$, $N_W$ - COM (Including surge voltage) | -4 | | 4 | V |

## Mechanical Characteristics and Ratings

| Parameter | Conditions | | Limits | | | Units |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Mounting Torque | Mounting Screw: - M3 | Recommended 0.62N•m | 0.51 | 0.62 | 0.80 | N•m |
| Device Flatness | | Note Figure 5 | 0 | - | +120 | µm |
| Weight | | | - | 15.00 | - | g |

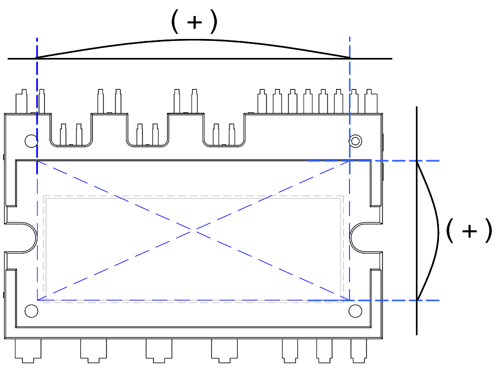
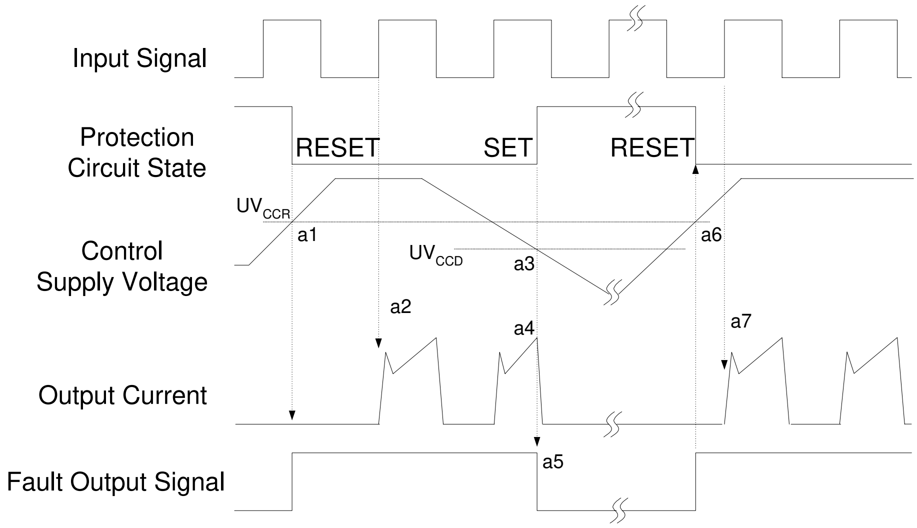



**Figure 7. Flatness Measurement Position**

## Package Marking and Ordering Information

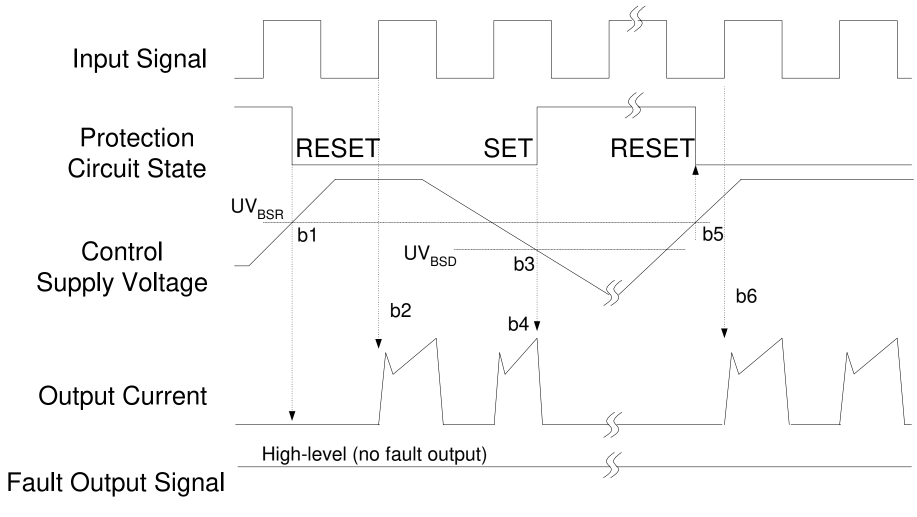
| Device Marking | Device | Package | Reel Size | Tape Width | Quantity |
|---|---|---|---|---|---|
| FSBB15CH60B | FSBB15CH60B | SPM27-CC | - | - | 10 |

## Time Charts of SPMs Protective Function



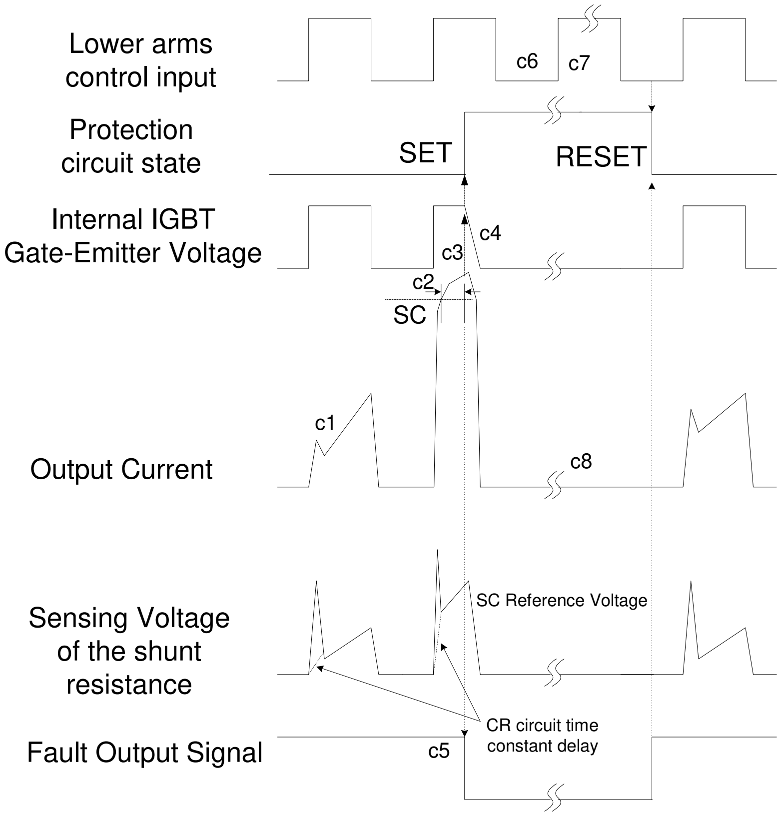

a1 : Control supply voltage rises: After the voltage rises $UV_{CCR}$, the circuits start to operate when next input is applied.
a2 : Normal operation: IGBT ON and carrying current.
a3 : Under voltage detection ($UV_{CCD}$).
a4 : IGBT OFF in spite of control input condition.
a5 : Fault output operation starts.
a6 : Under voltage reset ($UV_{CCR}$).
a7 : Normal operation: IGBT ON and carrying current.

**Figure 8. Under-Voltage Protection (Low-side)**




b1 : Control supply voltage rises: After the voltage reaches $UV_{BSR}$, the circuits start to operate when next input is applied.
b2 : Normal operation: IGBT ON and carrying current.
b3 : Under voltage detection ($UV_{BSD}$).
b4 : IGBT OFF in spite of control input condition, but there is no fault output signal.
b5 : Under voltage reset ($UV_{BSR}$)
b6 : Normal operation: IGBT ON and carrying current

**Figure 9. Under-Voltage Protection (High-side)**




(with the external shunt resistance and CR connection)

c1 : Normal operation: IGBT ON and carrying current.

c2 : Short circuit current detection (SC trigger).

c3 : Hard IGBT gate interrupt.

c4 : IGBT turns OFF.

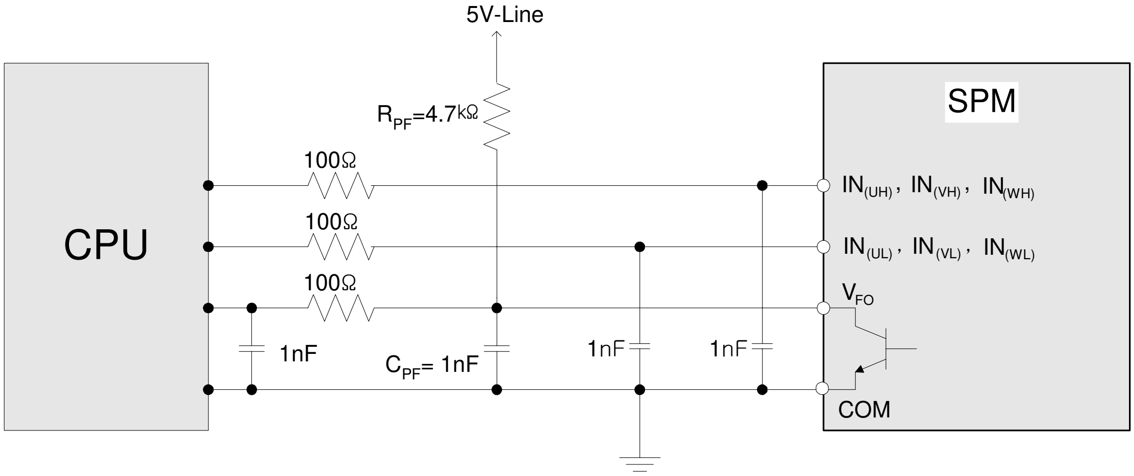
c5 : Fault output timer operation starts: The pulse width of the fault output signal is set by the external capacitor $C_{FO}$.

c6 : Input “L” : IGBT OFF state.

c7 : Input “H”: IGBT ON state, but during the active period of fault output the IGBT doesn’t turn ON.

c8 : IGBT OFF state

**Figure 10. Short-Circuit Current Protection (Low-side Operation only)**

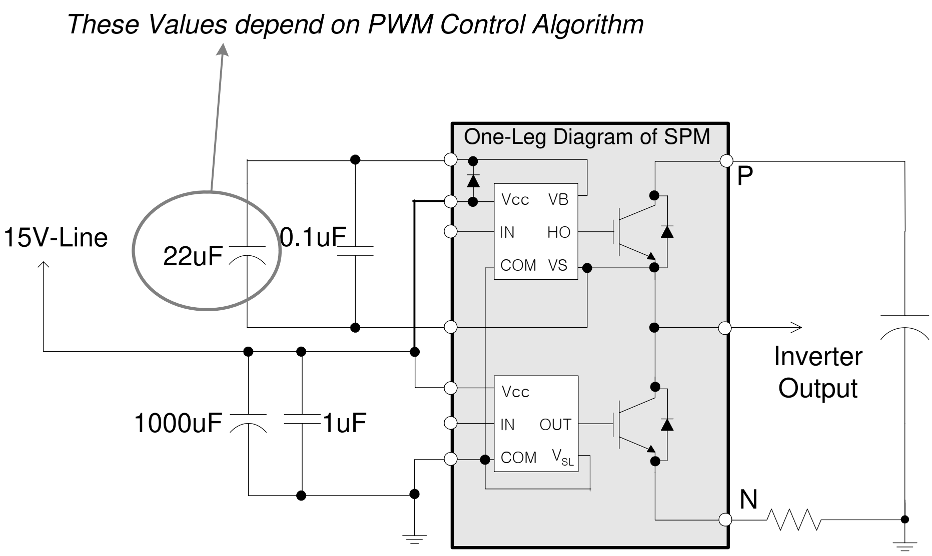



**Note:**

1) RC coupling at each input might change depending on the PWM control scheme used in the application and the wiring impedance of the application's printed circuit board. The SPM input signal section integrates 5kΩ (typ.) pull-down resistor. Therefore, when using an external filtering resistor, please pay attention to the signal voltage drop at input terminal.

2) The logic input is compatible with standard CMOS or LSTTL outputs.

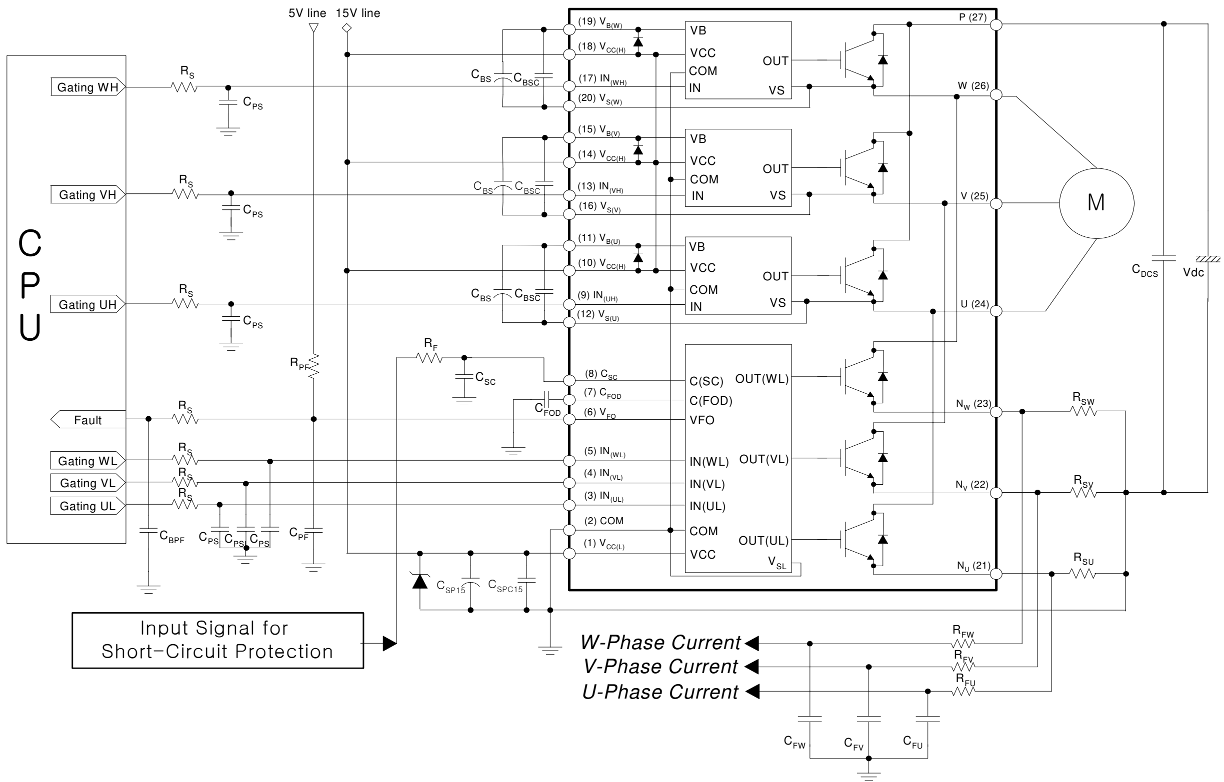
**Figure 11. Recommended CPU I/O Interface Circuit**




**Note:**

1) The ceramic capacitor placed between $V_{CC}$-COM should be over 1uF and mounted as close to the pins of the SPM as possible.

**Figure 12. Recommended Bootstrap Operation Circuit and Parameters**




**Note:**

1) To avoid malfunction, the wiring of each input should be as short as possible. (less than 2-3cm)

2) By virtue of integrating an application specific type HVIC inside the SPM, direct coupling to CPU terminals without any opto-coupler or transformer isolation is possible.

3) $V_{FO}$ output is open collector type. This signal line should be pulled up to the positive side of the 5V power supply with approximately 4.7kΩ resistance. Please refer to Figure11.

4) $C_{SP15}$ of around 7 times larger than bootstrap capacitor $C_{BS}$ is recommended.

5) $V_{FO}$ output pulse width should be determined by connecting an external capacitor($C_{FOD}$) between $C_{FOD}$(pin7) and COM(pin2). (Example : if $C_{FOD}$ = 33 nF, then $t_{FO}$ = 1.8ms (typ.)) Please refer to the note 5 for calculation method.

6) Input signal is High-Active type. There is a 5kΩ resistor inside the IC to pull down each input signal line to GND. RC coupling circuits should be adopted for the prevention of input signal oscillation. $R_SC_{PS}$ time constant should be selected in the range 50~150ns. $C_{PS}$ should not be less than 1nF.(Recommended $R_S$=100Ω , $C_{PS}$=1nF)

7) To prevent errors of the protection function, the wiring around $R_F$ and $C_{SC}$ should be as short as possible.

8) In the short-circuit protection circuit, please select the $R_FC_{SC}$ time constant in the range 1.5~2μs.

9) Each capacitor should be mounted as close to the pins of the SPM as possible.

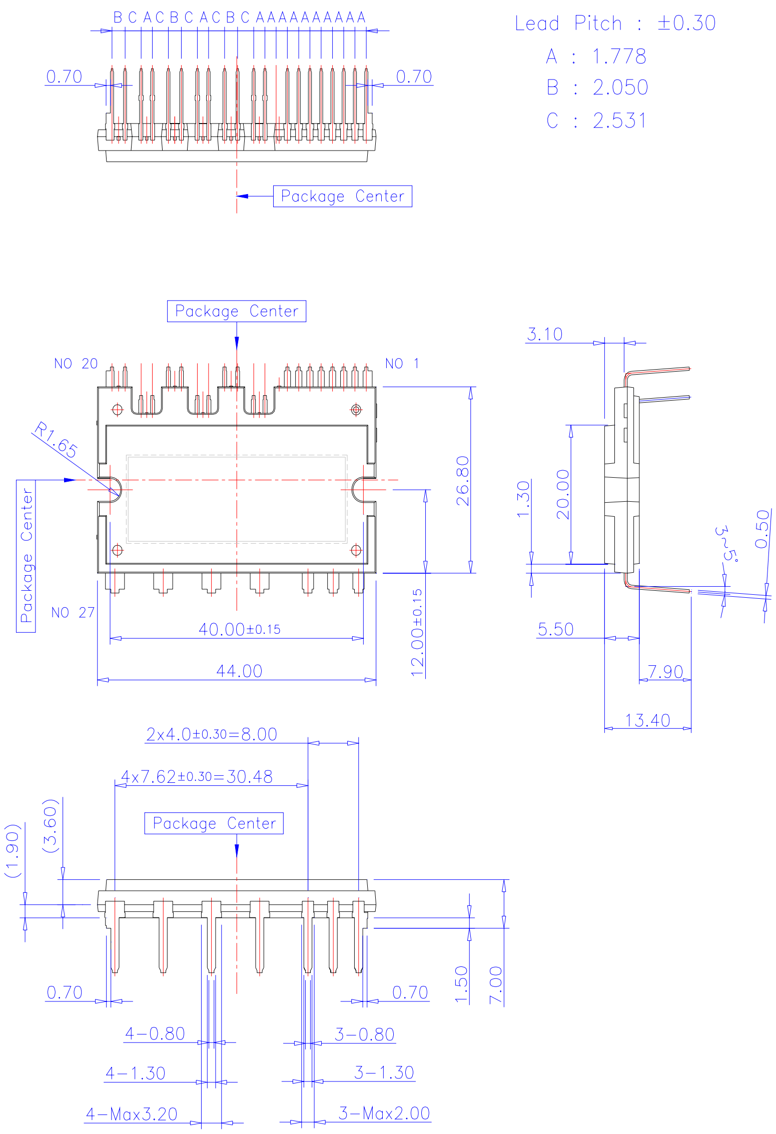
10) To prevent surge destruction, the wiring between the smoothing capacitor and the P&GND pins should be as short as possible. The use of a high frequency non-inductive capacitor of around 0.1~0.22μF between the P&GND pins is recommended.

11) Relays are used at almost every systems of electrical equipments of home appliances. In these cases, there should be sufficient distance between the CPU and the relays.

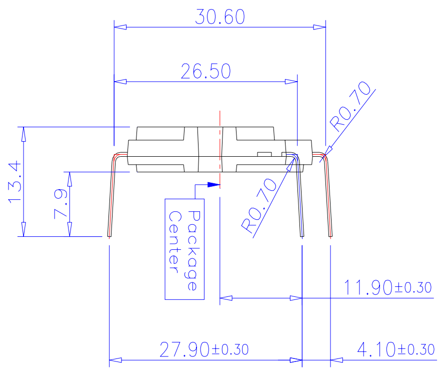
12) $C_{SPC15}$ should be over 1μF and mounted as close to the pins of the SPM as possible.

**Figure 13. Typical Application Circuit**

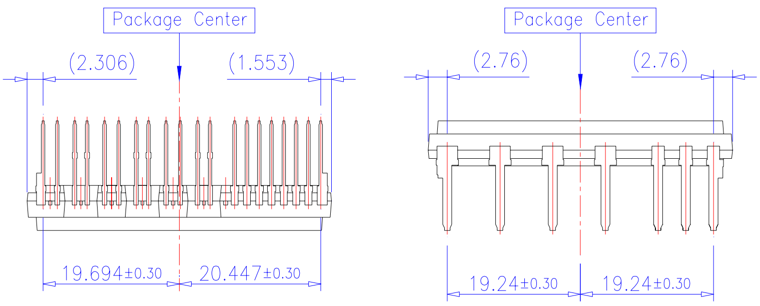
## Detailed Package Outline Drawings



## Detailed Package Outline Drawings (Continued)

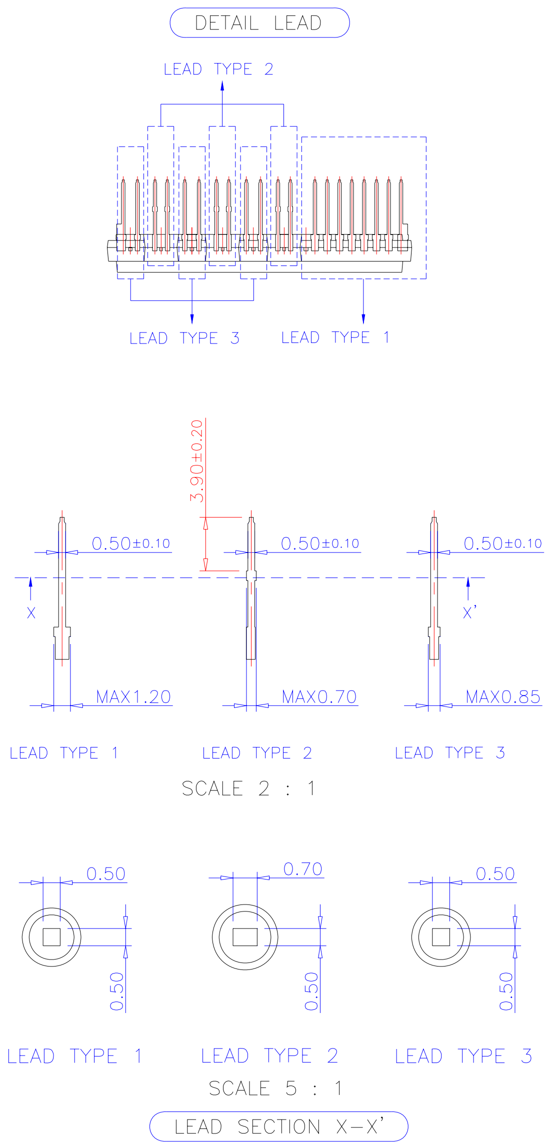



Lead Forming Dimension




PKG Center to Lead Distance

## Detailed Package Outline Drawings (Continued)



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Motion-SPM™
OPTOLOGIC®
OPTOPLANAR®
PDP-SPM™
Power220®
Power247®
POWEREDGE®
Power-SPM™
PowerTrench®
Programmable Active Droop™
QFET®
QS™
QT Optoelectronics™
Quiet Series™
RapidConfigure™
SMART START™
SPM®
STEALTH™
SuperFET™
SuperSOT™-3
SuperSOT™-6
SuperSOT™-8
SyncFET™
The Power Franchise®
™
TinyBoost™
TinyBuck™
TinyLogic®
TINYOPTO™
TinyPower™
TinyPWM™
TinyWire™
µSerDes™
UHC®
UniFET™
VCX™

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1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

### PRODUCT STATUS DEFINITIONS

**Definition of Terms**

| Datasheet Identification | Product Status | Definition |
|---|---|---|
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