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FSCQ-Series FSCQ0565RT/FSCQ0765RT/FSCQ0965RT/FSCQ1265RT/ FSCQ1465RT/FSCQ1565RT/FSCQ1565RP Green Mode Fairchild Power Switch (FPS™)

Features

- Optimized for Quasi-Resonant Converter (QRC)
- Advanced Burst-Mode Operation for under 1W Standby Power Consumption
- Pulse-by-Pulse Current Limit
- Over Load Protection (OLP) Auto Restart
- Over Voltage Protection (OVP) Auto Restart
- Abnormal Over Current Protection (AOCP) Latch
- Internal Thermal Shutdown (TSD) Latch
- Under Voltage Lock Out (UVLO) with Hysteresis
- Low Startup Current (typical: 25µA)
- Internal High Voltage SenseFET
- Built-in Soft Start (20ms)
- Extended Quasi-Resonant Switching

Applications

- CTV
- Audio Amplifier

Related Application Notes

- AN4146: Design Guidelines for Quasi-Resonant Converters Using FSCQ-Series Fairchild Power Switch.
- AN4140: Transformer Design Consideration for Off-Line Flyback Converters Using Fairchild Power Switch.

Description

A Quasi-Resonant Converter (QRC) typically shows lower EMI and higher power conversion efficiency compared to conventional hard-switched converter with a fixed switching frequency. Therefore, a QRC is well suited for noise-sensitive applications, such as color TV and audio. Each product in the FSCQ-Series contains an integrated Pulse Width Modulation (PWM) controller and a SenseFET, and is specifically designed for quasiresonant off-line Switch Mode Power Supplies (SMPS) with minimal external components. The PWM controller includes an integrated fixed frequency oscillator, under voltage lockout, leading edge blanking (LEB), optimized gate driver, internal soft start, temperature-compensated precise current sources for a loop compensation, and self protection circuitry. Compared with a discrete MOSFET and PWM controller solution, the FSCQ-Series can reduce total cost, component count, size, and weight, while simultaneously increasing efficiency, productivity, and system reliability. These devices provide a basic platform that is well suited for cost-effective designs of quasi-resonant switching flyback converters.

Ordering Information

Product Number	Package	Marking Code	BVdss	R _{ds(ON)} Max.
FSCQ0565RTYDTU	TO-220F-5L (Forming)	CQ0565RT	650V	2.2Ω
FSCQ0765RTYDTU	TO-220F-5L (Forming)	CQ0765RT	650V	1.6Ω
FSCQ0965RTYDTU	TO-220F-5L (Forming)	CQ0965RT	650V	1.2Ω
FSCQ1265RTYDTU	TO-220F-5L (Forming)	CQ1265RT	650V	0.9Ω
FSCQ1465RTYDTU	TO-220F-5L(Forming)	CQ1465RT	650V	0.8Ω
FSCQ1565RTYDTU	TO-220F-5L (Forming)	CQ1565RT	650V	0.7Ω
FSCQ1565RPVDTU	TO-3PF-7L (Forming)	CQ1565RP	650V	0.7Ω

YDTU: Forming Type VDTU: Forming Type

Typical Circuit

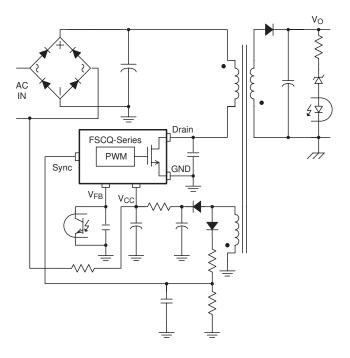


Figure 1. Typical Flyback Application

Table 1. Maximum Output Power

Output Power Table ³						
	85-265 VAC					
Product	Open Frame ¹	Open Frame ¹				
FSCQ0565RT	70W	60W				
FSCQ0765RT	100W	85W				
FSCQ0965RT	130W	110W				
FSCQ1265RT	170W	140W				
FSCQ1465RT	190W	160W				
FSCQ1565RT	210W	170W				
FSCQ1565RP	250W	210W				

Notes:

- 1. Maximum practical continuous power in an open frame design at 50°C ambient.
- 2. 230 VAC or 100/115 VAC with doubler.
- 3. The junction temperature can limit the maximum output power.

Internal Block Diagram Vcc Drain 3 1 Quasi-Resonant (QR) Switching Controller Threshold - 9V/15V Soft Start 4.6V/2.6V: Normal QR Vcc good 3.0V/1.8V: Extended QR Burst Mode Auxiliary Controller Vref OSC Main Bias V_{Burst} □ Burst Switching Normal Operation Normal Vref Vref Operation Internal Bias I_B I_{FB} Idelay PWM V_{FB} 4 2.5R Gate RŠ Driver LEB 600ns Sync AOCP Vovp □ VCC good (VCC = 9V) R 2 GND TSD Vocp Power Off Reset (V_{CC} = 6V)

Figure 2. Functional Block Diagram of FSCQ-Series

Pin Configuration

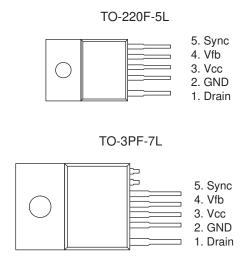


Figure 3. Pin Configuration (Top View)

Pin Definitions

Pin Number	Pin Name	Pin Function Description				
1	Drain	High voltage power SenseFET drain connection.				
2	GND	This pin is the control ground and the SenseFET source.				
3	Vcc	This pin is the positive supply input. This pin provides internal operating current for both start-up and steady-state operation.				
4	Vfb	This pin is internally connected to the inverting input of the PWM comparator. The collector of an optocoupler is typically tied to this pin. For stable operation, a capacitor should be placed between this pin and GND. If the voltage of this pin reaches 7.5V, the over load protection triggers, which results in the FPS shutting down.				
5	Sync	This pin is internally connected to the sync detect comparator for quasi-resonant switching. In normal quasi-resonant operation, the threshold of the sync comparator is 4.6V/2.6V. Whereas, the sync threshold is changed to 3.0V/1.8V in an extended quasi-resonant operation.				

Absolute Maximum Ratings

 $(T_A = 25$ °C, unless otherwise specified)

Parameter	Symbol		Value	Unit
Drain Pin Voltage		V _{DS}	650	V
Supply Voltage		V _{CC}	20	V
Analog Input Voltage Range		V _{sync}	-0.3 to 13V	V
		V _{FB}	-0.3 to V _{CC}	V
Drain Current Pulsed ⁴	I _{DM}	FSCQ0565RT	11.2	А
		FSCQ0765RT	15.2	
		FSCQ0965RT	16.4	
		FSCQ1265RT	21.2	
		FSCQ1465RT	22	
		FSCQ1565RT	26.4	
		FSCQ1565RP	33.2	
Continuous Drain Current (Tc = 25°C)	I _D	FSCQ0565RT	2.8	A _(rms)
(Tc: Case Back Surface Temperature)		FSCQ0765RT	3.8	
		FSCQ0965RT	4.1	
		FSCQ1265RT	5.3	
		FSCQ1465RT	5.5	
		FSCQ1565RT	6.6	
		FSCQ1565RP	8.3	
Continuous Drain Current* (T _{DL} = 25°C)	I _D *	FSCQ0565RT	5	A _(rms)
(T _{DL:} Drain Lead Temperature)		FSCQ0765RT	7	
		FSCQ0965RT	7.6	
		FSCQ1265RT	11	
		FSCQ1465RT	12	
		FSCQ1565RT	13.3	
		FSCQ1565RP	15	7
Continuous Drain Current (T _C = 100°C)	I _D	FSCQ0565RT	1.7	A _(rms)
		FSCQ0765RT	2.4	
		FSCQ0965RT	2.6	
		FSCQ1265RT	3.4	
		FSCQ1465RT	3.5	
		FSCQ1565RT	4.4	
		FSCQ1565RP	5.5	
Single-Pulsed Avalanche Energy ⁵	E _{AS}	FSCQ0565RT	400	mJ
		FSCQ0765RT	570	
		FSCQ0965RT	630	
		FSCQ1265RT	950	
		FSCQ1465RT	1000	
		FSCQ1565RT	1050	
		FSCQ1565RP	1050	

Absolute Maximum Ratings (Continued)

 $(T_A = 25$ °C, unless otherwise specified)

Total Power Dissipation	P _D	FSCQ0565RT	38	W
(Tc = 25°C with Infinite Heat Sink)		FSCQ0765RT	45	
		FSCQ0965RT	49	
		FSCQ1265RT	50	
		FSCQ1465RT	60	
		FSCQ1565RT	75	
		FSCQ1565RP	98	
Operating Junction Temperature		T _J	+150	°C
Operating Ambient Temperature		T _A	-25 to +85	°C
Storage Temperature Range		T _{STG}	-55 to +150	°C
ESD Capability, HBM Model (All pins except Vfb)		_	2.0 (GND – Vfb = 1.7kV)	kV
ESD Capability, Machine Model (All pins except Vfb)		_	300 (GND – Vfb = 170V)	V

Notes:

Thermal Impedance

(T_A = 25°C unless otherwise specified)

Parameter	Symbol		Value	Unit
Junction to Case Thermal Impedance	θ_{JC}	FSCQ0565RT	3.29	°C/W
		FSCQ0765RT	2.60	
		FSCQ0965RT	2.55	
		FSCQ1265RT	2.50	
		FSCQ1465RT	2.10	
		FSCQ1565RT	2.00	
		FSCQ1565RP	1.28	

^{4.} Repetitive rating: pulse width limited by maximum junction temperature.

^{5.} L = 15mH, starting $T_i = 25^{\circ}$ C, These parameters, although guaranteed at the design, are not tested in mass production.

Electrical Characteristics (SenseFET Part)

 $(T_A = 25^{\circ}C \text{ unless otherwise specified})$

Zero Gate Voltage Drain Current IDSS	Parameter	Symbol		Condition	Min.	Тур.	Max.	Unit
Drain-Source ON-State Rosistance Rosis	Drain-Source Breakdown Voltage	BV _{DSS}		$V_{GS} = 0V, I_D = 250\mu A$	650	-	-	V
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Zero Gate Voltage Drain Current	I _{DSS}		$V_{DS} = 650 V, V_{GS} = 0 V$	_	-	250	μΑ
FSCQ0965RT VGS = 10V, ID = 1A		R _{DS(ON)}	FSCQ0565RT	$V_{GS} = 10V, I_{D} = 1A$	_	1.76	2.2	Ω
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Resistance		FSCQ0765RT	$V_{GS} = 10V, I_{D} = 1A$	_	1.4	1.6	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$			FSCQ0965RT	$V_{GS} = 10V, I_{D} = 1A$	_	1.0	1.2	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$			FSCQ1265RT	$V_{GS} = 10V, I_D = 1A$	_	0.75	0.9	
FSCQ1565RP V _{GS} = 10V, I _D = 1A - 0.53 0.7			FSCQ1465RT	$V_{GS} = 10V, I_D = 1A$	_	0.7	0.8	
Input Capacitance C_{ISS}			FSCQ1565RT	$V_{GS} = 10V, I_D = 1A$	_	0.53	0.7	
FSCQ0765RT FSCQ0965RT FSCQ1265RT FSCQ1465RT FSCQ1565RP FSCQ0565RT FSCQ0			FSCQ1565RP	$V_{GS} = 10V, I_D = 1A$	_	0.53	0.7	
FSCQ0765RT	Input Capacitance	C _{ISS}	FSCQ0565RT		_	1080	-	pF
FSCQ1265RT FSCQ1465RT			FSCQ0765RT	f = 1MHz	_	1415	-	
FSCQ1465RT			FSCQ0965RT		_	1750	-	
FSCQ1565RT - 3050 -			FSCQ1265RT		_	2400	-	
FSCQ1565RP			FSCQ1465RT		_	2400	-	
Output Capacitance $ \begin{array}{c ccccccccccccccccccccccccccccccccccc$			FSCQ1565RT		_	3050	-	
FSCQ0765RT			FSCQ1565RP		_	3050	-	
FSCQ0765RT	Output Capacitance	C _{OSS}	FSCQ0565RT	0.0	_	90	-	pF
FSCQ1265RT		FSCQ0765RT f = 1MHz	f = 1MHz	_	100	-		
FSCQ1465RT - 185 - FSCQ1565RT - 220 -			FSCQ0965RT		_	130	_	
FSCQ1565RT - 220 -			FSCQ1265RT		_	175	_	
			FSCQ1465RT		_	185	_	
FSCQ1565BP - 220 -			FSCQ1565RT		_	220	_	
1.004.000.11			FSCQ1565RP		_	220	_	

 $(T_A = 25^{\circ}C \text{ unless otherwise specified})$

Parameter	Symbol	Condition	Min.	Тур.	Max.	Unit
Control Section	'	1				
Switching Frequency	Fosc	$V_{FB} = 5V, V_{CC} = 18V$	18	20	22	kHz
Switching Frequency Variation ⁷	ΔF _{OSC}	$-25^{\circ}C \le T_A \le 85^{\circ}C$	0	±5	±10	%
Feedback Source Current	I _{FB}	$V_{FB} = 0.8V, V_{CC} = 18V$	0.5	0.65	0.8	mA
Maximum Duty Cycle	D _{MAX}	V _{FB} = 5V, V _{CC} = 18V	92	95	98	%
Minimum Duty Cycle	D _{MIN}	$V_{FB} = 0V$, $V_{CC} = 18V$	_	0	_	%
UVLO Threshold Voltage	V _{START}	V _{FB} = 1V	14	15	16	V
	V _{STOP}		8	9	10	
Soft Start Time ⁶	T _{SS}		18	20	22	ms
Burst Mode Section	•		'		!	
Burst Mode Enable Feedback Voltage	V _{BEN}		0.25	0.40	0.55	V
Burst Mode Feedback Source Current	I _{BFB}	$V_{FB} = 0V$	60	100	140	μΑ
Burst Mode Switching Time	T _{BS}	V _{FB} = 0.9V, Duty = 50%	1.2	1.4	1.6	ms
Burst Mode Hold Time	T _{BH}	$V_{FB} = 0.9V \rightarrow 0V$	1.2	1.4	1.6	ms
Protection Section		1	'		•	
Shutdown Feedback Voltage	V _{SD}	V _{CC} = 18V	7.0	7.5	8.0	V
Shutdown Delay Current	I _{DELAY}	V _{FB} = 5V, V _{CC} = 18V	4	5	6	μΑ
Over Voltage Protection	V _{OVP}	$V_{FB} = 3V$	11	12	13	V
Over Current Latch Voltage ⁶	V _{OCL}	V _{CC} = 18V	0.9	1.0	1.1	V
Thermal Shutdown Temp ⁷	T _{SD}		140	-	_	°C

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Notes:

^{6.} These parameters, although guaranteed, are tested only in EDS (wafer test) process.

^{7.} These parameters, although guaranteed at the design, are not tested in mass production.

 $(T_A = 25^{\circ}C \text{ unless otherwise specified})$

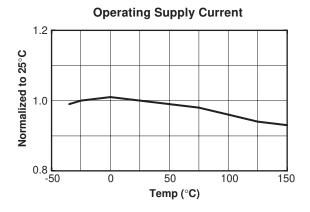
Parameter	Symbol		Condition	Min.	Тур.	Max.	Unit
Sync Section							
Sync Threshold in Normal QR (H)	V _{SH1}		$V_{CC} = 18V, V_{FB} = 5V$	4.2	4.6	5.0	V
Sync Threshold in Normal QR (L)	V _{SL1}			2.3	2.6	2.9	V
Sync Threshold in Extended QR (H)	V _{SH2}			2.7	3.0	3.3	V
Sync Threshold in Extended QR (L)	V _{SL2}			1.6	1.8	2.0	V
Extended QR Enable Frequency	F _{SYH}			_	90	_	kHz
Extended QR Disable Frequency	F _{SYL}			_	45	_	kHz
Total Device Section							
Operating Supply Current ⁹							
- In Normal Operation	I _{OP}	FSCQ0565RT	V _{FB} = 5V	_	4	6	mA
		FSCQ0765RT		_	4	6	
		FSCQ0965RT		_	6	8	
		FSCQ1265RT		_	6	8	
		FSCQ1465RT		_	7	9	
		FSCQ1565RT		_	7	9	
		FSCQ1565RP		_	7	9	
- In Burst Mode (Non-switching)	I _{OB}		V _{FB} = GND	_	0.25	0.50	mA
Startup Current	I _{START}		$V_{CC} = V_{START} - 0.1V$	_	25	50	μΑ
Sustain Latch Current ¹¹	I _{SN}		$V_{CC} = V_{STOP} - 0.1V$	_	50	100	μΑ
Current Sense Section							
Maximum Current Limit ¹⁰	I _{LIM}	FSCQ0565RT	$V_{CC} = 18V, V_{FB} = 5V$	3.08	3.5	3.92	Α
		FSCQ0765RT		4.4	5	5.6	
		FSCQ0965RT		5.28	6.0	6.72	
		FSCQ1265RT		6.16	7	7.84	
		FSCQ1465RT		7.04	8.0	8.96	
		FSCQ1565RT		7.04	8	8.96	
		FSCQ1565RP		10.12	11.5	12.88	
Burst Peak Current	I _{BUR(pk)}	FSCQ0565RT	$V_{CC} = 18V, V_{FB} = Pulse$	0.45	0.65	0.85	Α
		FSCQ0765RT		0.65	0.9	1.15	
		FSCQ0965RT		0.6	0.9	1.2	
		FSCQ1265RT		0.8	1.2	1.6	
		FSCQ1465RT		0.6	0.9	1.2	
		FSCQ1565RT		_	1	_	
		FSCQ1565RP		_	1	_	

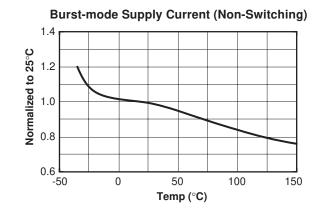
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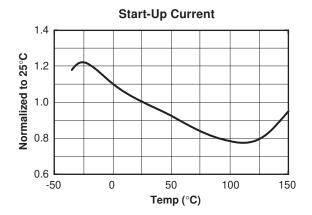
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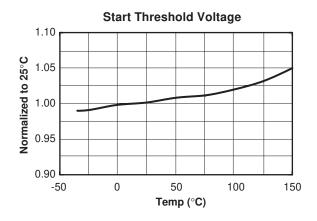
- 9. This parameter is the current flowing in the control IC.10. These parameters indicate inductor current.
- 11. These parameters, although guaranteed, are tested only in EDS (wafer test) process.

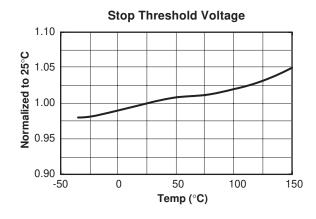
Electrical Characteristics

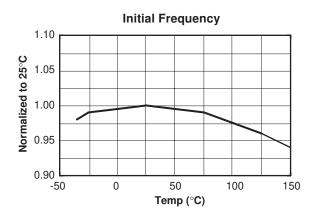


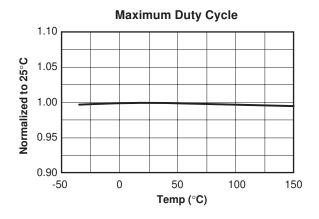


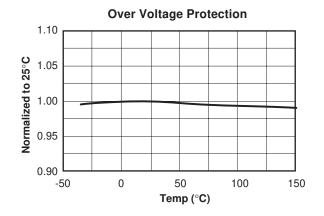


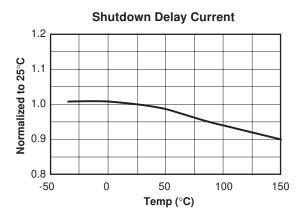


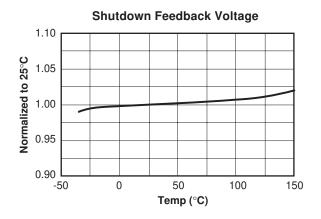


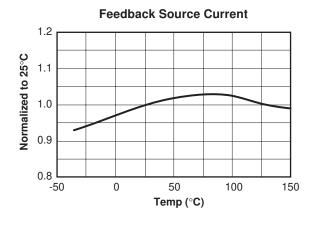


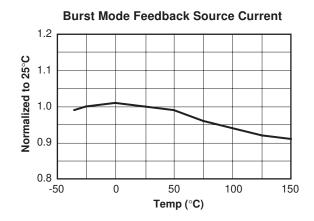


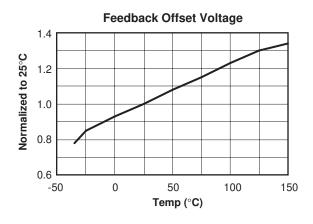


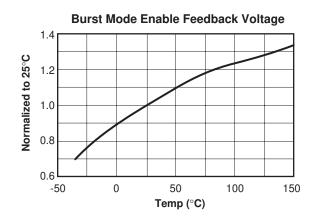


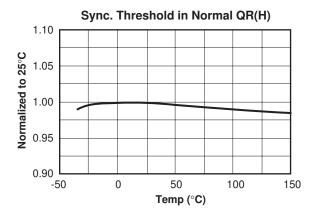


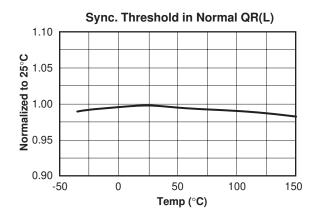


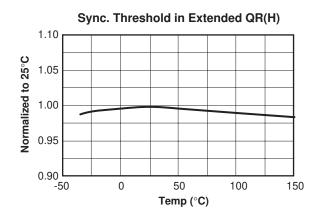


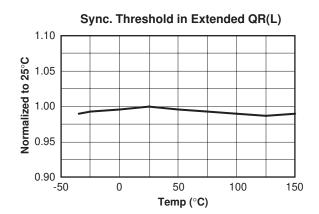


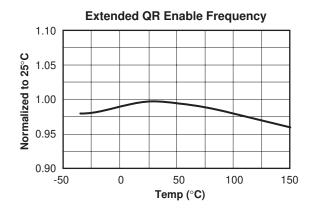


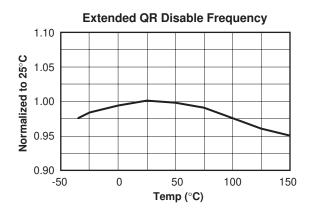


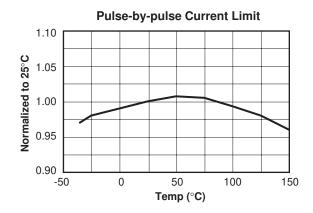












Functional Description

1. Startup: Figure 4 shows the typical startup circuit and the transformer auxiliary winding for the FSCQ-Series. Before the FSCQ-Series begins switching, it consumes only startup current (typically 25µA). The current supplied from the AC line charges the external capacitor (Ca1) that is connected to the Vcc pin. When Vcc reaches the start voltage of 15V (VSTART), the FSCQ-Series begins switching, and its current consumption increases to IOP. Then, the FSCQ-Series continues its normal switching operation and the power required for the FSCQ-Series is supplied from the transformer auxiliary winding, unless V_{CC} drops below the stop voltage of 9V (V_{STOP}). To guarantee the stable operation of the control IC, V_{CC} has under voltage lockout (UVLO) with 6V hysteresis. Figure 5 shows the relationship between the operating supply current of the FSCQ-Series and the supply voltage (V_{CC}).

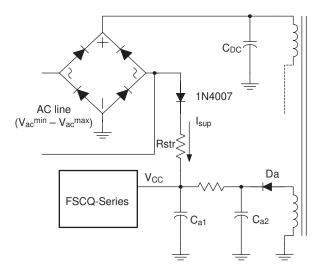


Figure 4. Startup circuit

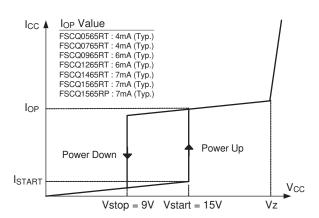


Figure 5. Relationship Between Operating Supply Current and Vcc Voltage

The minimum average of the current supplied from the AC is given by:

$$I_{sup}^{avg} = \left(\frac{\sqrt{2} \cdot V_{ac}^{min}}{\pi} - \frac{V_{start}}{2}\right) \bullet \frac{1}{R_{str}}$$

where $V_{ac}^{\ min}$ is the minimum input voltage, V_{start} is the FSCQ-Series start voltage (15V), and R_{str} is the startup resistor. The startup resistor should be chosen so that $I_{sup}^{\ avg}$ is larger than the maximum startup current (50 μ A).

Once the resistor value is determined, the maximum loss in the startup resistor is obtained as:

$$Loss = \frac{1}{R_{str}} \bullet \left(\frac{({V_{ac}}^{max})^2 + {V_{start}}^2}{2} - \frac{2\sqrt{2} \bullet {V_{start}} \bullet {V_{ac}}^{max}}{\pi} \right)$$

where V_{ac}^{max} is the maximum input voltage. The startup resistor should have properly-rated dissipation wattage.

2. Synchronization: The FSCQ-Series employs a quasiresonant switching technique to minimize the switching
noise and loss. In this technique, a capacitor (Cr) is
added between the MOSFET drain and the source as
shown in Figure 6. The basic waveforms of the quasiresonant converter are shown in Figure 7. The external
capacitor lowers the rising slope of the drain voltage to
reduce the EMI caused when the MOSFET turns off. To
minimize the MOSFET's switching loss, the MOSFET
should be turned on when the drain voltage reaches its
minimum value as shown in Figure 7.

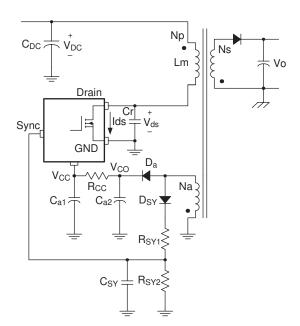


Figure 6. Synchronization Circuit

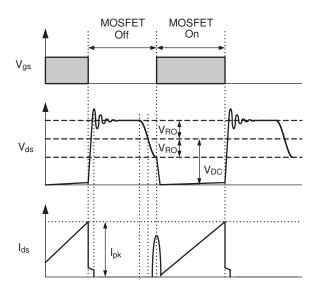


Figure 7. Quasi-Resonant Operation Waveforms

The minimum drain voltage is indirectly detected by monitoring the Vcc winding voltage as shown in Figure 6 and 8. Choose voltage dividers, R_{SY1} and $R_{SY2,}$ so that the peak voltage of the sync signal (V_{sypk}) is lower than the OVP voltage (12V) to avoid triggering OVP in normal operation. It is typical to set V_{sypk} to be lower than OVP voltage by 3–4V. To detect the optimum time to turn on MOSFET, the sync capacitor (C_{SY}) should be determined so that T_R is the same with T_Q as shown in Figure 8. The T_R and T_Q are given as, respectively:

$$\mathsf{T}_\mathsf{R} = \mathsf{R}_\mathsf{SY2} \bullet \mathsf{C}_\mathsf{SY} \bullet \mathsf{In} \bigg(\frac{\mathsf{V}_\mathsf{co}}{2.6} \bullet \frac{\mathsf{R}_\mathsf{SY2}}{\mathsf{R}_\mathsf{SY1} + \mathsf{R}_\mathsf{SY2}} \bigg)$$

$$T_Q = \pi \cdot \sqrt{L_m \cdot C_{eo}}$$

$$V_{co} = \frac{N_a \cdot (V_o + V_{FO})}{N_s} - V_{Fa}$$

where L_m is the primary side inductance of the transformer, and N_s and N_a are the number of turns for the output winding and V_{CC} winding, respectively, V_{Fo} and V_{Fa} are the diode forward voltage drops of the output winding and Vcc winding, respectively, and C_{eo} is the sum of the output capacitance of the MOSFET and the external capacitor, Cr.

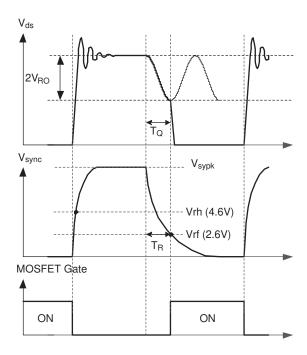


Figure 8. Normal Quasi-Resonant Operation Waveforms

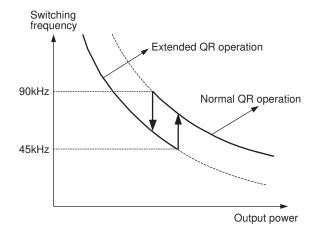


Figure 9. Extended Quasi-Resonant Operation

In general, the QRC has a limitation in a wide load range application, since the switching frequency increases as the output load decreases, resulting in a severe switching loss in the light load condition. To overcome this limitation, the FSCQ-Series employs an extended quasi-resonant switching operation. Figure 9 shows the mode change between normal and extended quasi-resonant operations. In the normal quasi-resonant operation, the FSCQ-Series enters into the extended quasi-resonant operation when the switching frequency exceeds 90kHz as the load reduces. To reduce the switching frequency, the MOSFET is turned on when the drain voltage

reaches the second minimum level, as shown in Figure 10. Once the FSCQ-Series enters into the extended quasi-resonant operation, the first sync signal is ignored. After the first sync signal is applied, the sync threshold levels are changed from 4.6V and 2.6V to 3V and 1.8V, respectively, and the MOSFET turn-on time is synchronized to the second sync signal. The FSCQ-Series returns to its normal quasi-resonant operation when the switching frequency reaches 45kHz as the load increases.

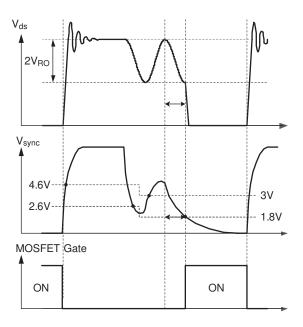


Figure 10. Extended Quasi-Resonant Operation Waveforms

- 3. Feedback Control: The FSCQ-Series employs current mode control, as shown in Figure 11. An optocoupler (such as Fairchild's H11A817A) and shunt regulator (such as Fairchild's KA431) are typically used to implement the feedback network. Comparing the feedback voltage with the voltage across the Rsense resistor plus an offset voltage makes it possible to control the switching duty cycle. When the reference pin voltage of the KA431 exceeds the internal reference voltage of 2.5V, the H11A817A LED current increases, pulling down the feedback voltage and reducing the duty cycle. This event typically happens when the input voltage is increased or the output load is decreased.
- **3.1 Pulse-by-Pulse Current Limit:** Because current mode control is employed, the peak current through the SenseFET is limited by the inverting input of the PWM comparator (Vfb*) as shown in Figure 11. The feedback current (I_{FB}) and internal resistors are designed so that the maximum cathode voltage of diode D_2 is about 2.8V, which occurs when all I_{FB} flows through the internal resistors. Since D_1 is blocked when the feedback voltage (Vfb) exceeds 2.8V, the maximum voltage of the cathode

of D2 is clamped at this voltage, thus clamping Vfb*. Therefore, the peak value of the current through the SenseFET is limited.

3.2 Leading Edge Blanking (LEB): At the instant the internal Sense FET is turned on, there is usually a high current spike through the Sense FET, caused by the external resonant capacitor across the MOSFET and secondary-side rectifier reverse recovery. Excessive voltage across the R_{sense} resistor can lead to incorrect feedback operation in the current mode PWM control. To counter this effect, the FSCQ-Series employs a leading edge blanking (LEB) circuit. This circuit inhibits the PWM comparator for a short time (T_{LEB}) after the Sense FET is turned on.

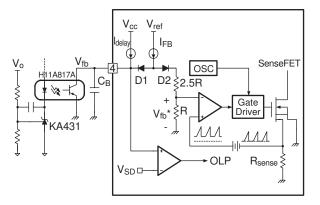


Figure 11. Pulse Width Modulation (PWM) Circuit

- **4. Protection Circuits:** The FSCQ-Series has several self-protective functions such as over load protection (OLP), abnormal over current protection (AOCP), over voltage protection (OVP), and thermal shutdown (TSD). OLP and OVP are auto-restart mode protections, while TSD and AOCP are latch mode protections. Because these protection circuits are fully integrated into the IC without external components, the reliability can be improved without increasing cost.
- Auto-restart mode protection: Once the fault condition is detected, switching is terminated and the SenseFET remains off. This causes $V_{\mbox{\footnotesize CC}}$ to fall. When Vcc falls to the under voltage lockout (UVLO) stop voltage of 9V, the protection is reset and the FSCQ-Series consumes only startup current (25µA). Then, the Vcc capacitor is charged up, since the current supplied through the startup resistor is larger than the current that the FPS consumes. When $V_{\mbox{\footnotesize CC}}$ reaches the start voltage of 15V, the FSCQ-Series resumes its normal operation. If the fault condition is not removed, the SenseFET remains off and V_{CC} drops to stop voltage again. In this manner, the auto-restart can alternately enable and disable the switching of the power SenseFET until the fault condition is eliminated (see Figure 12).

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Latch mode protection: Once this protection is triggered, switching is terminated and the Sense FET remains off until the AC power line is unplugged. Then, V_{CC} continues charging and discharging between 9V and 15V. The latch is reset only when V_{CC} is discharged to 6V by unplugging the AC power line.

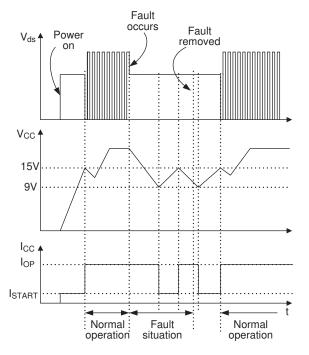


Figure 12. Auto Restart Mode Protection

4.1 Over Load Protection (OLP): Overload is defined as the load current exceeding its normal level due to an unexpected abnormal event. In this situation, the protection circuit should trigger to protect the SMPS. However, even when the SMPS is in the normal operation, the over load protection circuit can be triggered during the load transition. To avoid this undesired operation, the over load protection circuit is designed to trigger after a specified time to determine whether it is a transient situation or an overload situation. Because of the pulse-by-pulse current limit capability, the maximum peak current through the SenseFET is limited, and therefore the maximum input power is restricted with a given input voltage. If the output consumes more than this maximum power, the output voltage (Vo) decreases below the set voltage. This reduces the current through the optocoupler LED, which also reduces the optocoupler transistor current, thus increasing the feedback voltage (Vfb). If Vfb exceeds 2.8V, D1 is blocked, and the 5µA current source starts to charge C_B slowly up to V_{CC} . In this condition, Vfb continues increasing until it reaches 7.5V, then the switching operation is terminated as shown in Figure 13. The delay time for shutdown is the time required to charge C_B from 2.8V to 7.5V with 5µA. In general, a 20~50ms delay time is typical for most applications. OLP is implemented in auto restart mode.

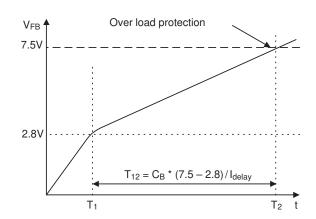


Figure 13. Over Load Protection

4.2 Abnormal Over Current Protection (AOCP): When the secondary rectifier diodes or the transformer pins are shorted, a steep current with extremely high di/dt can flow through the SenseFET during the LEB time. Even though the FSCQ-Series has OLP (Over Load Protection), it is not enough to protect the FSCQ-Series in that abnormal case, since severe current stress will be imposed on the SenseFET until the OLP triggers. The FSCQ-Series has an internal AOCP (Abnormal Over Current Protection) circuit as shown in Figure 14. When the gate turn-on signal is applied to the power SenseFET, the AOCP block is enabled and monitors the current through the sensing resistor. The voltage across the resistor is then compared with a preset AOCP level. If the sensing resistor voltage is greater than the AOCP level, the set signal is applied to the latch, resulting in the shutdown of SMPS. This protection is implemented in the latch mode.

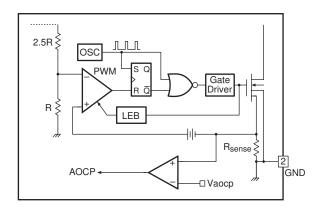


Figure 14. AOCP Block

4.3 Over Voltage Protection (OVP): If the secondary side feedback circuit malfunctions or a solder defect causes an open in the feedback path, the current through the optocoupler transistor becomes almost zero. Then, Vfb climbs up in a similar manner to the over load situation, forcing the preset maximum current to be supplied to the SMPS until the over load protection triggers. Because more energy than required is provided to the

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output, the output voltage may exceed the rated voltage before the over load protection triggers, resulting in the breakdown of the devices in the secondary side. In order to prevent this situation, an over voltage protection (OVP) circuit is employed. In general, the peak voltage of the sync signal is proportional to the output voltage and the FSCQ-Series uses a sync signal instead of directly monitoring the output voltage. If the sync signal exceeds 12V, an OVP is triggered resulting in a shutdown of SMPS. In order to avoid undesired triggering of OVP during normal operation, the peak voltage of the sync signal should be designed to be below 12V. This protection is implemented in the auto restart mode.

- **4.4 Thermal Shutdown (TSD):** The SenseFET and the control IC are built in one package. This makes it easy for the control IC to detect abnormal over temperature of the SenseFET. When the temperature exceeds approximately 150°C, the thermal shutdown triggers. This protection is implemented in the latch mode.
- **5. Soft Start:** The FSCQ-Series has an internal soft-start circuit that increases PWM comparator's inverting input voltage together with the SenseFET current slowly after it starts up. The typical soft start time is 20ms. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. Increasing the pulse width to the power switching device also helps prevent transformer saturation and reduces the stress on the secondary diode during startup. For a fast build up of the output voltage, an offset is introduced in the soft-start reference current.
- **6. Burst Operation:** In order to minimize the power consumption in the standby mode, the FSCQ-Series employs burst operation. Once FSCQ-Series enters into the burst mode, FSCQ-Series allows all output voltages and effective switching frequency to be reduced. Figure 15 shows the typical feedback circuit for C-TV applications. In normal operation, the picture on signal is applied and the transistor Q_1 is turned on, which decouples R_3 , D_z and D1 from the feedback network. Therefore, only V_{01} is regulated by the feedback circuit in normal operation and determined by R_1 and R_2 as:

$$V_{o1}^{\text{norm}} = 2.5 \bullet \left(\frac{R_1 + R_2}{R_2}\right)$$

In the standby mode, the picture ON signal is disabled and the transistor Q_1 is turned off, which couples R_3 , Dz, and D₁ to the reference pin of KA431. Then, Vo2 is determined by the zener diode breakdown voltage. Assuming that the forward voltage drop of D₁ is 0.7V, V_{o2} in standby mode is approximately given by:

$$V_{o2}^{stby} = V_Z + 0.7 + 2.5$$

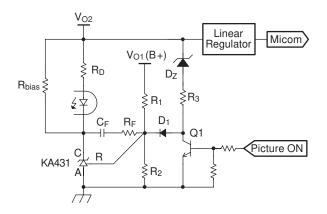


Figure 15. Typical Feedback Circuit to Drop
Output Voltage in Standby Mode

Figure 17 shows the burst mode operation waveforms. When the picture ON signal is disabled, Q₁ is turned off and R_3 and Dz are connected to the reference pin of KA431 through D_1 . Before V_{o2} drops to $V_{o2}^{\rm stby}$, the voltage on the reference pin of KA431 is higher than 2.5V, which increases the current through the opto LED. This pulls down the feedback voltage (VFR) of FSCQ-Series and forces FSCQ-Series to stop switching. If the switching is disabled longer than 1.4ms, FSCQ-Series enters into burst operation and the operating current is reduced from I_{OP} to 0.25mA (I_{OB}). Since there is no switching, V_{o2} decreases until it reaches $V_{o2}^{\rm stby}$. As V_{o2} reaches $V_{o2}^{\rm stby}$, the current through the opto LED decreases allowing the feedback voltage to rise. When the feedback voltage reaches 0.4V, FSCQ-Series resumes switching with a predetermined peak drain current of 0.9A. After burst switching for 1.4ms, FSCQ-Series stops switching and checks the feedback voltage. If the feedback voltage is below 0.4V, FSCQ-Series stops switching until the feedback voltage increases to 0.4V. If the feedback voltage is above 0.4V, FSCQ-Series goes back to the normal operation.

The output voltage drop circuit can be implemented alternatively as shown in Figure 16. In the circuit of Figure 16, the FSCQ-Series goes into burst mode, when picture off signal is applied to Q1. Then, V_{o2} is determined by the zener diode breakdown voltage. Assuming that the forward voltage drop of opto LED is 1V, the approximate value of V_{o2} in standby mode is given by:

$$V_{02}^{stby} = V_Z + 1$$

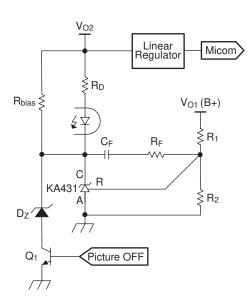
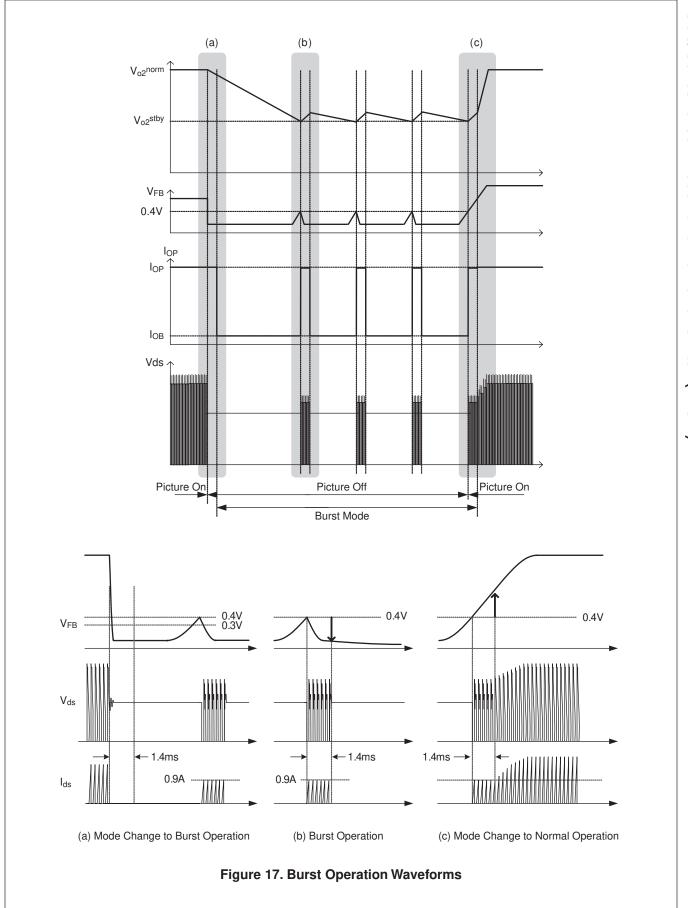


Figure 16. Feedback Circuit to Drop Output Voltage in Standby Mode



FSCQ0565RT Typical Application Circuit

Application	Output Power	Input Voltage	Output Voltage (Max Current)
C-TV	59W	Universal Input	12V (0.5A)
		(90-270 Vac)	18V (0.3A)
			125V (0.3A)
			24V (0.4A)

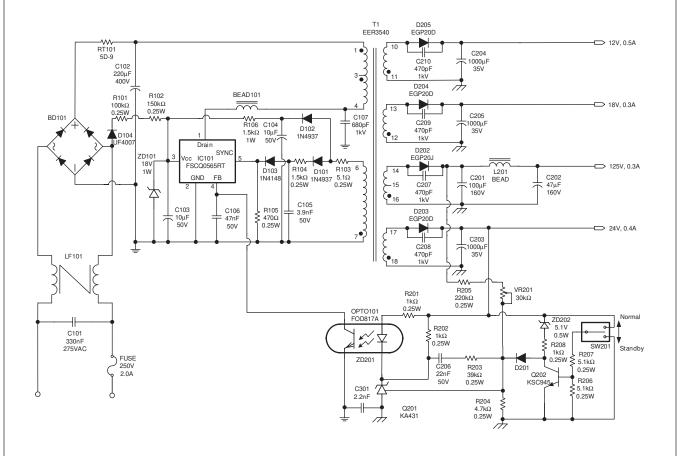
Features

- High Efficiency (>83% at 90 Vac Input)
- Wider Load Range through the Extended Quasi-Resonant Operation
- Low Standby Mode Power Consumption (<1W)
- Low Component Count
- Enhanced System Reliability Through Various Protection Functions
- Internal Soft-Start (20ms)

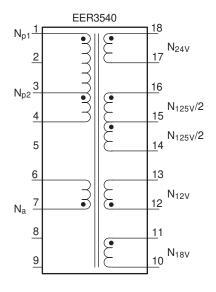
Key Design Notes

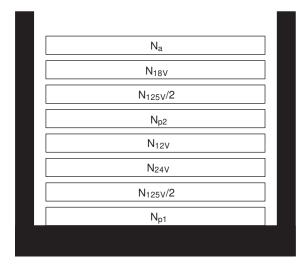
■ 24V output is designed to drop to around 8V in standby mode

1. Schematic



2. Transformer Schematic Diagram





3. Winding Specification

No	Pin (s→f)	Wire	Turns	Winding Method
N _{p1}	1–3	$0.5^{\phi} \times 1$	32	Center Winding
N _{125V} /2	16–15	$0.5^{\phi} \times 1$	32	Center Winding
N _{24V}	18–17	$0.4^{\phi} \times 2$	13	Center Winding
N _{12V}	12–13	$0.5^{\phi} \times 2$	7	Center Winding
N _{p2}	3–4	$0.5^{\phi} \times 1$	32	Center Winding
N _{125V} /2	15–14	$0.5^{\phi} \times 1$	32	Center Winding
N _{18V}	11–10	$0.4^{\phi} \times 2$	10	Center Winding
N _a	7–6	$0.3^{\phi} \times 1$	20	Center Winding

4. Electrical Characteristics

	Pin	Specification	Remarks
Inductance	1–3	740μH ± 5%	1kHz, 1V
Leakage Inductance	1–3	10μH Max	2nd all short

5. Core & Bobbin

Core: EER3540 Bobbin: EER3540 Ae: 107 mm²

6. Demo Circuit Part List

Part	Value	Note	Part	Value	Note	
Fuse			Capacitor (Continued)			
FUSE	250V/2A		C210	470pF/1kV	Ceramic Capacitor	
	NTC		C301	2.2nF/1kV	AC Ceramic Capacitor	
RT101 5D-9			Inductor			
Resistor			BEAD101	BEAD		
R101	100kΩ	0.25W	BEAD201	5μΗ	3A	
R102	150kΩ	0.25W		Diode		
R103	5.1Ω	0.25W	D101	1N4937	1A, 600V	
R104	1.5kΩ	0.25W	D102	1N4937	1A, 600V	
R105	470Ω	0.25W	D103	1N4148	0.15A, 50V	
R106	1.5kΩ	1W	D104	Short		
R107	Open		D105	Open		
R201	1kΩ	0.25W	ZD101	1N4746	18V, 1W	
R202	1kΩ	0.25W	ZD102	Open		
R203	39kΩ	0.25W	ZD201	1N5231	5.1V, 0.5W	
R204	4.7kΩ	0.25W, 1%	D201	1N4148	0.15A, 50V	
R205	220kΩ	0.25W, 1%	D202	EGP20J	2A, 600V	
R206	5.1kΩ	0.25W	D203	EGP20D	2A, 200V	
R207	5.1kΩ	0.25W	D204	EGP20D	2A, 200V	
R208	1kΩ	0.25W	D205	EGP20D	2A, 200V	
VR201	30kΩ			Bridge Did	ode	
	Capacito	or	BD101	GSIB660	6A, 600V	
C101	330n/275VAC	Box Capacitor	Line Filter		er	
C102	220μF/400V	Electrolytic	LF101		14mH	
C103	10μF/50V	Electrolytic	Transformer		er	
C104	10μF/50V	Electrolytic	T101	EER3540		
C105	3.9nF/50V	Film Capacitor	Switch			
C106	47nF/50V	Film Capacitor	SW201	ON/OFF	For MCU Signal	
C107	680pF/1kV	Film Capacitor	IC			
C108	Open		IC101	FSCQ0565RT	TO-220F-5L	
C201	100μF/160V	Electrolytic	OPT101	FOD817A		
C202	47μF/160V	Electrolytic	Q201	KA431LZ	TO-92	
C203	1000μF/35V	Electrolytic	Q202	KSC945		
C204	1000μF/35V	Electrolytic				
C205	1000μF/35V	Electrolytic				
C206	22nF/50V	Film Capacitor				
C207	470pF/1kV	Ceramic Capacitor				
C208	470pF/1kV	Ceramic Capacitor				
C209	470pF/1kV	Ceramic Capacitor				

FSCQ0765RT Typical Application Circuit

Application	Output Power	Input Voltage	Output Voltage (Max Current)
C-TV	83W	Universal input	12V (1A)
		(90-270 Vac)	18V (0.5A)
			125V (0.4A)
			24V (0.5A)

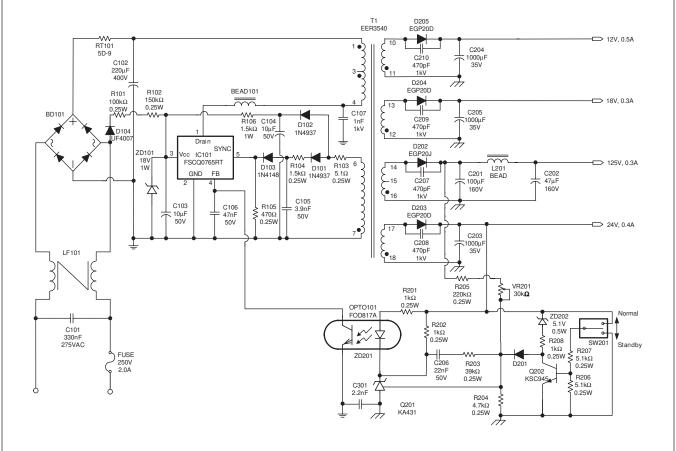
Features

- High Efficiency (>83% at 90 Vac Input)
- Wider Load Range through the Extended Quasi-Resonant Operation
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- Internal Soft-Start (20ms)

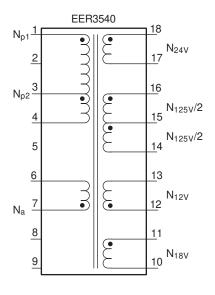
Key Design Notes

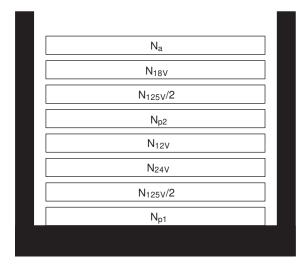
24V output is designed to drop to around 8V in standby mode

1. Schematic



2. Transformer Schematic Diagram





3. Winding Specification

No	Pin (s→f)	Wire	Turns	Winding Method
N _{p1}	1–3	$0.5^{\phi} \times 1$	32	Center Winding
N _{125V} /2	16–15	$0.5^{\phi} \times 1$	32	Center Winding
N _{24V}	18–17	$0.4^{\phi} \times 2$	13	Center Winding
N _{12V}	12–13	$0.5^{\phi} \times 2$	7	Center Winding
N _{p2}	3–4	$0.5^{\phi} \times 1$	32	Center Winding
N _{125V} /2	15–14	$0.5^{\phi} \times 1$	32	Center Winding
N _{18V}	11–10	$0.4^{\circ} \times 2$	10	Center Winding
N _a	7–6	$0.3^{\phi} \times 1$	20	Center Winding

4. Electrical Characteristics

	Pin	Specification	Remarks
Inductance	1–3	515μH ± 5%	1kHz, 1V
Leakage Inductance	1–3	10μH Max	2nd all short

5. Core & Bobbin

Core: EER3540 Bobbin: EER3540 Ae: 107 mm²