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FAIRCHILD SEMICONDUCTOR®

November 2009

FSUSB11 — Low-Power, Full-Speed (12Mbps) Switch

Features

- Space Saving MicroPak™ (1.6 x 2.1mm)
- USB 1.1 Signal Switching Compliant
- 3db Bandwidth: >350MHz
- Maximum 1.15Ω R_{ON} at 4.5V V_{CC} and 4Ω for 2.7V Supply
- 0.3Ω Maximum R_{ON} Flatness for +5V Supply
- Broad V_{CC} Operating Range: 1.65V to 5.5V
- Fast Turn-On and Turn-Off Time
- Break-Before-Make Enable Circuitry
- Over-Voltage Tolerant, TTL-Compatible Control Input

Applications

- Cell Phones, PDAs, Digital Cameras, Notebook Computers

Description

The FSUSB11 is a high-performance, dual Single-Pole Double-Throw (SPDT) switch designed for switching USB 1.1 signals. The device features ultra-low on resistance (R_{ON}) of 1.15Ω maximum at 4.5V V_{CC} and 4.3Ω at 2.7V supply. High bandwidth and ultra low (R_{ON}) make this switch able to pass both USB low- and full-speed signal with minimum signal distortion. The device is fabricated with sub-micron CMOS technology to achieve fast switching speeds and designed for break-before-make operation. The select input is TTL-level compatible.

Ordering Information

Part Number	Operating Temperature Range	Eco Status	Package	Packing Method
FSUSB11L10X	-40 to +85°C	RoHS	10-Lead, MicroPak™, JEDEC MO255,1.6 X 2.1mm	Tape and Reel
FSUSB11MTCX	-40 to +85°C	RoHS	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide	Tape and Reel

For Fairchild's definition of Eco Status, please visit: http://www.fairchildsemi.com/company/green/rohs_green.html.

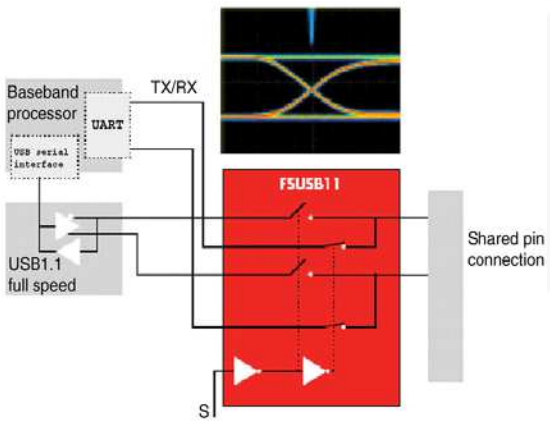


Figure 1. Block Diagram

MicroPak™ is a trademark of Fairchild Semiconductor Corporation.

Pin Configuration

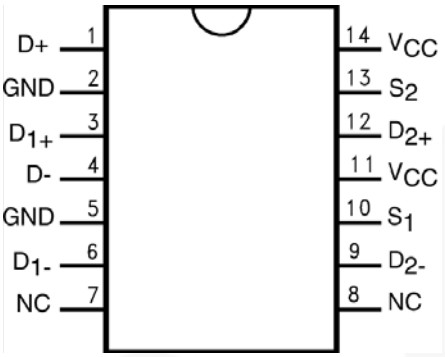


Figure 2. TSSOP Pin Assignment (Top View)

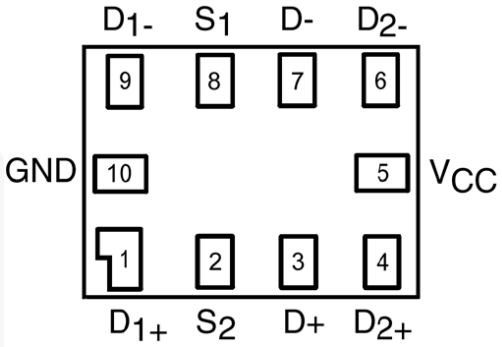


Figure 3. Micropak™ Pin Assignment (Top View)

Analog Symbol

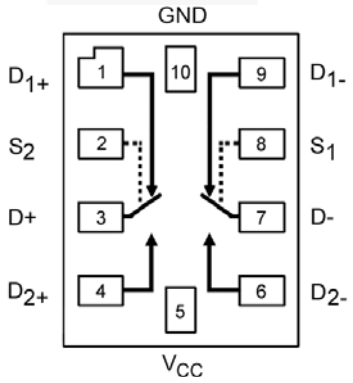


Figure 4. Analog Symbol

Pin Descriptions

TSSOP Pin #	MicroPak™ Pin #	Pin Names	Description
1, 3, 4, 6, 9, 12	1, 3, 4, 6, 7, 9	D+, D_{1+}, D-, D_{1-}, D_{2-}, D_2+	Data Ports
2, 5	10	GND	Ground
7, 8		NC	No Connect
10, 13	2, 8	S_1, S_2	Control Input
11, 14	5	V_{CC}	Supply Voltage

Truth Table

Control Inputs	Function
Low Logic Level	D_1 Connected to D+/D-
High Logic Level	D_2 Connected to D+/D-

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply Voltage	-0.5	6.0	V
V_S	Switch Voltage	-0.5	V_{CC} + 0.5	V
V_{IN}	Input Voltage[1]	-0.5	6.0	V
I_{IK}	Input Diode Current	-50		mA
I_{SW}	Switch Current		200	mA
I_{SWPEAK}	Peak Switch Current (Pulsed at 1ms Duration, <10% Duty Cycle)		400	mA
T_{STG}	Storage Temperature Range	-65	+150	°C
T_J	Maximum Junction Temperature		+150	°C
T_L	Lead Temperature (Soldering, 10 Seconds)		+260	°C
ESD	Human Body Model, JESD22-A114		8	kV

Note:

1. The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Power Supply	1.65	5.50	V
V_{IN}	Control Input Voltage[2]	0	V_{CC}	V_{CC}
V_{SW}	Switch Input Voltage	0	V_{CC}	V_{CC}
T_A	Operating Temperature	-40	+85	°C

Note:

2. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Unless otherwise specified, typical values are at +25°C.

Symbol	Parameter		Conditions	V_{CC} (V)	T_A=+25°C			T_A=-40 to +85°C		Units
					Min.	Typ.	Max.	Min.	Max.	
V_{IH}	Input Voltage High			2.7 to 3.6				2.0		V
				4.5 to 5.5				4.0		
V_{IL}	Input Voltage Low			2.7 to 3.6						V
				4.5 to 5.5						
I_{IN}	Control Input Leakage		V_{IN}=0V to V_{CC}	2.7 to 3.6						µA
				4.5 to 5.5						
$I_{NO(OFF)}$, $I_{NO(OFF)}$	Off-Leakage Current of Port D_1 and D_2		A=1V, 4.5V, B_0 or B_1=1V, 4.5V	5.5	-50		50	-100	100	nA
$I_{A(ON)}$	On-Leakage Current of Port D		A=1V, 4.5V, B_0 or B_1=1V, 4.5V or Floating	5.5	50		50	-100	100	nA
R_{ON}	Switch On Resistance[3]	Micropak	I_{OUT}= 100mA, D_1 or D_2=1.5V	2.7		2.60	4.00		4.30	Ω
			I_{OUT}= 100mA, D_1 or D_2=3.5V	4.5		0.95	1.15		1.30	
		TSSOP	I_{OUT}= 100mA, D_1 or D_2=1.5V	2.7		2.80			4.50	
			I_{OUT}= 100mA, D_1 or D_2=3.5V	4.5		1.50			3.00	
ΔR_{ON}	On Resistance Matching Between Channel[4]	Micropak	I_{OUT}= 100mA, D_1 or D_2=3.5V	4.5		0.06	0.12		0.15	Ω
		TSSOP				0.07			0.30	
$R_{FLAT(ON)}$	On Resistance Flatness[5]		I_{OUT}=100mA, D_1 or D_2=0V, 0.75V, 1.5V	2.7		1.4				Ω
			I_{OUT}=100mA, B_0 or B_1=0V, 1V, 2V	4.5		0.2	0.3		0.4	
I_{CC}	Quiescent Supply Current		V_{IN}=0V or V_{CC}, I_{OUT}=0	3.6		0.1	0.5		1.0	µA
				5.5		0.1	0.5		1.0	

Notes:

3. On resistance is determined by the voltage drop between D and Dn pins at the indicated current through the switch.
4. $\Delta R_{ON} = R_{ONmax} - R_{ONmin}$ measured at identical V_{CC}, temperature, and voltage.
5. Flatness is defined as the difference between the maximum and minimum value of on resistance over the specified range of conditions.

AC Electrical Characteristics

Unless otherwise specified, typical values are at +25°C.

Symbol	Parameter	Conditions	V_{CC}(V)	T_A=+25°C			T_A=-40 to +85°C		Units	Figure
				Min.	Typ.	Max.	Min.	Max.		
t_{ON}	Turn-on Time S-to-Bus B	D_1 or D_2=1.5V, R_L=50Ω, C_L=35pF	2.7 to 3.6			50		60	ns	Figure 5
		D_1 or D_2=3.0V, R_L=50Ω, C_L=35pF	4.5 to 5.5			35		30		
t_{OFF}	Turn-off Time S-to-Bus B	D_1 or D_2=1.5V, R_L=50Ω, C_L=35pF	2.7 to 3.6			20		20	ns	Figure 5
		D_1 or D_2=3.0V, R_L=50Ω, C_L=35pF	4.5 to 5.5			15				
t_{BBM}	Break-Before-Make Time	D_1 or D_2=1.5V, R_L=50Ω, C_L=35pF	2.7 to 3.6				1		ns	Figure 6
		D_1 or D_2=3.0V, R_L=50Ω, C_L=35pF	4.5 to 5.5		20		1			
Q	Charge Injection	C_L=1.0nF, V_{GEN}=0V, R_{GEN}=0Ω	2.7 to 3.6		20				pC	Figure 8
			4.5 to 5.5		10					
O_{IRR}	Off Isolation	f=1MHz, R_L=50Ω	2.7 to 3.6		-70				dB	Figure 7
			4.5 to 5.5		-70					
X_{TALK}	Non-Adjacent Channel Crosstalk	f=1MHz, R_L=50Ω	2.7 to 3.6		-75				dB	Figure 7
			4.5 to 5.5		-75					
BW	-3dB Bandwidth	R_L=50Ω	2.7 to 3.6		350				MHz	Figure 10
			4.5 to 5.5		350					

USB Related AC Electrical Characteristics

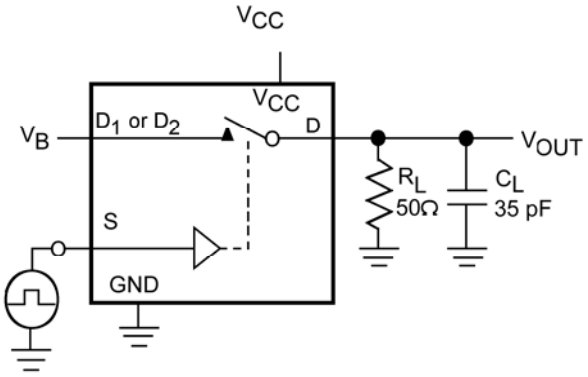
Unless otherwise specified, typical values are at 25°C.

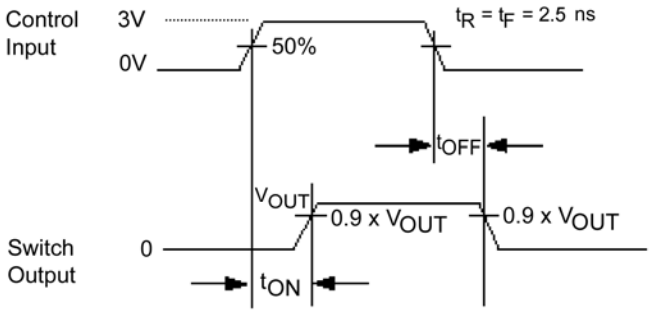
Symbol	Parameter	Conditions	V_{CC} (V)	T_A=+25°C			Units	Figure
				Min.	Typ.	Max.		
$t_{SK(O)}$	Skew	R_S=39, C_L=50pF, t_R=t_F=12ns at 12Mbps	2.7 to 3.6		0.15		ns	Figure 11
			4.5 to 5.5		0.15			
$t_{SK(P)}$	Rising/Fall Time Mismatch	(Duty Cycle=50%)	2.7 to 3.6		30		ps	Figure 12
			4.5 to 5.5		20			
T_J	Total Jitter	R_S=39, C_L=50pF, t_R=t_F=12ns at 12Mbps (PRBS=2^{15} 1)	2.7 to 3.6		1.7		ps	Figure 12
			4.5 to 5.5		1.6			

Capacitance

Symbol	Parameter	Conditions	V_{CC} (V)	T_A=+25°C			Units	Figure
				Min.	Typ.	Max.		
C_{IN}	Control Pin Input Capacitance	f=1MHz	0.0		3.5		pF	Figure 9
C_{OFF}	D_n Port Off Capacitance	f=1MHz	4.5		12.0		pF	Figure 9
C_{ON}	D Port On Capacitance	f=1MHz	4.5		40.0		pF	Figure 9

AC Loadings and Waveforms





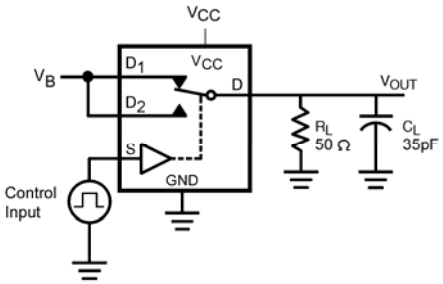
Note:

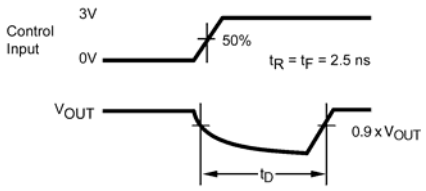
6. CL includes fixture and stray capacitance.

Note:

7. Logic input waveforms inverted for switches that have the opposite logic sense.

Figure 5. Turn On/ Turn Off Timing





Note:

8. C_L includes fixture and stray capacitance.

Figure 6. Break-Before-Make Timing

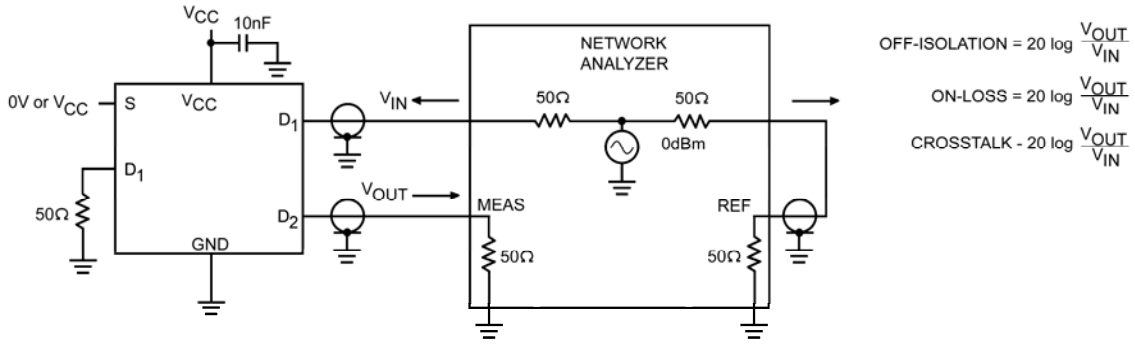
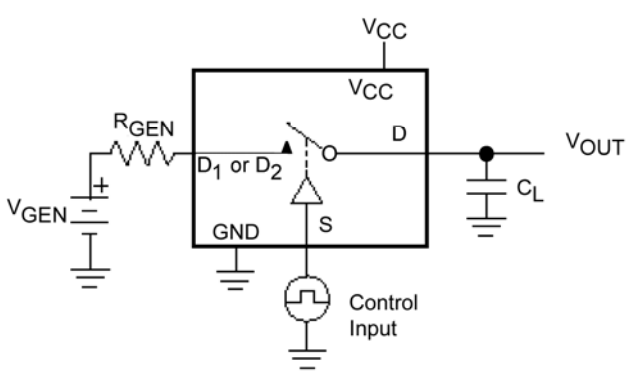
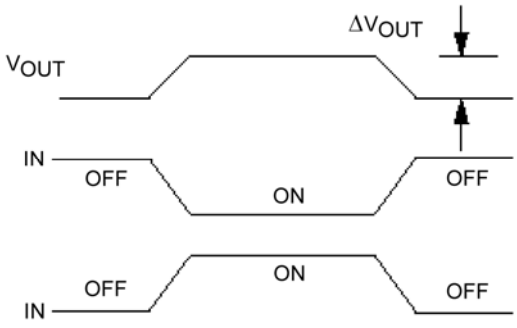


Figure 7. Off Isolation and Crosstalk

AC Loadings and Waveforms (Continued)





Note:

9. $Q=(\Delta V_{OUT})\,(C_L)$.

Figure 8. Charge Injection

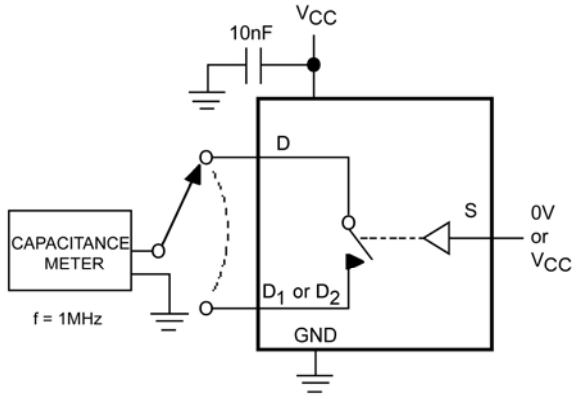


Figure 9. On/Off Capacitance Measurement Setup

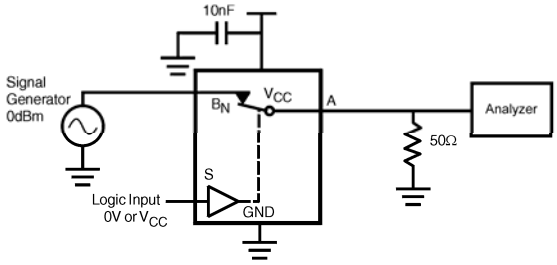
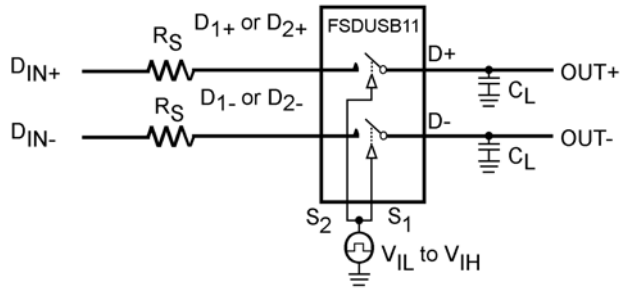


Figure 10. Bandwidth



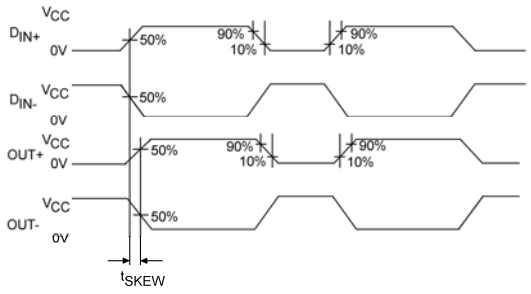
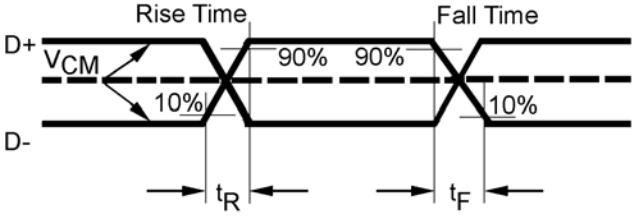


Figure 11. Skew Test



$$1.3V < V_{CM} < 2V$$

$$t_M = \frac{|t_R - t_F|}{\min(t_R, t_F)}$$

Figure 12. Rise/Fall Time Mismatch Test

Physical Dimensions

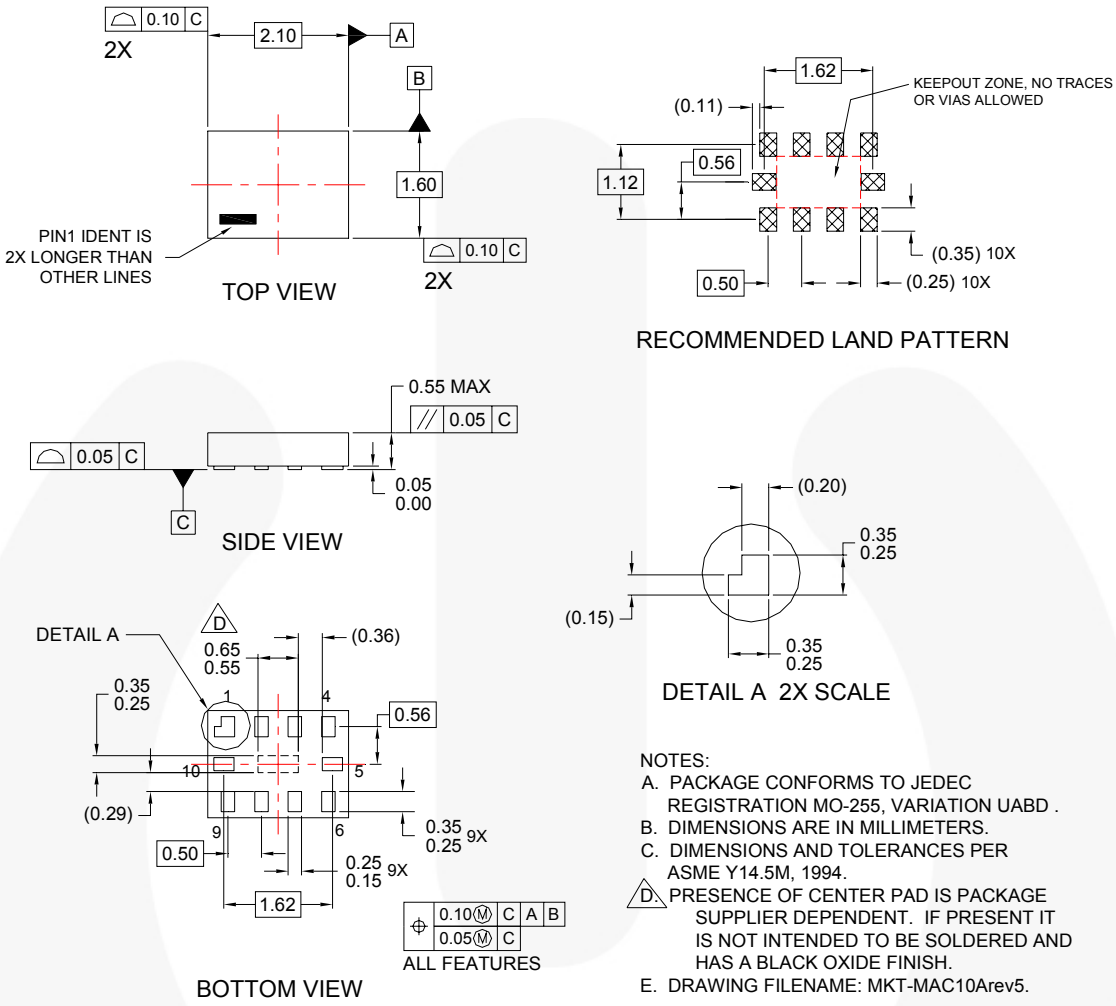


Figure 13. 10-Lead, MicroPak™, JEDEC MO255,1.6 X 2.1mm

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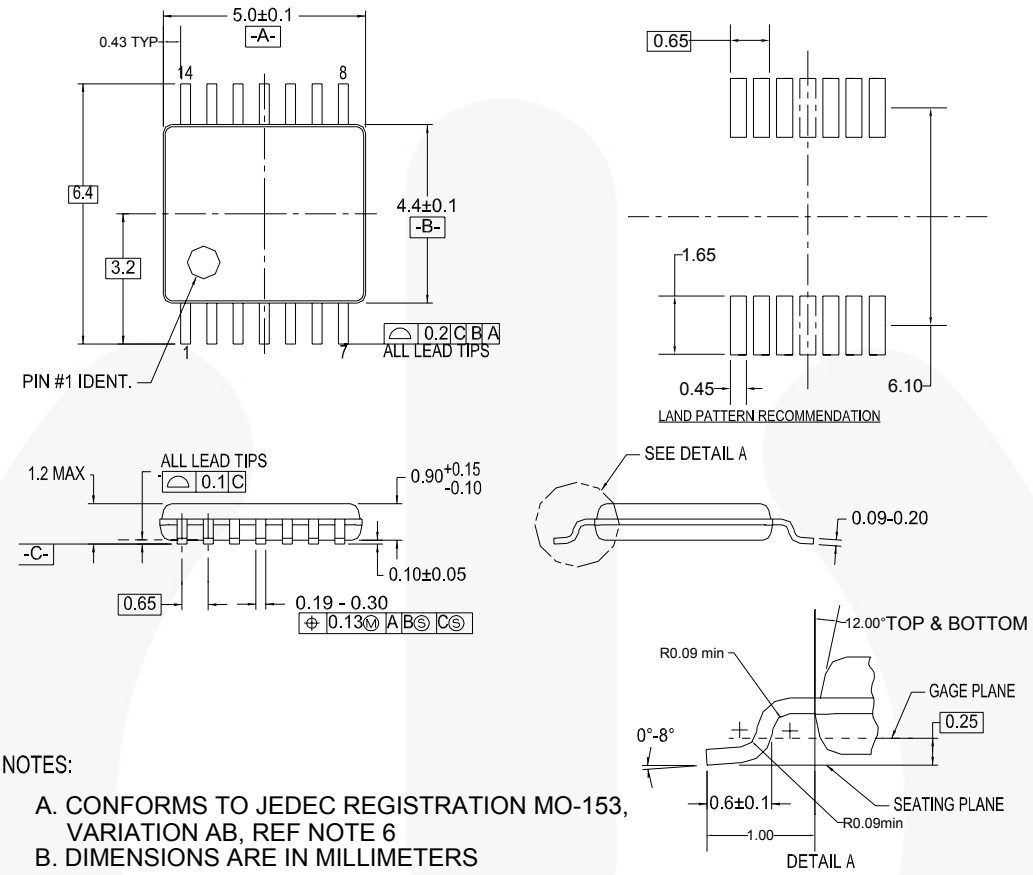
Tape and Reel Specification

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications:
http://www.fairchildsemi.com/products/logic/pdf/micropak_tr.pdf.

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
L10X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

Physical Dimensions



NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6
B. DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
E. LANDPATTERN STANDARD: SOP65P640X110-14M
F. DRAWING FILE NAME: MTC14REV6

Figure 14. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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SuperSOT™-8
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TinyLogic®
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PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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