Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

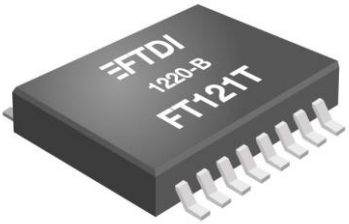
Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

Future Technology Devices International Ltd.

FT121

(Enhanced USB Device Controller with SPI Slave IC)



The FT121 is a USB generic interface controller with the following advanced features:

- USB 2.0 Full Speed compatible
- High performance USB device controller with integrated SIE, endpoint buffer, transceiver and voltage regulators
- Fully integrated clock generation with no external crystal required
- Supports Serial Parallel interface (SPI) slave to external microcontroller
- Supports up to 8 bi-directional endpoints with total 2K bytes endpoint buffer
- Max packet size is 504 bytes for isochronous endpoint and 64 bytes for control/bulk/interrupt endpoint
- Double buffer scheme for any endpoint increases data transfer throughput
- Multiple interrupt modes to facilitate both bulk and isochronous transfers
- USB Battery Charger detection allowing optimized charging profile
- Integrated DP pull-up resistor for USB connection
- Supports bus powered or self powered application
- VCC power supply operation at 3.3V or 5V
- Internal 1.8V and 3.3V LDO regulators
- VCC IO level range from 1.8V to 3.3V
- Integrated power-on-reset circuit
- UHCI/OHCI/EHCI host controller compatible
- -40°C to 85°C extended operating temperature range
- Available in Pb-free TSSOP-16 and QFN-16 packages (RoHS compliant)

1 Typical Applications

- Provide USB port to Microcontrollers
- USB Industrial Control
- Mass storage data transfers for multitude of embedded systems applications, including medical, industrial data-logger, power-metering, and test instrumentation
- Provide USB port to FPGA's
- Utilising USB to add system modularity
- Isochronous support for video applications in security, industrial control, and quality inspections

1.1 Part Numbers

Part Number	Package
FT121T-x	TSSOP-16
FT121Q-x	QFN-16

Note: Packaging codes for x is:

- R: Taped and Reel, (TSSOP is 2,500pcs per reel, QFN is 6,000pcs per reel).
- U: Tube packing, 96pcs per tube (TSSOP only)
- T: Tray packing, 490pcs per tray (QFN only)

For example: FT121T-R is 2,500pcs taped and reel packing

1.2 USB Compliant

At the time of writing this datasheet, the FT121 was in the process of completing USB compliance testing.

2 Block Diagrams

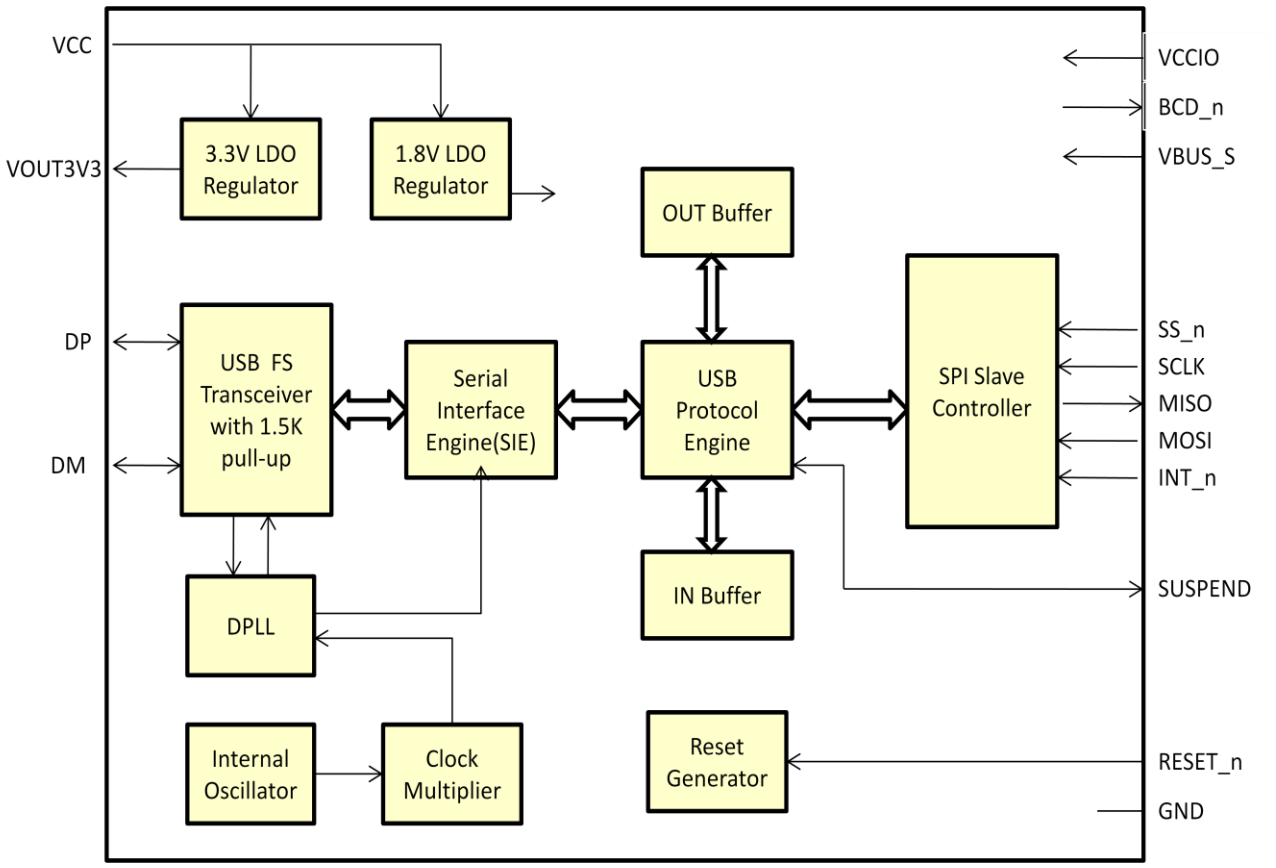


Figure 2-1 FT121 Block Diagram

For a description of each function please refer to Section 4.

Table of Contents

3 Device Pin Out and Signal Description

3.1 TSSOP-16 Package Pin Out

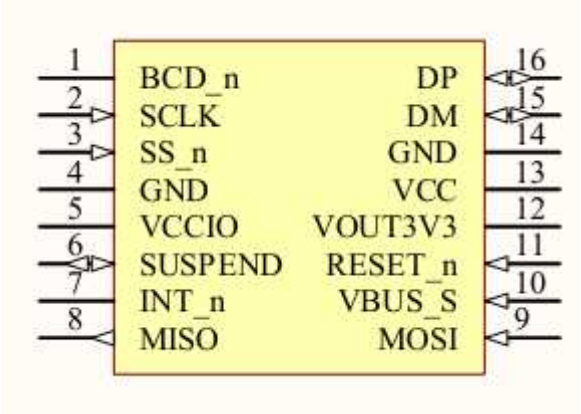


Figure 3-1 TSSOP-16 package schematic symbol

3.2 QFN-16 Package Pin Out

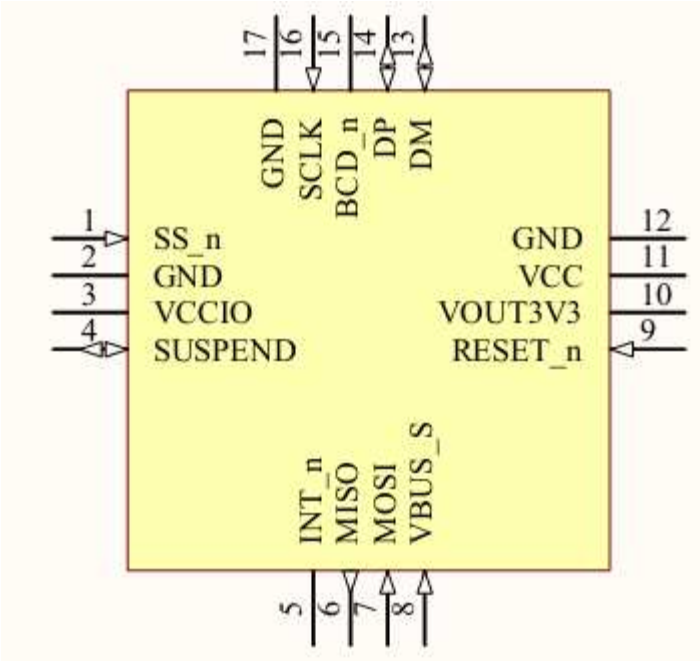


Figure 3-2 QFN-16 package schematic symbol

3.3 Pin Description

PIN No. (TSSOP-16)	PIN No. (QFN-16)	PIN NAME	TYPE	DESCRIPTION
1	15	BCD_n	OD	USB Charger detector output
2	16	SCLK	I	SPI clock input.
3	1	SS_n	I	SPI slave select input.
4	2	GND	P	Ground.
5	3	VCCIO	P	IO Supply Voltage; 1.8V, 2.5V or 3.3V
6	4	SUSPEND	I,OD	Device suspend (output) and wakeup (input).
7	5	INT_n	OD	Interrupt (Active Low).
8	6	MISO	O	4-wire mode: SPI slave output. 3-wire mode: no function. Leave it un-connected.
9	7	MOSI	I/IO	4-wire mode: SPI salve input 3-wire mode: SPI data input/output
10	8	VBUS_S	I	Vbus sensing input.
11	9	RESET_n	I	Asynchronous reset (Active Low).
12	10	VOUT3V3	P	3.3V regulator output for 5V operation; To operate the IC at 3.3 V, supply 3.3 V to both the VCC and VOUT3V3 pins
13	11	VCC	P	Power supply (3.3V or 5V)
14	12	GND	P	Ground.
15	13	DM	AIO	USB data signal minus
16	14	DP	AIO	USB data signal plus
-	17	GND	P	Ground. Die pad for QFN-16 package.

Table 3-1 FT121 Pin Description

Note: a) Pin name with suffix "_n" denotes active low input/output signal.

b) Symbol used for pin TYPE:

OD : Open Drain Output

O : Output

IO : Bi-directional Input and Output

I : Plain input

AIO : Analog Input and Output

P : Power or ground

4 Function Description

The FT121 is a USB device controller which interfaces with microcontrollers via an SPI slave interface.

4.1 Functional Block Descriptions

The following sections describe the function of each block. Please refer to the block diagram shown in **Figure 2-1**.

+1.8V LDO Regulator. The +1.8V LDO regulator generates the +1.8V reference voltage for the internal core of the IC with input capabilities from 3.3V or 5V.

+3.3V LDO Regulator. The +3.3V LDO regulator generates the +3.3V supply voltage for the USB transceiver. An external decoupling capacitor needs to be attached to the VOUT3V3 regulator output pin. The regulator also provides +3.3V power to the 1.5kΩ internal pull up resistor on DP pin. The allowable input voltages are 5V or 3.3V. When using 3.3V voltage as input voltage, the VCC and VOUT3V3 pins should be tied together. This will result in the regulator being by-passed.

USB Transceiver. The USB Transceiver cell provides the USB 1.1 / USB 2.0 full-speed physical interface. Output drivers provide +3.3V level slew rate control, while a differential input and two single ended input receivers provide data in, Single-Ended-0 (SE0) and USB reset detection conditions respectfully. A 1.5kΩ pull up resistor on DP is incorporated.

DPLL. The DPLL cell locks on to the incoming NRZI USB data and generates recovered clock and data signals.

Internal Oscillator. The Internal Oscillator cell generates a reference clock. This provides an input to the Clock Multiplier function.

Clock Multiplier. The 12MHz and 48MHz reference clock signals for various internal blocks can be generated from the reference clock via the oscillator functions and clock multiplier circuitry.

Serial Interface Engine (SIE). The Serial Interface Engine (SIE) block performs the parallel to serial and serial to parallel conversion of the USB data. In accordance with the USB 2.0 specification, it performs bit stuffing/un-stuffing and CRC5/CRC16 generation. It also checks the CRC on the USB data stream.

USB Protocol Engine. The USB Protocol Engine manages the data stream from the device USB control endpoint. It handles the low level USB protocol requests generated by the USB host controller. The Protocol Engine also includes a memory management unit which handles endpoint buffers.

OUT Buffer. Data sent from the USB host controller to FT121 via the USB data OUT endpoint is stored in the OUT buffer. Data is removed from the OUT buffer to system memory under control of the parallel interface block.

IN Buffer. Data from system memory is stored in the IN buffer. The USB host controller removes data from the IN buffer by sending a USB request for data from the device data IN endpoint.

RESET Generator. The integrated Reset Generator cell provides a reliable power-on reset to the device internal circuitry at power up. The RESET_n input pin allows an external device to reset the FT121.

SPI Controller Block. The SPI slave controller provides control and data interfaces between the external MCU and internal registers and endpoint buffers. It supports 4-wire (default) or 3-wire SPI operation.

4.2 Interrupt Modes

The FT121 interrupt pin (INT_n) can be programmed to generate an interrupt in different modes. The interrupt source can be any bit in the Interrupt Register, or receiving SOF packet, or both. The interrupt modes are selectable by two register bits, one is the SOF-only Interrupt Mode bit (bit 7 of Clock Division Factor register), and the other is the Interrupt Pin Mode bit (bit 5 of Interrupt Configuration register).

Interrupt mode	Bit SOF-only Interrupt Mode	Bit Interrupt Pin Mode	Interrupt source
0	0	0	Any bit in Interrupt register
1	0	1	Any bit in Interrupt register and SOF
2	1	X	SOF only

Table 4-1 Interrupt modes

4.3 SPI Slave Interface

The SPI slave interface supports 4-wire (default) and 3-wire operation. In 4-wire operation the SPI master will drive data on MOSI pin and the SPI slave will drive data on MISO pin. In 3-wire operation both SPI master and SPI slave share the same data pin (MOSI pin becomes bi-directional pin). Upon power-on or hardware reset, the FT121 SPI slave interface is in 4-wire mode. The 3-wire operation is enabled when a Set 3-wire command is issued to FT121.

The SPI protocol will follow a command + data format where a command is transmitted after SS_n is asserted and each subsequent byte will be a data byte. When all data bytes for this command are completed the SS_n is de-asserted. This can be seen in Figure 4-1.

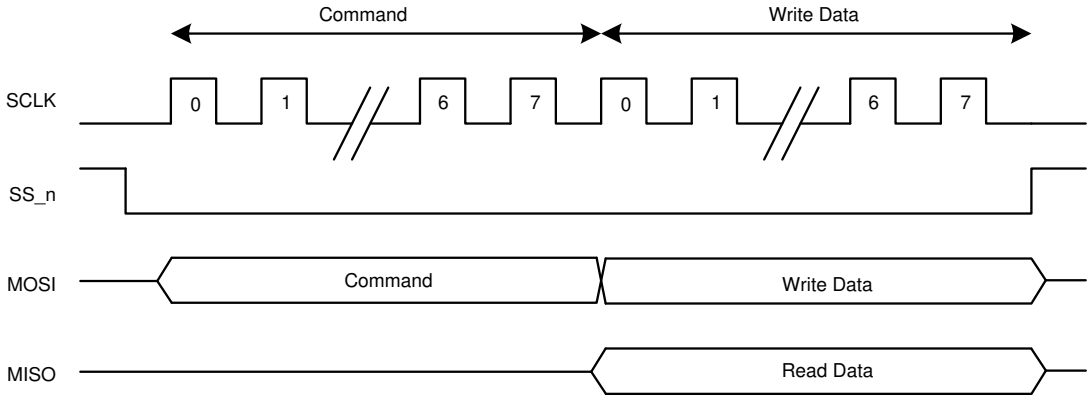


Figure 4-1 SPI access

The SPI slave supports SPI mode 1 (CPOL=0, CPHA=1). This means the rising edge is the driving edge while the falling edge is the sample edge. The drive edge is always before the sample edge.

The maximum SPI clock supported is 20MHz, for both 4-wire and 3-wire modes. Refer to the AC characteristics section for SPI timing figures.

4.3.1 4-wire write operation

When the SPI master performs data write operation, it drives the SS_n line low, send the 8-bit command byte on MOSI line, followed by sending the data bytes. The length of the data byte ranges from 0 to maximum 506, depending on the command type. The master will signal the end of the data write operation by drive the SS_n line high.

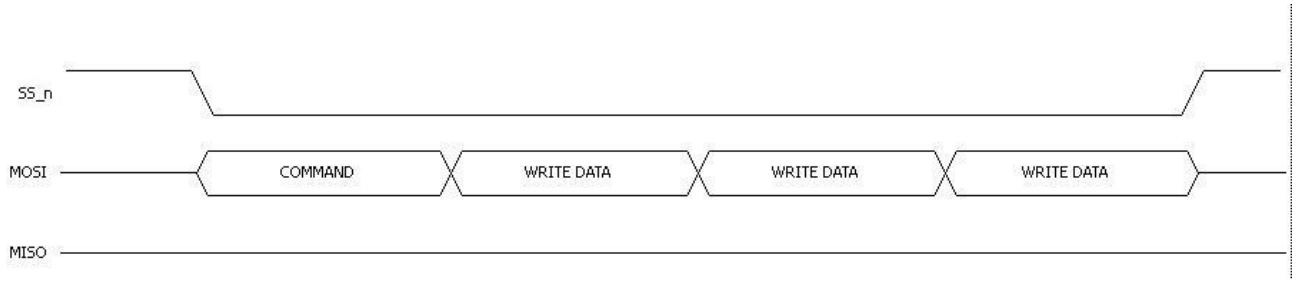


Figure 4-2 4-wire write operation

4.3.2 4-wire read operation

When the SPI master performs data read operation, it drives the SS_n line low, send the 8-bit command byte on MOSI line. The FT121 will output data bytes on the MISO line. The length of the data byte ranges from 0 to maximum 506, depending on the command type. The master will signal the end of the data read operation by drive the SS_n line high.

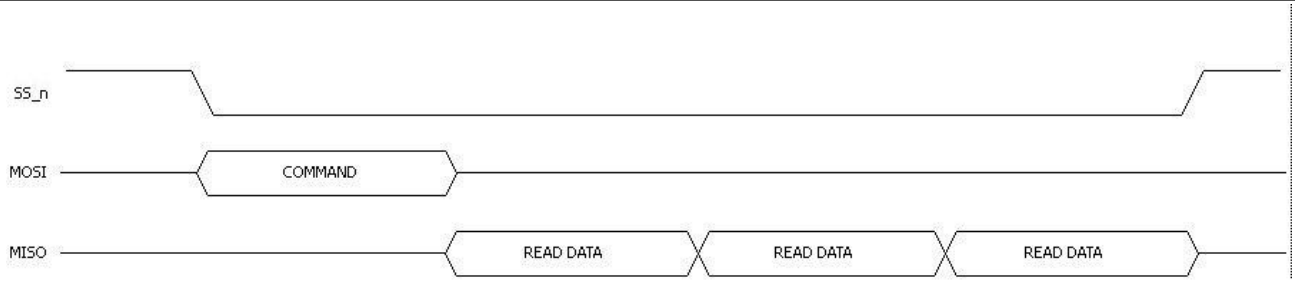


Figure 4-3 4-wire read operation

4.3.3 3-wire write operation

When the SPI master performs data write operation, it drives the SS_n line low, send the 8-bit command byte on MOSI line, followed by sending the data bytes. The length of the data byte ranges from 0 to maximum 506, depending on the command type. The master will signal the end of the data write operation by drive the SS_n line high.

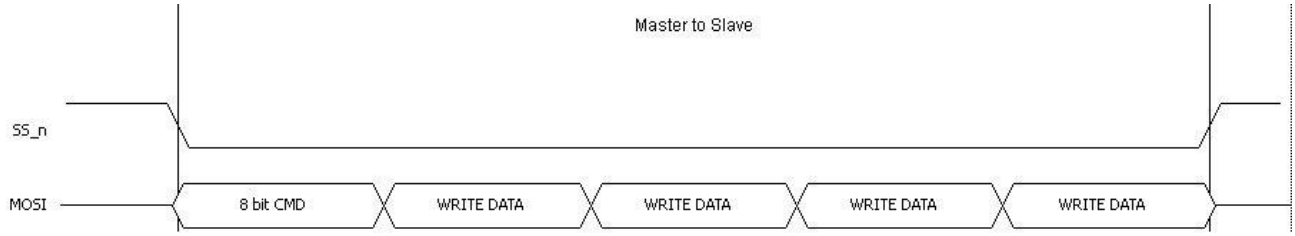


Figure 4-4 3-wire write operation

4.3.4 3-wire read operation

When the SPI master performs data read operation, it drives the SS_n line low, send the 8-bit command byte on MOSI line. The master will stop driving the MOSI line. The FT121 will output data bytes on the MOSI line. The length of the data byte ranges from 0 to maximum 506, depending on the command type. The master will signal the end of the data read operation by drive the SS_n line high.

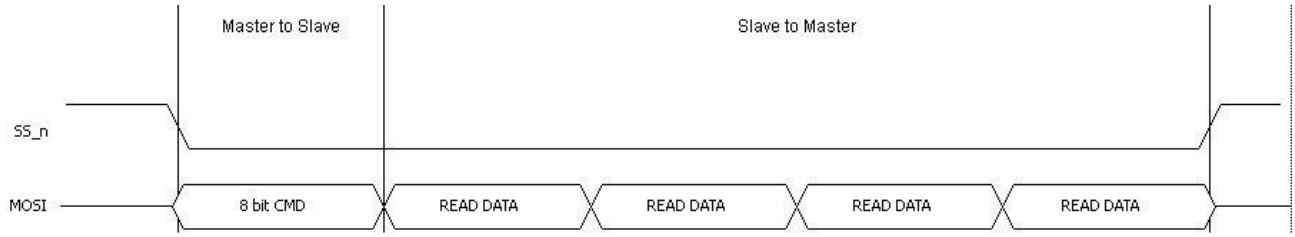


Figure 4-5 3-wire read operation

It is important that bus contention should be avoided during the bus turnaround period – i.e. moving from the command byte to a read byte. In this instance the master will stop driving at the same clock edge (rising edge) as the slave starts to drive. To avoid bus contention the FT121 will implement delays so that it only start to drive the MOSI line at least 5ns after the SCLK driving edge – this will give the master a minimum of 5ns to stop driving MOSI, which should ensure no bus contentions. At this bus turnaround point it's also more natural for a clash not to occur, as the master is the source of the clock, so will drive the clock and MOSI off at similar times. For the slave to drive MOSI it has to pass the clock

through the I/O buffers, into the internal circuits, clock MOSI and then get MOSI out through the output buffers. This long path in and out of the slave will have an inherent delay of a few nanoseconds.

5 Endpoint Buffer Management

The FT121 has 2 modes of operation for command and memory management: the default mode and the enhanced mode. The buffer management schemes are different in these two modes. Upon reset the default mode is functional. The enhanced mode is activated when any of the Set Endpoint Configuration command (B0h – BFh) is received.

5.1 Endpoint Buffer Management in Default Mode

In default mode the FT121 has 3 bi-directional endpoints (EP0, EP1 and EP2). EP0 is the control endpoint, with 16 bytes maximum packet size for both the control OUT and control IN endpoints. EP1 can be used as either a bulk endpoint or an interrupt endpoint, with 16 bytes maximum packet size for both OUT and IN endpoints. Table 5-1 shows the endpoint type and maximum packet size for EP0 and EP1.

Endpoint Number (EP)	Endpoint Index (EPI)	Endpoint Direction	Transfer Type	Max Packet Size
0	0	OUT	Control	16
	1	IN	Control	16
1	2	OUT	Bulk/Interrupt	16
	3	IN	Bulk/Interrupt	16

Table 5-1 Endpoint configuration for EP0 and EP1

EP2 is the primary endpoint. It can be configured as either bulk/interrupt or isochronous endpoint. The maximum packet size allowed for EP2 depends on the mode of configuration through Set Mode command. Table 5-2 shows all the 4 endpoint configuration modes for EP2.

EP2 Endpoint Configuration Mode	Endpoint Index (EPI)	Endpoint Direction	Transfer Type	Max Packet Size
0 (default)	4	OUT	Bulk/Interrupt	64
	5	IN	Bulk/Interrupt	64
1	4	OUT	Isochronous	128
2	5	IN	Isochronous	128
3	4	OUT	Isochronous	64
	5	IN	Isochronous	64

Table 5-2 Endpoint configuration for EP2

As the primary endpoint, EP2 is suitable for transmitting or receiving relatively large data. To improve the data throughput, EP2 is implemented with double buffereing. This allows the concurrent operation between USB bus access and MCU local bus access. For example, for EP2 IN endpoint (EPI5), the USB host can read data from FT121 Buffer 0 while the local MCU is writing to Buffer 1 at the same time. The USB host can subsequently read from FT121 Buffer 1 without waiting for it to be filled. Buffer switching is handled automatically by FT121.

5.2 Endpoint Buffer Management in Enhanced Mode

In enhanced mode the FT121 supports a dedicated 1kB buffer for IN packets and a dedicated 1kB buffer for OUT packets. The OUT/IN buffer can be allocated to any endpoint with the same direction, up to a maximum of 504 bytes double buffered (1008 bytes in total) to one endpoint. 504 is the maximum byte count as there are 1024 bytes in total per OUT/IN Buffer and 8 bytes for IN and OUT packets on control endpoint 0 must always be reserved. Control, interrupt and bulk endpoints can have a maximum packet size of 64 bytes and only isochronous endpoints can be allocated more than 64 bytes.

Isochronous modes can have larger buffer sizes as USB packets can be larger than 64 bytes for isochronous transfer. Isochronous buffers are managed in the same way as bulk, interrupt and control buffers – i.e. a buffer is for one USB packet only and will not span more than one USB packet.

An example of buffer configurations follows, where Configuration 1 and 2 have larger isochronous buffers.

Each cell indicates a 64 byte block

Configuration 0		Configuration 1		Configuration 2	
EP	Buffer	EP	Buffer	EP	Buffer
7	1	7 (ISO)	1	5 (ISO)	1
7	0				
6	1	7 (ISO)	0		
6	0				
5	1	6	1		
5	0	6	0		
4	1	2	1		
4	0	2	0	5 (ISO)	0
3	1	1 (ISO)	1		
3	0				
2	1				
2	0	1 (ISO)	0		
1	1				
1	0				
0	1	0	1	0	1
0	0	0	0	0	0

Table 5-3 Example buffer configuration

The endpoint buffer configurations, settable using the Set Endpoint Configuration command, are as follows:

Endpoint buffer size register setting (0b')	Non-isochronous endpoint	Isochronous endpoint
0000	8 bytes	16 bytes
0001	16 bytes	32 bytes
0010	32 bytes	48 bytes
0011	64 bytes	64 bytes
0100	-	96 bytes
0101	-	128 bytes
0110	-	160 bytes
0111	-	192 bytes
1000	-	256 bytes
1001	-	320 bytes
1010	-	384 bytes
1011	-	504 bytes
1100-1111	-	-

Table 5-4 Endpoint Maximum Packet Size

Note: 504 is the maximum byte count as there are 1024 bytes in total and 8 bytes IN and OUT packets for control endpoint 0 must always be reserved.

6 Commands and Registers

The FT121 supports two command sets: a default command set (Table 6-1) and an enhanced command set (Table 6-2). The enhanced command set is activated if any of the Set Endpoint Configuration commands (0xB0-0xBF) are received by the FT121. Otherwise, the default command set shall be valid.

6.1 Command Summary

Command Name	Target	Code (hex)	Data phase
Initialization Commands			
Set Address Enable	Device	D0h	Write 1 byte
Set Endpoint Enable	Device	D8h	Write 1 byte
Set Mode	Device	F3h	Write 2 bytes
Set Interrupt	Device	FBh	Write 1 byte
Data Flow Commands			
Read Interrupt Register	Device	F4h	Read 2 bytes
Select Endpoint	Endpoint 0 OUT	00h	Read 1 byte (optional)
	Endpoint 0 IN	01h	Read 1 byte (optional)
	Endpoint 1 OUT	02h	Read 1 byte (optional)
	Endpoint 1 IN	03h	Read 1 byte (optional)
	Endpoint 2 OUT	04h	Read 1 byte (optional)
	Endpoint 2 IN	05h	Read 1 byte (optional)
Read Last Transaction Status	Endpoint 0 OUT	40h	Read 1 byte
	Endpoint 0 IN	41h	Read 1 byte
	Endpoint 1 OUT	42h	Read 1 byte
	Endpoint 1 IN	43h	Read 1 byte
	Endpoint 2 OUT	44h	Read 1 byte
	Endpoint 2 IN	45h	Read 1 byte
Read Endpoint Status	Endpoint 0 OUT	80h	Read 1 byte
	Endpoint 0 IN	81h	Read 1 byte
	Endpoint 1 OUT	82h	Read 1 byte
	Endpoint 1 IN	83h	Read 1 byte
	Endpoint 2 OUT	84h	Read 1 byte

Command Name	Target	Code (hex)	Data phase
	Endpoint 2 IN	85h	Read 1 byte
Read Buffer	Selected Endpoint	E0h	Read multiple bytes
Write Buffer	Selected Endpoint	F0h	Write multiple bytes
Set Endpoint Status	Endpoint 0 OUT	50h	Write 1 byte
	Endpoint 0 IN	51h	Write 1 byte
	Endpoint 1 OUT	52h	Write 1 byte
	Endpoint 1 IN	53h	Write 1 byte
	Endpoint 2 OUT	54h	Write 1 byte
	Endpoint 2 IN	55h	Write 1 byte
Acknowledge Setup	Selected Endpoint	F1h	None
Clear Buffer	Selected Endpoint	F2h	None
Validate Buffer	Selected Endpoint	FAh	None
General Commands			
Read Current Frame Number	Device	F5h	Read 1 or 2 bytes
Send Resume	Device	F6h	None

Table 6-1 FT121 default command set

Command Name	Target	Code (hex)	Data phase
Initialization Commands			
Set Address Enable	Device	D0h	Write 1 byte
Set Endpoint Enable	Device	D8h	Write 1 byte
Set Mode	Device	F3h	Write 2 bytes
Set Interrupt	Device	FBh	Write 1 byte
Set Endpoint Configuration	Endpoint 0 OUT	B0h	Write 1 byte
	Endpoint 0 IN	B1h	Write 1 byte
	Endpoint 1 OUT	B2h	Write 1 byte
	Endpoint 1 IN	B3h	Write 1 byte
	Endpoint 2 OUT	B4h	Write 1 byte
	Endpoint 2 IN	B5h	Write 1 byte

Command Name	Target	Code (hex)	Data phase
	Endpoint 3 OUT	B6h	Write 1 byte
	Endpoint 3 IN	B7h	Write 1 byte
	Endpoint 4 OUT	B8h	Write 1 byte
	Endpoint 4 IN	B9h	Write 1 byte
	Endpoint 5 OUT	BAh	Write 1 byte
	Endpoint 5 IN	BBh	Write 1 byte
	Endpoint 6 OUT	BCh	Write 1 byte
	Endpoint 6 IN	BDh	Write 1 byte
	Endpoint 7 OUT	BEh	Write 1 byte
	Endpoint 7 IN	BFh	Write 1 byte
Data Flow Commands			
Read Interrupt Register	Device	F4h	Read 1 to 4 bytes
Select Endpoint	Endpoint 0 OUT	00h	Read 1 byte (optional)
	Endpoint 0 IN	01h	Read 1 byte (optional)
	Endpoint 1 OUT	02h	Read 1 byte (optional)
	Endpoint 1 IN	03h	Read 1 byte (optional)
	Endpoint 2 OUT	04h	Read 1 byte (optional)
	Endpoint 2 IN	05h	Read 1 byte (optional)
	Endpoint 3 OUT	06h	Read 1 byte (optional)
	Endpoint 3 IN	07h	Read 1 byte (optional)
	Endpoint 4 OUT	08h	Read 1 byte (optional)
	Endpoint 4 IN	09h	Read 1 byte (optional)
	Endpoint 5 OUT	0Ah	Read 1 byte (optional)
	Endpoint 5 IN	0Bh	Read 1 byte (optional)
	Endpoint 6 OUT	0Ch	Read 1 byte (optional)
	Endpoint 6 IN	0Dh	Read 1 byte (optional)
	Endpoint 7 OUT	0Eh	Read 1 byte (optional)
	Endpoint 7 IN	0Fh	Read 1 byte (optional)
Read Last Transaction Status	Endpoint 0 OUT	40h	Read 1 byte

Command Name	Target	Code (hex)	Data phase
	Endpoint 0 IN	41h	Read 1 byte
	Endpoint 1 OUT	42h	Read 1 byte
	Endpoint 1 IN	43h	Read 1 byte
	Endpoint 2 OUT	44h	Read 1 byte
	Endpoint 2 IN	45h	Read 1 byte
	Endpoint 3 OUT	46h	Read 1 byte
	Endpoint 3 IN	47h	Read 1 byte
	Endpoint 4 OUT	48h	Read 1 byte
	Endpoint 4 IN	49h	Read 1 byte
	Endpoint 5 OUT	4Ah	Read 1 byte
	Endpoint 5 IN	4Bh	Read 1 byte
	Endpoint 6 OUT	4Ch	Read 1 byte
	Endpoint 6 IN	4Dh	Read 1 byte
	Endpoint 7 OUT	4Eh	Read 1 byte
	Endpoint 7 IN	4Fh	Read 1 byte
Read Endpoint Status	Endpoint 0 OUT	80h	Read 1 byte
	Endpoint 0 IN	81h	Read 1 byte
	Endpoint 1 OUT	82h	Read 1 byte
	Endpoint 1 IN	83h	Read 1 byte
	Endpoint 2 OUT	84h	Read 1 byte
	Endpoint 2 IN	85h	Read 1 byte
	Endpoint 3 OUT	86h	Read 1 byte
	Endpoint 3 IN	87h	Read 1 byte
	Endpoint 4 OUT	88h	Read 1 byte
	Endpoint 4 IN	89h	Read 1 byte
	Endpoint 5 OUT	8Ah	Read 1 byte
	Endpoint 5 IN	8Bh	Read 1 byte
	Endpoint 6 OUT	8Ch	Read 1 byte
	Endpoint 6 IN	8Dh	Read 1 byte

Command Name	Target	Code (hex)	Data phase
	Endpoint 7 OUT	8Eh	Read 1 byte
	Endpoint 7 IN	8Fh	Read 1 byte
Read Buffer	Selected Endpoint	E0h	Read multiple bytes
Write Buffer	Selected Endpoint	F0h	Write multiple bytes
Set Endpoint Status	Endpoint 0 OUT	50h	Write 1 byte
	Endpoint 0 IN	51h	Write 1 byte
	Endpoint 1 OUT	52h	Write 1 byte
	Endpoint 1 IN	53h	Write 1 byte
	Endpoint 2 OUT	54h	Write 1 byte
	Endpoint 2 IN	55h	Write 1 byte
	Endpoint 3 OUT	56h	Write 1 byte
	Endpoint 3 IN	57h	Write 1 byte
	Endpoint 4 OUT	58h	Write 1 byte
	Endpoint 4 IN	59h	Write 1 byte
	Endpoint 5 OUT	5Ah	Write 1 byte
	Endpoint 5 IN	5Bh	Write 1 byte
	Endpoint 6 OUT	5Ch	Write 1 byte
	Endpoint 6 IN	5Dh	Write 1 byte
	Endpoint 7 OUT	5Eh	Write 1 byte
	Endpoint 7 IN	5Fh	Write 1 byte
Acknowledge Setup	Selected Endpoint	F1h	None
Clear Buffer	Selected Endpoint	F2h	None
Validate Buffer	Selected Endpoint	FAh	None
General Commands			
Send Resume	Device	F6h	None
Read Current Frame Number	Device	F5h	Read 1 or 2 bytes
Set 3-wire Mode	Device	E8h	None
Set IO Pad Drive Strength	Device	E9h	Write 1 byte

Command Name	Target	Code (hex)	Data phase
Read Vendor ID	Device	EBh	Read 2 bytes
Read Product ID	Device	EAh	Read 2 bytes
Read FTDI ID	Device	EDh	Read 1 byte

Table 6-2 enhanced command set

6.2 Initialization Commands

6.2.1 Set Address Enable

Command : D0h

Data : Write 1 byte

Bit	Symbol	Reset	Description
6-0	Address	0b'0000000	USB assigned device address. A bus reset will reset all address bits to 0.
7	Enable	0	Function enable. A bus reset will automatically enable the function at default address 0.

Table 6-3 Address Enable Register

6.2.2 Set Endpoint Enable

Command : D8h

Data : Write 1 byte

Bit	Symbol	Reset	Description
0	EP_Enable	0	Enable all endpoints (Note EP0 is always enabled regardless the setting of EP_Enable bit). Endpoints can only be enabled when the function is enabled.
7-1	Reserved	0b'0000000	Reserved, write to 0

Table 6-4 Endpoint Enable Register

6.2.3 Set Mode

Command : F3h

Data : Write 2 bytes

Bit	Symbol	Reset	Description
1-0	Reserved	0b'00	Reserved, write to 0

Bit	Symbol	Reset	Description
2	Clock Running	1	0: internal clocks stop during USB suspend 1: internal clocks continue running during USB suspend This bit must be set to '0' for bus powered application in order to meet the USB suspend current requirement. Note: The programmed value will not be changed by a bus reset.
3	Interrupt Mode	1	0: interrupt will not generate on NAK or Error transactions 1: interrupt will generate on NAK and Error transactions Note: The programmed value will not be changed by a bus reset.
4	DP_Pullup	0	0: Pullup resistor on DP pin disabled 1: Pullup resistor on DP pin enabled when Vbus is present Note: The programmed value will not be changed by a bus reset.
5	Reserved	0	Reserved, write to 0
7-6	Endpoint Configuration Mode	0b'00	Set the endpoint configuration mode for EP2. 00: Mode 0 (Non-ISO Mode) 01: Mode 1 (ISO-OUT Mode) 10: Mode 2 (ISO-IN Mode) 11: Mode 3 (ISO-IO Mode) In Enhanced Mode, these 2 bits are reserved. The Endpoint Configuration will be done through separate command. See "Set Endpoint Configuration" commands.

Table 6-5 Configuration Register (Byte 1)

Bit	Symbol	Reset	Description
3-0	Reserved	0b'1011	Reserved, write to 0b'1111
5-4	Reserved	0b'00	Reserved, write to 0
6	SET_TO_ONE	0	This bit must be set to 1
7	SOF-only Interrupt Mode	0	0: normal operation 1: interrupt will generate on receiving SOF packet only, regardless the value of the Interrupt Pin Mode bit in the Interrupt configuration register.

Table 6-6 Configuration Register (Byte 2)

6.2.4 Set Interrupt

Command : FBh

Data : Write 1 byte

Bit	Symbol	Reset	Description
4-0	Reserved	0b'00000	Reserved, write to 0b'00000
5	Interrupt Pin Mode	0	0: normal operation. Interrupt will generate if any bit in the interrupt register is set. 1: interrupt will generate upon receiving a SOF packet or if any bit in the interrupt register is set.
6	EPI4 Interrupt Enable	0	Interrupt Enable for endpoint index 4. For enhanced mode this bit has no function. EPI4 interrupt is always enabled.
7	EPI5 Interrupt Enable	0	Interrupt Enable for endpoint index 5. For enhanced mode this bit has no function. EPI5 interrupt is always enabled

Table 6-7 Interrupt Configuration Register

6.2.5 Set Endpoint Configuration (for Enhanced Mode)

Command : B0-BFh

Data : Write 1 byte

Bit	Symbol	Reset	Description
0	Endpoint Enabled	0	Enable or disable the endpoint index associated with the command
2-1	Endpoint Type	0b'00	Endpoint type 00: control 01: bulk or interrupt 10: isochronous 11: reserved
6-3	Max Packet Size	0b'0000	Maximum USB packet size for this endpoint. Defines the IN buffer or OUT buffer size for the endpoint. Refer to Table 5-4 for full details on the buffer configuration.
7	Reserved	0	Reserved, write to 0

Table 6-8 Endpoint Configuration Register

6.3 Data Flow Commands

6.3.1 Read Interrupt Register

Command : F4h

Data : Read 1 or 2 bytes (Default Mode); Read 1-4 bytes (Enhanced Mode)

Bit	Symbol	Reset	Description
0	Endpoint 0 Out	0	Interrupt for endpoint 0 OUT buffer. Cleared by Read Last Transaction Status command.
1	Endpoint 0 In	0	Interrupt for endpoint 0 IN buffer. Cleared by Read Last Transaction Status command.
2	Endpoint 1 Out	0	Interrupt for endpoint 1 OUT buffer. Cleared by Read Last Transaction Status command.
3	Endpoint 1 In	0	Interrupt for endpoint 1 IN buffer. Cleared by Read Last Transaction Status command.
4	Endpoint 2 Out	0	Interrupt for endpoint 2 OUT buffer. Cleared by Read Last Transaction Status command.
5	Endpoint 2 In	0	Interrupt for endpoint 2 IN buffer. Cleared by Read Last Transaction Status command.
6	Bus Reset	0	Interrupt for bus reset. This bit will be cleared after reading.
7	Suspend Change	0	Interrupt for USB bus suspend status change. This bit will be set to '1' when FT121 goes to suspend (missing 3 continuous SOFs) or resumes from suspend. This bit will be cleared after reading.

Table 6-9 Interrupt Register Byte 1

Bit	Symbol	Reset	Description
7-0	Reserved	00h	Reserved

Table 6-10 Interrupt Register Byte 2

Bit	Symbol	Reset	Description
0	Endpoint 3 Out	0	Interrupt for endpoint 3 OUT buffer. Cleared by Read Last Transaction Status command.
1	Endpoint 3 In	0	Interrupt for endpoint 3 IN buffer. Cleared by Read Last Transaction Status command.
2	Endpoint 4 Out	0	Interrupt for endpoint 4 OUT buffer. Cleared by Read Last Transaction Status command.
3	Endpoint 4 In	0	Interrupt for endpoint 4 IN buffer. Cleared by Read Last Transaction Status command.

Bit	Symbol	Reset	Description
4	Endpoint 5 Out	0	Interrupt for endpoint 5 OUT buffer. Cleared by Read Last Transaction Status command.
5	Endpoint 5 In	0	Interrupt for endpoint 5 IN buffer. Cleared by Read Last Transaction Status command.
6	Endpoint 6 Out	0	Interrupt for endpoint 6OUT buffer. Cleared by Read Last Transaction Status command.
7	Endpoint 6 In	0	Interrupt for endpoint 6 IN buffer. Cleared by Read Last Transaction Status command.

Table 6-11 Interrupt Register Byte 3 (for Enhanced Mode)

Bit	Symbol	Reset	Description
0	Endpoint 7 Out	0	Interrupt for endpoint 7 OUT buffer. Cleared by Read Last Transaction Status command.
1	Endpoint 7 In	0	Interrupt for endpoint 7 IN buffer. Cleared by Read Last Transaction Status command.
7-2	Reserved	0b'xxxxxx	Reserved

Table 6-12 Interrupt Register Byte 4 (for Enhanced Mode)