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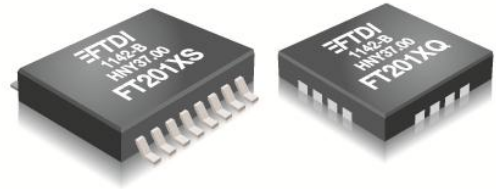
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Future Technology Devices International Ltd.

FT201X (USB I2C SLAVE IC)



The FT201X is a USB to I²C interface with the following advanced features:

- Single chip USB to I²C slave interface.
- Up to 3.4MHz, high speed mode, I²C supported
- Entire USB protocol handled on the chip. No USB specific firmware programming required.
- Fully integrated 2048 byte multi-time-programmable (MTP) memory, storing device descriptors and CBUS I/O configuration.
- Fully integrated clock generation with no external crystal required plus optional clock output selection enabling a glue-less interface to external MCU or FPGA.
- 512 byte receive buffer and 512 byte transmit buffer utilising buffer smoothing technology to allow for high data throughput.
- FTDI's royalty-free Virtual Com Port (VCP) and Direct (D2XX) drivers eliminate the requirement for USB driver development in most cases.
- Configurable CBUS I/O pins.
- Transmit and receive LED drive signals.
- USB Battery Charger Detection. Allows for USB peripheral devices to detect the presence of a higher power source to enable improved charging.
- Device supplied pre-programmed with unique USB serial number.
- USB Power Configurations; supports bus-powered, self-powered and bus-powered with power switching.
- Integrated +3.3V level converter for USB I/O.
- True 3.3V CMOS drive output and TTL input; Operates down to 1V8 with external pull-ups. Tolerant of 5V input.
- Configurable I/O pin output drive strength; 4 mA (min) and 16 mA (max).
- Integrated power-on-reset circuit.
- Fully integrated AVCC supply filtering - no external filtering required.
- + 5V Single Supply Operation.
- Internal 3V3/1V8 LDO regulators
- Low operating and USB suspend current; 8mA (active-typ) and 125uA (suspend-typ).
- UHCI/OHCI/EHCI host controller compatible.
- USB 2.0 Full Speed compatible.
- Extended operating temperature range; -40 to 85°C.
- Available in compact Pb-free 16 Pin SSOP and QFN packages (both RoHS compliant).

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1 Typical Applications

- Upgrading Legacy Peripherals to USB
- Utilising USB to add system modularity
- Incorporate USB interface to enable PC transfers for development system communication
- Motherboard and system monitoring through USB
- USB dongle implementations for Software/ Hardware Encryption and Wireless Modules
- Interfacing MCU/PLD/FPGA based designs to add USB connectivity
- USB Instrumentation
- USB Industrial Control
- USB Digital Camera Interface
- Ability to detect dedicated charging ports for high current charging of batteries in portable devices

1.1 Driver Support

Royalty free VIRTUAL COM PORT (VCP) DRIVERS for...

- Windows 8 32,64-bit
- Windows 7 32,64-bit
- Windows Vista and Vista 64-bit
- Windows XP and XP 64-bit
- Windows Embedded Operating Systems
- Server 2003, XP and Server 2008
- Windows CE 4.2, 5.0 and 6.0
- Mac OS-X
- Linux 3.2 and greater
- Android

Royalty free D2XX Direct Drivers (USB Drivers + DLL S/W Interface)

- Windows 8 32,64-bit
- Windows 7 32,64-bit
- Windows Vista and Vista 64-bit
- Windows XP and XP 64-bit
- Windows Embedded Operating Systems
- Server 2003, XP and Server 2008
- Windows CE 4.2, 5.0 and 6.0
- Mac OS-X
- Linux 2.6 and greater
- Android

The drivers listed above are all available to download for free from FTDI website (www.ftdichip.com). Various 3rd party drivers are also available for other operating systems - see FTDI website (www.ftdichip.com) for details.

For driver installation, please refer to <http://www.ftdichip.com/Documents/InstallGuides.htm>

1.2 Part Numbers

Part Number	Package
FT201XQ-x	16 Pin QFN
FT201XS-x	16 Pin SSOP

Note: Packing codes for x is:

- R: Taped and Reel, (SSOP is 3,000pcs per reel, QFN is 5,000pcs per reel).
- U: Tube packing, 100pcs per tube (SSOP only)
- T: Tray packing, 490pcs per tray (QFN only)

For example: FT201XQ-R is 5,000pcs taped and reel packing

1.3 USB Compliant

The FT201X is fully compliant with the USB 2.0 specification and has been given the USB-IF Test-ID (TID) 40001460 (Rev D).



2 FT201X Block Diagram

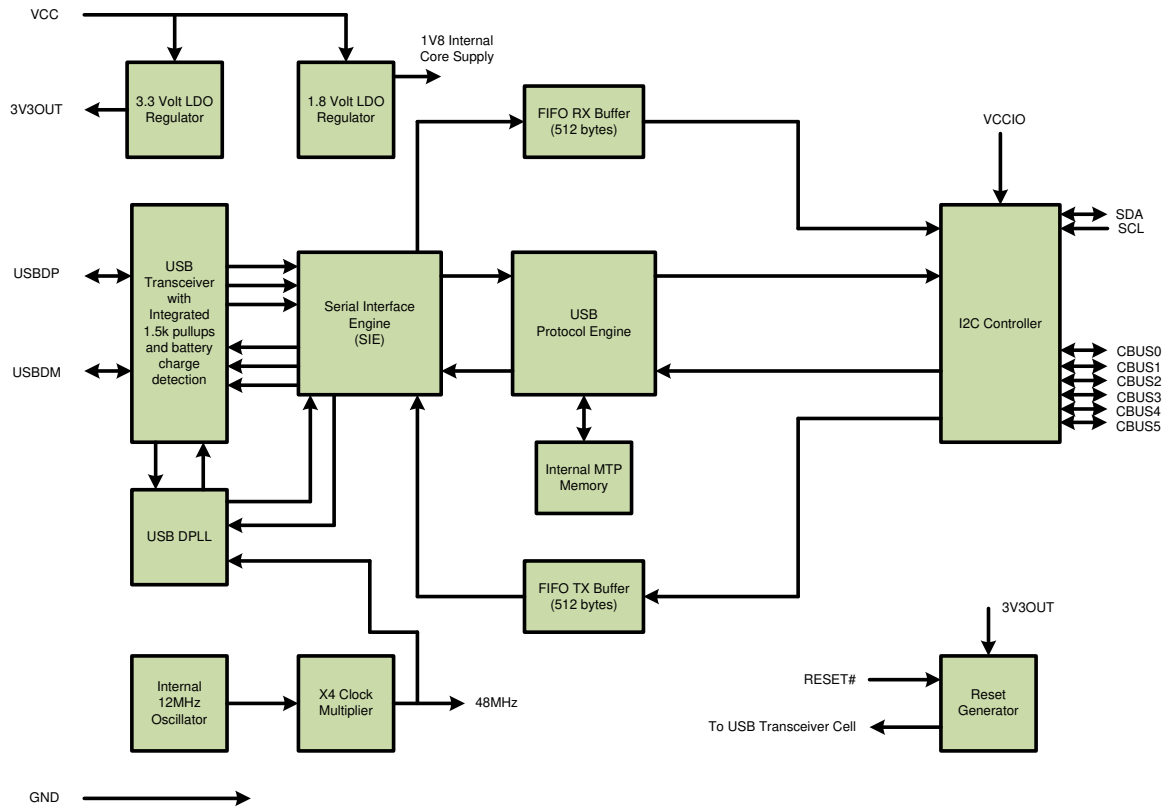


Figure 2.1 FT201X Block Diagram

For a description of each function please refer to Section 4.

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3 Device Pin Out and Signal Description

3.1 16-LD QFN Package

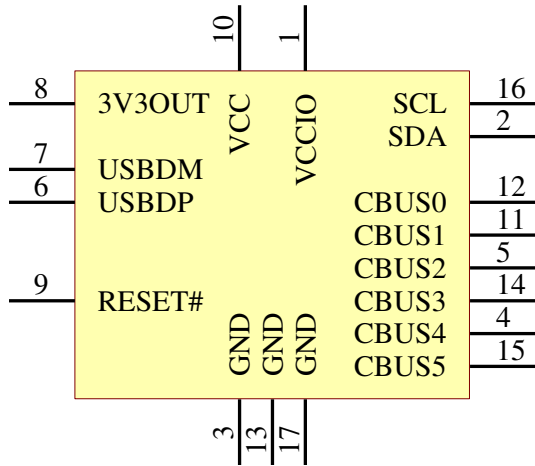


Figure 3.1 QFN Schematic Symbol

3.1.1 QFN Package PinOut Description

Note: # denotes an active low signal.

Pin No.	Name	Type	Description
10	** VCC	POWER Input	5 V (or 3V3) supply to IC
1	VCCIO	POWER Input	1V8 - 3V3 supply for the IO cells
8	** 3V3OUT	POWER Output	3V3 output at 50mA. May be used to power VCCIO. When VCC is 3V3; pin 8 is an input pin. Connect to pin 10.
3, 13	GND	POWER Input	0V Ground input.

Table 3.1 Power and Ground

*Pin 17 is centre pad beneath the IC. Connect to GND.

** If VCC is 3V3 then 3V3OUT must also be driven with 3V3 input

Pin No.	Name	Type	Description
7	USBDM	INPUT	USB Data Signal Minus.
6	USBDP	INPUT	USB Data Signal Plus.
9	RESET#	INPUT	Reset input (active low).

Table 3.2 Common Function pins

Pin No.	Name	Type	Description
2	SDA	I/O	I ² C bi-directional data line
16	SCL	Input	I ² C clock input
12	CBUS0	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device MTP memory. See CBUS Signal Options, Table 3.7.
11	CBUS1	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device MTP memory. See CBUS Signal Options, Table 3.7.
5	CBUS2	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device MTP memory. See CBUS Signal Options, Table 3.7.
14	CBUS3	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device MTP memory. See CBUS Signal Options, Table 3.7.
4	CBUS4	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device MTP memory. See CBUS Signal Options, Table 3.7.
15	CBUS5	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device MTP memory. See CBUS Signal Options, Table 3.7.

Table 3.3 I²C Interface and CBUS Group (see note 1)

Notes:

1. When used in Input Mode, the input pins are pulled to VCCIO via internal 75kΩ (approx) resistors. These pins can be programmed to gently pull low during USB suspend (PWREN# = "1") by setting an option in the MTP memory.

2. Clock stretching is not supported

3.2 16-LD SSOP Package

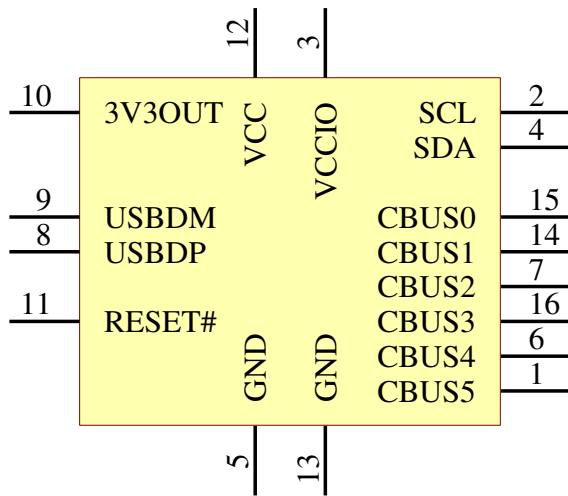


Figure 3.2 SSOP Schematic Symbol

3.2.1 SSOP Package PinOut Description

Note: # denotes an active low signal.

Pin No.	Name	Type	Description
12	** VCC	POWER Input	5 V (or 3V3) supply to IC
3	VCCIO	POWER Input	1V8 - 3V3 supply for the IO cells
10	** 3V3OUT	POWER Output	3V3 output at 50mA. May be used to power VCCIO. When VCC is 3V3, pin 10 is an input pin and should be connected to pin 12.
5, 13	GND	POWER Input	0V Ground input.

Table 3.4 Power and Ground

** If VCC is 3V3 then 3V3OUT must also be driven with 3V3 input

Pin No.	Name	Type	Description
9	USBDM	INPUT	USB Data Signal Minus.
8	USBDP	INPUT	USB Data Signal Plus.
11	RESET#	INPUT	Reset input (active low).

Table 3.5 Common Function pins

Pin No.	Name	Type	Description
4	SDA	I/O	I ² C bi-directional data line
2	SCL	Input	I ² C clock input
15	CBUS0	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device MTP memory. See CBUS Signal Options, Table 3.7.
14	CBUS1	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device MTP memory. See CBUS Signal Options, Table 3.7.
7	CBUS2	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device MTP memory. See CBUS Signal Options, Table 3.7.
16	CBUS3	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device MTP memory. See CBUS Signal Options, Table 3.7.
6	CBUS4	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device MTP memory. See CBUS Signal Options, Table 3.7.
1	CBUS5	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device MTP memory. See CBUS Signal Options, Table 3.7.

Table 3.6 Interface and CBUS Group (see note 1)

Notes:

1. When used in Input Mode, the input pins are pulled to VCCIO via internal 75kΩ (approx) resistors. These pins can be programmed to gently pull low during USB suspend (PWREN# = "1") by setting an option in the MTP memory.
2. Clock stretching is not supported

3.3 CBUS Signal Options

The following options can be configured on the CBUS I/O pins. CBUS signal options are common to both package versions of the FT201X. These options can be configured in the internal MTP memory using the software utility FT_PROG, which can be downloaded from the FTDI Utilities (www.ftdichip.com). The default configuration is described in Section 9.

CBUS Signal Option	Available On CBUS Pin	Description
TRI-STATE	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4, CBUS5	IO Pad is tri-stated
DRIVE 1	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4, CBUS5	Output a constant 1
DRIVE 0	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4, CBUS5	Output a constant 0
PWREN#	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4, CBUS5	Output is low after the device has been configured by USB, then high during USB suspend mode. This output can be used to control power to an external logic P-Channel logic level MOSFET switch. Enable the interface pull-down option when using the PWREN# in this way.
SLEEP#	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4, CBUS5	Goes low during USB suspend mode. Typically used to power down an external logic.
CLK24MHz	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4, CBUS5	24 MHz Clock output.*
CLK12MHz	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4, CBUS5	12 MHz Clock output.*
CLK6MHz	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4, CBUS5	6 MHz Clock output.*
GPIO	CBUS0, CBUS1, CBUS2, CBUS3,	CBUS bit bang mode option. Allows up to 4 of the CBUS pins to be used as general purpose I/O. Configured individually for CBUS0, CBUS1, CBUS2 and CBUS3 in the internal MTP memory. A separate application note, AN232R-01, available from FTDI website (www.ftdichip.com) describes in more detail how to use CBUS bit bang mode.
BCD Charger	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4, CBUS5	Battery charge Detect, indicates when the device is connected to a dedicated battery charger host. Active high output.
BCD Charger#	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4, CBUS5	Inverse of BCD Charger (open drain)
BitBang_WR#	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4, CBUS5	Synchronous and asynchronous bit bang mode WR# strobe output.
BitBang_RD#	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4, CBUS5	Synchronous and asynchronous bit bang mode RD# strobe output.
I2C_TXE#	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4, CBUS5	Transmit buffer empty, used to indicate to I ² C master device status of the FT201EX transmit buffer
I2C_RXF#	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4, CBUS5	Receive buffer full, used to indicate to I ² C master device status of FT201EX receive buffer

CBUS Signal Option	Available On CBUS Pin	Description
VBUS Sense	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4, CBUS5	Input to detect when VBUS is present.
Time Stamp	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4, CBUS5	Toggle signal which changes state each time a USB SOF is received
Keep_Awake#	CBUS0, CBUS1, CBUS2, CBUS3, CBUS4, CBUS5	Prevents the device from entering suspend state when unplugged. May be used if programming the MTP memory over I2C

Table 3.7 CBUS Configuration Control

*When in USB suspend mode the outputs clocks are also suspended.

4 Function Description

The FT201X is a USB to I²C interface device which simplifies USB implementations and reduces external component count by fully integrating into the device an EEPROM, and a clock circuit which requires no external crystal. It has been designed to operate efficiently with USB host controllers by using as little bandwidth as possible when compared to the total USB bandwidth available.

4.1 Key Features

Functional Integration. Fully integrated MTP memory, clock generation, AVCC filtering, Power-On-Reset (POR) and LDO regulators.

Configurable CBUS I/O Pin Options. The fully integrated MTP memory allows configuration of the Control Bus (CBUS) functionality and drive strength selection. There are 6 configurable CBUS I/O pins. These configurable options are defined in section 3.3.

The device is shipped with the most commonly used pin definitions pre-programmed - see Section 9 for details.

Asynchronous Bit Bang Mode with RD# and WR# Strokes. The FT201X supports FTDI's previous chip generation bit-bang mode. In bit-bang mode, the 2 I²C lines can be switched from the regular interface mode to a 2-bit general purpose I/O port. Data packets can be sent to the device and they will be sequentially sent to the interface at a rate controlled by an internal timer (equivalent to the baud rate pre-scalar). In the FT201X device this mode has been enhanced by outputting the internal RD# and WR# strobes signals which can be used to allow external logic to be clocked by accesses to the bit-bang I/O bus. This option will be described more fully in a separate application note available from FTDI website (www.ftdichip.com).

Synchronous Bit Bang Mode. The FT201X supports synchronous bit bang mode. This mode differs from asynchronous bit bang mode in that the interface pins are only read when the device is written to. This makes it easier for the controlling program to measure the response to an output stimulus as the data returned is synchronous to the output data. An application note, AN232R-01, available from FTDI website (www.ftdichip.com) describes this feature.

Source Power and Power Consumption. The FT201X is capable of operating at a voltage supply between +3.3V and +5.25V with a nominal operational mode current of 8mA and a nominal USB suspend mode current of 125µA. This allows greater margin for peripheral designs to meet the USB suspend mode current limit of 2.5mA. An integrated level converter within the I²C interface allows the FT201X to interface to UART logic running at +1.8V to +3.3V (5V tolerant).

4.2 Functional Block Descriptions

The following paragraphs detail each function within the FT201X. Please refer to the block diagram shown in Figure 2.1

Internal MTP Memory. The internal MTP memory in the FT201X is used to store USB Vendor ID (VID), Product ID (PID), device serial number, product description string and various other USB configuration descriptors. The internal MTP memory is also used to configure the CBUS pin functions. The FT201X is supplied with the internal MTP memory pre-programmed as described in Section 9. A user area of the internal MTP memory is available to system designers to allow storing of additional data from the user application over USB. The internal MTP memory descriptors can be programmed in circuit, over USB without any additional voltage requirement. The descriptors can be programmed using the FTDI utility software called FT_PROG, which can be downloaded from FTDI Utilities on the FTDI website (www.ftdichip.com). Additionally the MTP memory can be configured over the I²C interface.

+1.8V LDO Regulator. The +1.8V LDO regulator generates the +1.8V reference voltage for driving the internal core of the IC.

+3.3V LDO Regulator. The +3.3V LDO regulator generates the +3.3V reference voltage for driving the USB transceiver cell output buffers. It requires an external decoupling capacitor to be attached to the 3V3OUT regulator output pin. It also provides +3.3V power to the 1.5kΩ internal pull up resistor on USBDP. The main function of the LDO is to power the USB Transceiver and the Reset Generator Cells rather than to power external logic. However, it can be used to supply external circuitry requiring a +3.3V nominal supply with a maximum current of 50mA.

USB Transceiver. The USB Transceiver Cell provides the USB 1.1 / USB 2.0 full-speed physical interface to the USB cable. The output drivers provide +3.3V level slew rate control signalling, whilst a differential

input receiver and two single ended input receivers provide USB data in, Single-Ended-0 (SE0) and USB reset detection conditions respectfully. This function also incorporates a 1.5k Ω pull up resistor on USBDP. The block also detects when connected to a USB power supply which will not enumerate the device but still supply power and may be used for battery charging.

USB DPLL. The USB DPLL cell locks on to the incoming NRZI USB data and generates recovered clock and data signals for the Serial Interface Engine (SIE) block.

Internal 12MHz Oscillator - The Internal 12MHz Oscillator cell generates a 12MHz reference clock. This provides an input to the x4 Clock Multiplier function. The 12MHz Oscillator is also used as the reference clock for the SIE, USB Protocol Engine and UART FIFO controller blocks.

Clock Multiplier / Divider. The Clock Multiplier / Divider takes the 12MHz input from the Internal Oscillator function and generates the 48MHz, 24MHz, 12MHz and 6MHz reference clock signals. The 48MHz clock reference is used by the USB DPLL and the Baud Rate Generator blocks.

Serial Interface Engine (SIE). The Serial Interface Engine (SIE) block performs the parallel to serial and serial to parallel conversion of the USB data. In accordance with the USB 2.0 specification, it performs bit stuffing/un-stuffing and CRC5/CRC16 generation. It also checks the CRC on the USB data stream.

USB Protocol Engine. The USB Protocol Engine manages the data stream from the device USB control endpoint. It handles the low level USB protocol requests generated by the USB host controller and the commands for controlling the functional parameters of the I²C in accordance with the USB 2.0 specification chapter 9.

FIFO RX Buffer (512 bytes). Data sent from the USB host controller to the I²C interface via the USB data OUT endpoint is stored in the FIFO RX (receive) buffer. Data is removed from the buffer to the I²C transmit register under control of the I²C Controller. (Rx relative to the USB interface).

FIFO TX Buffer (512 bytes). Data from the I²C receive register is stored in the TX buffer. The USB host controller removes data from the FIFO TX Buffer by sending a USB request for data from the device data IN endpoint. (Tx relative to the USB interface).

I²C Controller. Module to handle the latching in and out of serial data on the I²C interface. Supports up to 3.4MHz, High Speed Serial Mode.

RESET Generator - The integrated Reset Generator Cell provides a reliable power-on reset to the device internal circuitry at power up. The RESET# input pin allows an external device to reset the FT201X.

RESET# can be tied to 3V3OUT.

5 I²C Interface Description

I²C (Inter Integrated Circuit) is a multi-master serial bus invented by Philips. I²C uses two bi-directional open-drain wires called serial data (SDA) and serial clock (SCL). Common I²C bus speeds are the 100 kbit/s standard mode (SM), 400 kbit/s fast mode (FM), 1 Mbit/s Fast mode plus (FM+), and 3.4 Mbit/s High Speed mode (HS)

An I²C bus node can operate either as a master or a slave:

- Master node – issues the clock and addresses slaves
- Slave node – receives the clock line and address.

The FT201X device shall only be able to operate as a slave, but is capable of speeds up to 3.4MBit/s. There are four potential modes of operation for a given bus device, although most devices only use a single role and its two modes:

- Master transmit – sending data to a slave
- Master receive – receiving data from a slave
- Slave transmit – sending data to a master
- Slave receive – receiving data from the master

The master is initially in master transmit mode by sending a start bit followed by the 7-bit address of the slave it wishes to communicate with, which is finally followed by a single bit representing whether it wishes to write(0) to or read(1) from the slave.

If the slave exists on the bus then it will respond with an ACK bit (active low for acknowledged) for that address. The master then continues in either transmit or receive mode (according to the read/write bit it sent), and the slave continues in its complementary mode (receive or transmit, respectively).

The address and the data bytes are sent most significant bit first. The start bit is indicated by a high-to-low transition of SDA with SCL high; the stop bit is indicated by a low-to-high transition of SDA with SCL high.

If the master wishes to write to the slave then it repeatedly sends a byte with the slave sending an ACK bit. (In this situation, the master is in master transmit mode and the slave is in slave receive mode.)

If the master wishes to read from the slave then it repeatedly receives a byte from the slave, the master sending an ACK bit after every byte but the last one. (In this situation, the master is in master receive mode and the slave is in slave transmit mode.)

The master then ends transmission with a stop bit, or it may send another START bit if it wishes to retain control of the bus for another transfer (a "combined message").

I²C defines three basic types of message, each of which begins with a START and ends with a STOP:

- Single message where a master writes data to a slave;
- Single message where a master reads data from a slave;
- Combined messages, where a master issues at least two reads and/or writes to one or more slaves

In a combined message, each read or write begins with a START and the slave address. After the first START, these are also called repeated START bits; repeated START bits are not preceded by STOP bits, which is how slaves know the next transfer is part of the same message.

Please refer to the I²C specification for more information on the protocol.

6 Devices Characteristics and Ratings

6.1 Absolute Maximum Ratings

The absolute maximum ratings for the FT201X devices are as follows. These are in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these may cause permanent damage to the device.

Parameter	Value	Unit	Conditions
Storage Temperature	-65°C to 150°C	Degrees C	
Floor Life (Out of Bag) At Factory Ambient (30°C / 60% Relative Humidity)	168 Hours (IPC/JEDEC J-STD-033A MSL Level 3 Compliant)*	Hours	
Ambient Operating Temperature (Power Applied)	-40°C to 85°C	Degrees C	
MTTF FT201XS	TBD	Hours	
MTTF FT201XQ	TBD	Hours	
VCC Supply Voltage	-0.3 to +5.5	V	
VCCIO IO Voltage	-0.3 to +4.0	V	
DC Input Voltage – USBDP and USBDM	-0.5 to +3.63	V	
DC Input Voltage – High Impedance Bi-directionals (powered from VCCIO)	-0.3 to +5.8	V	
DC Output Current – Outputs	22	mA	

Table 6.1 Absolute Maximum Ratings

* If devices are stored out of the packaging beyond this time limit the devices should be baked before use. The devices should be ramped up to a temperature of +125°C and baked for up to 17 hours.

6.2 ESD and Latch-up Specifications

Description	Specification
Human Body Mode (HBM)	> ± 2kV
Machine mode (MM)	> ± 200V
Charged Device Mode (CDM)	> ± 500V
Latch-up	> ± 200mA

Table 6.2 ESD and Latch-Up Specifications

6.3 DC Characteristics

DC Characteristics (Ambient Temperature = -40°C to +85°C)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
VCC	VCC Operating Supply Voltage	2.97	5	5.5	V	Normal Operation
VCC2	VCCIO Operating Supply Voltage	1.62	---	3.63	V	
Icc1	Operating Supply Current	6.4	8	8.65	mA	Normal Operation
Icc2	Operating Supply Current		125		μA	USB Suspend
3V3OUT	3.3v regulator output	2.97	3.3	3.63	V	VCC must be greater than 3V3 otherwise 3V3OUT is an input which must be driven with 3.3V

Table 6.3 Operating Voltage and Current

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.97	VCCIO	VCCIO	V	Ioh = -2mA I/O Drive strength* = 4mA
		2.97	VCCIO	VCCIO	V	I/O Drive strength* = 8mA
		2.97	VCCIO	VCCIO	V	I/O Drive strength* = 12mA
		2.97	VCCIO	VCCIO	V	I/O Drive strength* = 16mA
Vol	Output Voltage Low		0	0.4	V	Iol = +2mA I/O Drive strength* = 4mA
			0	0.4	V	I/O Drive strength* = 8mA
			0	0.4	V	I/O Drive strength* = 12mA
			0	0.4	V	I/O Drive strength* = 16mA
Vil	Input low Switching Threshold			0.8	V	LVTTTL
Vih	Input High Switching Threshold	2.0			V	LVTTTL
Vt	Switching Threshold		1.49		V	LVTTTL
Vt-	Schmitt trigger negative going threshold voltage		1.15		V	
Vt+	Schmitt trigger positive going threshold voltage		1.64		V	
Rpu	Input pull-up resistance	40	75	190	KΩ	Vin = 0
Rpd	Input pull-down resistance	40	75	190	KΩ	Vin = VCCIO
Iin	Input Leakage Current	-10	+/-1	10	μA	Vin = 0
Ioz	Tri-state output leakage current	-10	+/-1	10	μA	Vin = 5.5V or 0

Table 6.4 I/O Pin Characteristics VCCIO = +3.3V (except USB PHY pins)

* The I/O drive strength and slow slew-rate are configurable in the MTP memory.

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.25	VCCIO	VCCIO	V	Ioh = +/-2mA I/O Drive strength* = 4mA
		2.25	VCCIO	VCCIO	V	I/O Drive strength* = 8mA
		2.25	VCCIO	VCCIO	V	I/O Drive strength* = 12mA
		2.25	VCCIO	VCCIO	V	I/O Drive strength* = 16mA
Vol	Output Voltage Low		0	0.4	V	Iol = +/-2mA I/O Drive strength* = 4mA
			0	0.4	V	I/O Drive strength* = 8mA
			0	0.4	V	I/O Drive strength* = 12mA
			0	0.4	V	I/O Drive strength* = 16mA
Vil	Input low Switching Threshold			0.8	V	LVTTL
Vih	Input High Switching Threshold	0.8			V	LVTTL
Vt	Switching Threshold		1.1		V	LVTTL
Vt-	Schmitt trigger negative going threshold voltage		0.8		V	
Vt+	Schmitt trigger positive going threshold voltage		1.2		V	
Rpu	Input pull-up resistance	40	75	190	KΩ	Vin = 0
Rpd	Input pull-down resistance	40	75	190	KΩ	Vin = VCCIO
Iin	Input Leakage Current	-10	+/-1	10	μA	Vin = 0
Ioz	Tri-state output leakage current	-10	+/-1	10	μA	Vin = 5.5V or 0

Table 6.5 I/O Pin Characteristics VCCIO = +2.5V (except USB PHY pins)

* The I/O drive strength and slow slew-rate are configurable in the MTP memory.

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	1.62	VCCIO	VCCIO	V	Ioh = +/-2mA I/O Drive strength* = 4mA
		1.62	VCCIO	VCCIO	V	I/O Drive strength* = 8mA
		1.62	VCCIO	VCCIO	V	I/O Drive strength* = 12mA
		1.62	VCCIO	VCCIO	V	I/O Drive strength* = 16mA
Vol	Output Voltage Low		0	0.4	V	Iol = +/-2mA I/O Drive strength* = 4mA
			0	0.4	V	I/O Drive strength* = 8mA
			0	0.4	V	I/O Drive strength* = 12mA
			0	0.4	V	I/O Drive strength* = 16mA
Vil	Input low Switching Threshold			0.77	V	LVTTL
Vih	Input High Switching Threshold	1.6			V	LVTTL
Vt	Switching Threshold		0.77		V	LVTTL
Vt-	Schmitt trigger negative going threshold voltage		0.557		V	
Vt+	Schmitt trigger positive going threshold voltage		0.893		V	
Rpu	Input pull-up resistance	40	75	190	KΩ	Vin = 0
Rpd	Input pull-down resistance	40	75	190	KΩ	Vin = VCCIO
Iin	Input Leakage Current	-10	+/-1	10	μA	Vin = 0
Ioz	Tri-state output leakage current	-10	+/-1	10	μA	Vin = 5.5V or 0

Table 6.6 I/O Pin Characteristics VCCIO = +1.8V (except USB PHY pins)

 * The I/O drive strength and slow slew-rate are configurable in the **MTP memory**.

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	3V3OUT-0.2			V	
Vol	Output Voltage Low			0.2	V	
Vil	Input low Switching Threshold		-	0.8	V	
Vih	Input High Switching Threshold	2.0	-		V	

Table 6.7 USB I/O Pin (USBDP, USBDM) Characteristics

6.4 MTP Memory Reliability Characteristics

The internal 2048 Byte MTP memory has the following reliability characteristics:

Parameter	Value	Unit
Data Retention	10	Years
Write Cycle	2,000	Cycles
Read Cycle	Unlimited	Cycles

Table 6.8 MTP memory Characteristics

6.5 Internal Clock Characteristics

The internal Clock Oscillator has the following characteristics:

Parameter	Value			Unit
	Minimum	Typical	Maximum	
Frequency of Operation (see Note 1)	11.98	12.00	12.02	MHz
Clock Period	83.19	83.33	83.47	ns
Duty Cycle	45	50	55	%

Table 6.9 Internal Clock Characteristics

Note 1: Equivalent to +/-1667ppm

7 USB Power Configurations

The following sections illustrate possible USB power configurations for the FT201X. The illustrations have omitted pin numbers for ease of understanding since the pins differ between the FT201XS and FT201XQ package options.

All USB power configurations illustrated apply to both package options for the FT201X device. Please refer to Section 11 for the package option pin-out and signal descriptions.

7.1 USB Bus Powered Configuration

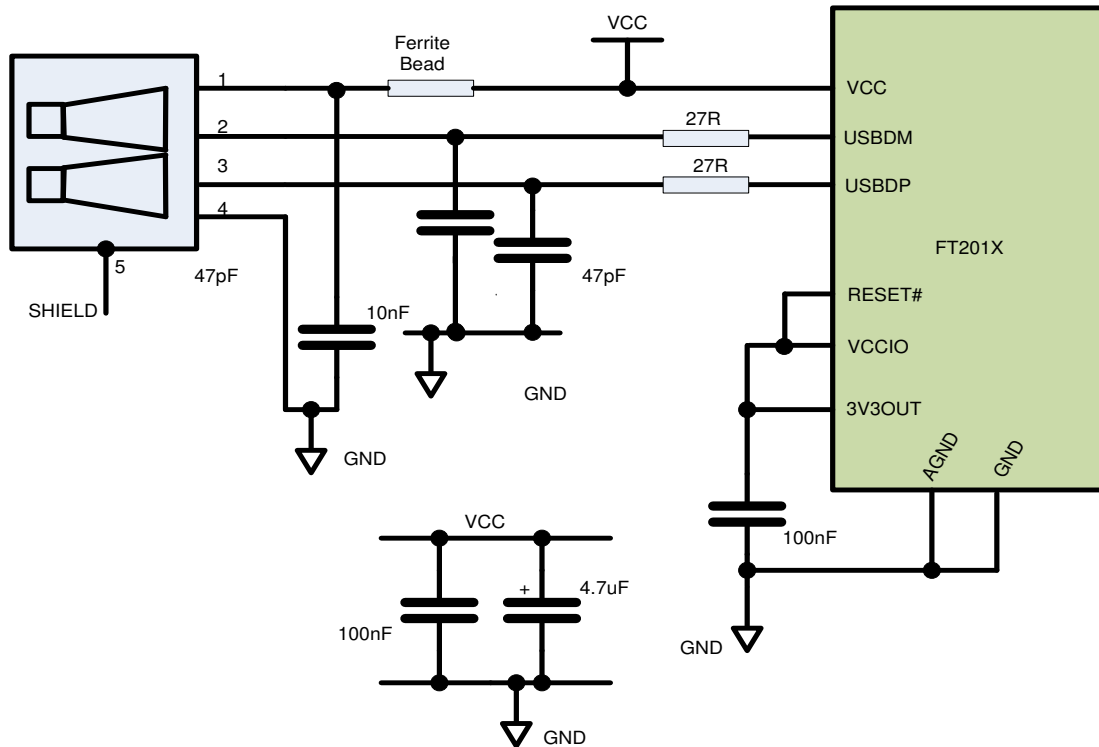


Figure 7.1 Bus Powered Configuration

Figure 7.1 Illustrates the FT201X in a typical USB bus powered design configuration. A USB bus powered device gets its power from the USB bus. Basic rules for USB bus power devices are as follows –

- i) On plug-in to USB, the device should draw no more current than 100mA.
- ii) In USB Suspend mode the device should draw no more than 2.5mA.
- iii) A bus powered high power USB device (one that draws more than 100mA) should use one of the CBUS pins configured as PWREN# and use it to keep the current below 100mA on plug-in and 2.5mA on USB suspend.
- iv) A device that consumes more than 100mA cannot be plugged into a USB bus powered hub.
- v) No device can draw more than 500mA from the USB bus.

The power descriptors in the internal MTP memory of the FT201X should be programmed to match the current drawn by the device.

A ferrite bead is connected in series with the USB power supply to reduce EMI noise from the FT201X and associated circuitry being radiated down the USB cable to the USB host. The value of the Ferrite Bead depends on the total current drawn by the application. A suitable range of Ferrite Beads is available from Laird Technologies (<http://www.lairdtech.com>), for example Laird Technologies Part # MI0805K601R-10.

Note: If using PWREN# (available using the CBUS) the pin should be pulled to VCCIO using a 10kΩ resistor.

7.2 Self Powered Configuration

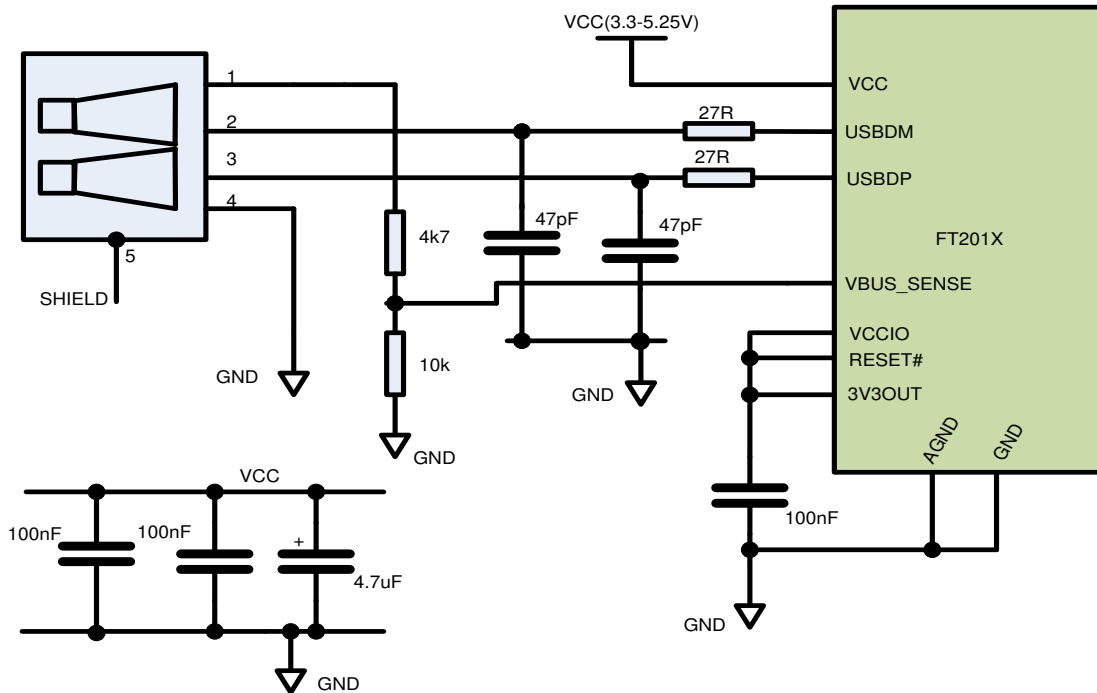


Figure 7.2 Self Powered Configuration

Figure 7.2 illustrates the FT201X in a typical USB self powered configuration. A USB self powered device gets its power from its own power supply, VCC, and does not draw current from the USB bus. The basic rules for USB self powered devices are as follows –

- i) A self powered device should not force current down the USB bus when the USB host or hub controller is powered down.
- ii) A self powered device can use as much current as it needs during normal operation and USB suspend as it has its own power supply.
- iii) A self powered device can be used with any USB host, a bus powered USB hub or a self powered USB hub.

The power descriptor in the internal MTP memory of the FT201X should be programmed to a value of zero (self powered).

In order to comply with the first requirement above, the USB bus power (pin 1) is used to control the VBUS_Sense pin of the FT201X device. When the USB host or hub is powered up an internal 1.5kΩ resistor on USBDP is pulled up to +3.3V, thus identifying the device as a full speed device to the USB host or hub. When the USB host or hub is powered off, VBUS_Sense pin will be low and the FT201X is held in a suspend state. In this state the internal 1.5kΩ resistor is not pulled up to any power supply (hub or host is powered down), so no current flows down USBDP via the 1.5kΩ pull-up resistor. Failure to do this may cause some USB host or hub controllers to power up erratically.

Figure 7.2 illustrates a self powered design which has a +3.3V to +5.25V supply.

Note:

1. When the FT201X is in reset, the interface I/O pins are tri-stated. Input pins have internal 75kΩ pull-up resistors to VCCIO, so they will gently pull high unless driven by some external logic.

7.3 USB Bus Powered with Power Switching Configuration

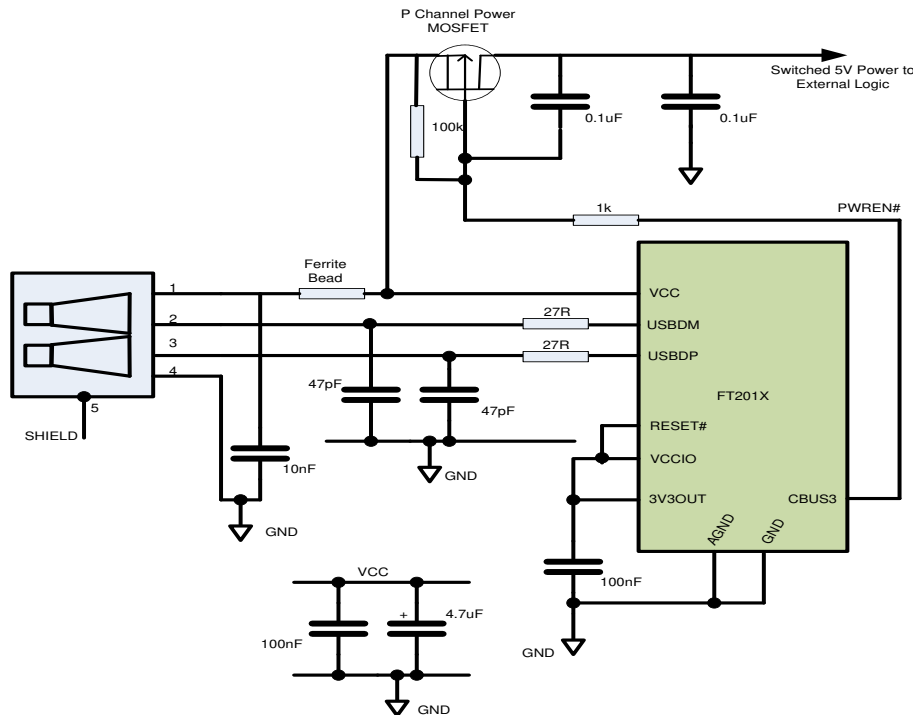


Figure 7.3 Bus Powered with Power Switching Configuration

A requirement of USB bus powered applications, is when in USB suspend mode, the application draws a total current of less than 2.5mA. This requirement includes external logic. Some external logic has the ability to power itself down into a low current state by monitoring the PWREN# signal. For external logic that cannot power itself down in this way, the FT201X provides a simple but effective method of turning off power during the USB suspend mode.

Figure 7.3 shows an example of using a discrete P-Channel MOSFET to control the power to external logic. A suitable device to do this is an International Rectifier (www.irf.com) IRLML6402, or equivalent. It is recommended that a "soft start" circuit consisting of a 1kΩ series resistor and a 0.1μF capacitor is used to limit the current surge when the MOSFET turns on. Without the soft start circuit it is possible that the transient power surge, caused when the MOSFET switches on, will reset the FT201X or the USB host/hub controller. The soft start circuit example shown in Figure 7.3 powers up with a slew rate of approximately 12.5V/ms. Thus supply voltage to external logic transitions from GND to +5V in approximately 400 microseconds.

As an alternative to the MOSFET, a dedicated power switch IC with inbuilt "soft-start" can be used. A suitable power switch IC for such an application is the Micrel (www.micrel.com) MIC2025-2BM or equivalent.

With power switching controlled designs the following should be noted:

- i) The external logic to which the power is being switched should have its own reset circuitry to automatically reset the logic when power is re-applied when moving out of suspend mode.
- ii) Set the Pull-down on Suspend option in the internal FT201X MTP memory.
- iii) One of the CBUS Pins should be configured as PWREN# in the internal FT201X MTP memory, and used to switch the power supply to the external circuitry.
- iv) For USB high-power bus powered applications (one that consumes greater than 100mA, and up to 500mA of current from the USB bus), the power consumption of the application must be set in the Max Power field in the internal FT201X MTP memory. A high-power bus powered application uses the descriptor in the internal FT201X MTP memory to inform the system of its power requirements.
- v) PWREN# gets its VCC from VCCIO. For designs using 3V3 logic, ensure VCCIO is not powered down using the external logic. In this case use the +3V3OUT.

8 Application Examples

The following sections illustrate possible applications of the FT201X. The illustrations have omitted pin numbers for ease of understanding since the pins differ between the FT201XS and FT201XQ package options.

8.1 USB to I²C Converter

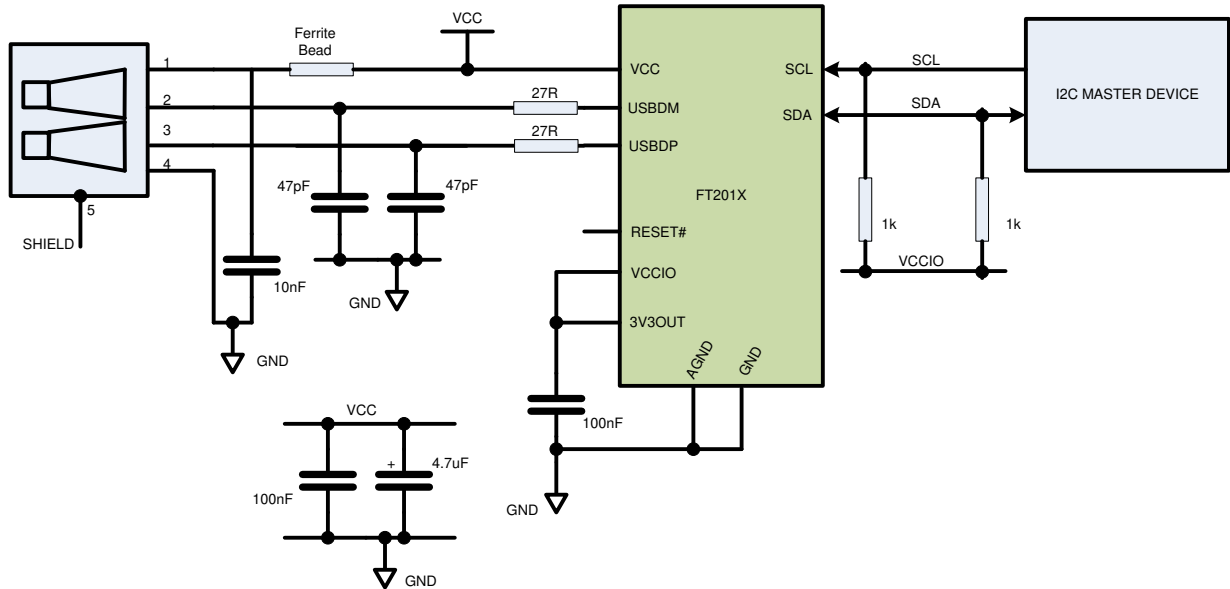


Figure 8.1 Application Example showing USB to I²C Converter

An example of using the FT201X as an I²C peripheral is shown in Figure 8.1. The FT201X is the slave on the I²C bus.

Therefore the clock supplied to the SCL pin must come from the I²C Master. The device will support standard I²C data rates such as 100 kbit/s standard mode (SM), 400 kbit/s fast mode (FM), 1 Mbit/s Fast mode plus (FM+), and 3.4 Mbit/s High Speed mode (HS).

The data line SDA is bi- directional.

The master is initially in master transmit mode by sending a start bit followed by the 7-bit address of the slave it wishes to communicate with, which is finally followed by a single bit representing whether it wishes to write(0) to or read(1) from the slave.

If the slave (FT201X) exists on the bus then it will respond with an ACK bit (active low for acknowledged) for that address. The master then continues in either transmit or receive mode (according to the read/write bit it sent), and the slave continues in its complementary mode (receive or transmit, respectively).

The address and the data bytes are sent most significant bit first. The start bit is indicated by a high-to-low transition of SDA with SCL high; the stop bit is indicated by a low-to-high transition of SDA with SCL high.

If the master wishes to write to the slave then it repeatedly sends a byte with the slave sending an ACK bit. (In this situation, the master is in master transmit mode and the slave is in slave receive mode.)

If the master wishes to read from the slave then it repeatedly receives a byte from the slave, the master sending an ACK bit after every byte but the last one. (In this situation, the master is in master receive mode and the slave is in slave transmit mode.)

The master then ends transmission with a stop bit, or it may send another START bit if it wishes to retain control of the bus for another transfer (a "combined message").

I²C defines three basic types of message, each of which begins with a START and ends with a STOP:

- Single message where a master writes data to a slave;
- Single message where a master reads data from a slave;