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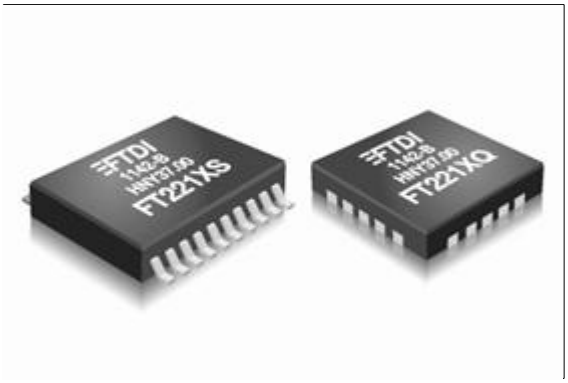
Future Technology Devices International Ltd.

FT221X

(USB 8-Bit SPI/FT1248 IC)



The FT221X is a USB to FTDI's proprietary FT1248 interface with the following advanced features:

- Single chip USB to 1, 2, 4, or 8 bit wide synchronous interface.
- Similar to an SPI Slave with variable bus width.
- Entire USB protocol handled on the chip. No USB specific firmware programming required.
- Fully integrated 2048 byte multi-time-programmable (MTP) memory, storing device descriptors and CBUS I/O configuration.
- Fully integrated clock generation with no external crystal required plus optional clock output selection enabling a glue-less interface to external MCU or FPGA.
- Data transfer rates to 1MByte/s.
- 512 byte receive buffer and 512 byte transmit buffer utilising buffer smoothing technology to allow for high data throughput.
- FTDI's royalty-free Virtual Com Port (VCP) and Direct (D2XX) drivers eliminate the requirement for USB driver development in most cases.
- Configurable CBUS I/O pin.
- USB Battery Charger Detection. Allows for USB peripheral devices to detect the presence of a higher power source to enable improved charging.
- Device supplied pre-programmed with unique USB serial number.
- USB Power Configurations; supports bus-powered, self-powered and bus-powered with power switching.
- Integrated +3.3V level converter for USB I/O.
- True 3.3V CMOS drive output and TTL input; operates down to 1V8 with external pull-ups. Tolerant of 5V inputs.
- Configurable I/O pin output drive strength; 4 mA(min) and 16 mA(max)
- Integrated power-on-reset circuit.
- Fully integrated AVCC supply filtering - no external filtering required.
- + 5V Single Supply Operation.
- Internal 3V3/1V8 LDO regulators
- Low operating and USB suspend current; 8mA (active-typ) and 125uA (suspend-typ).
- Low USB bandwidth consumption.
- UHCI/OHCI/EHCI host controller compatible.
- USB 2.0 Full Speed capable.
- Extended operating temperature range; -40 to 85ºC.
- Available in compact Pb-free 20 Pin SSOP and QFN packages (both RoHS compliant).

1 Typical Applications

- USB to SPI slave interface in 1-bit mode
- Upgrading Legacy Peripherals to USB
- Utilising USB to add system modularity
- Incorporate USB interface to enable PC transfers for development system communication
- Interfacing MCU/PLD/FPGA based designs to add USB connectivity
- USB Industrial Control
- USB MP3 Player Interface
- USB FLASH Card Reader and Writers
- Set Top Box PC - USB interface
- USB Digital Camera Interface
- Dedicated Charging Port detection for enabling higher current battery charging.

1.1 Driver Support

Royalty free VIRTUAL COM PORT (VCP) DRIVERS for...

- Windows 8 32,64-bit
- Windows 7 32,64-bit
- Windows Vista and Vista 64-bit
- Windows XP and XP 64-bit
- Server 2003, XP and Server 2008
- Windows XP Embedded
- Windows CE 4.2, 5.0 and 6.0
- Mac OS-X
- Linux 3.2 and greater
- Android

Royalty free D2XX *Direct* Drivers (USB Drivers + DLL S/W Interface)

- Windows 8 32,64-bit
- Windows 7 32,64-bit
- Windows Vista and Vista 64-bit
- Windows XP and XP 64-bit
- Server 2003, XP and Server 2008
- Windows XP Embedded
- Windows CE 4.2, 5.0 and 6.0
- Mac OS-X
- Linux 2.6 and greater
- Android

The drivers listed above are all available to download for free from FTDI website (www.ftdichip.com). Various 3rd party drivers are also available for other operating systems - see FTDI website (www.ftdichip.com) for details.

For driver installation, please refer to http://www.ftdichip.com/Documents/InstallGuides.htm

1.2 Part Numbers

Part Number	Package
FT221XQ-x	20 Pin QFN
FT221XS-x	20 Pin SSOP

Note: Packing codes for x is:

- R: Taped and Reel, (SSOP is 3,000pcs per reel, QFN is 5,000pcs per reel).

- U: Tube packing, 58pcs per tube (SSOP only)

- T: Tray packing, 490pcs per tray (QFN only)

For example: FT221XQ-R is 5,000pcs taped and reel packing

1.3 USB Compliant

The FT221X is fully compliant with the USB 2.0 specification and has been given the USB-IF Test-ID (TID) 40001462 (Rev D).

2 FT221X Block Diagram

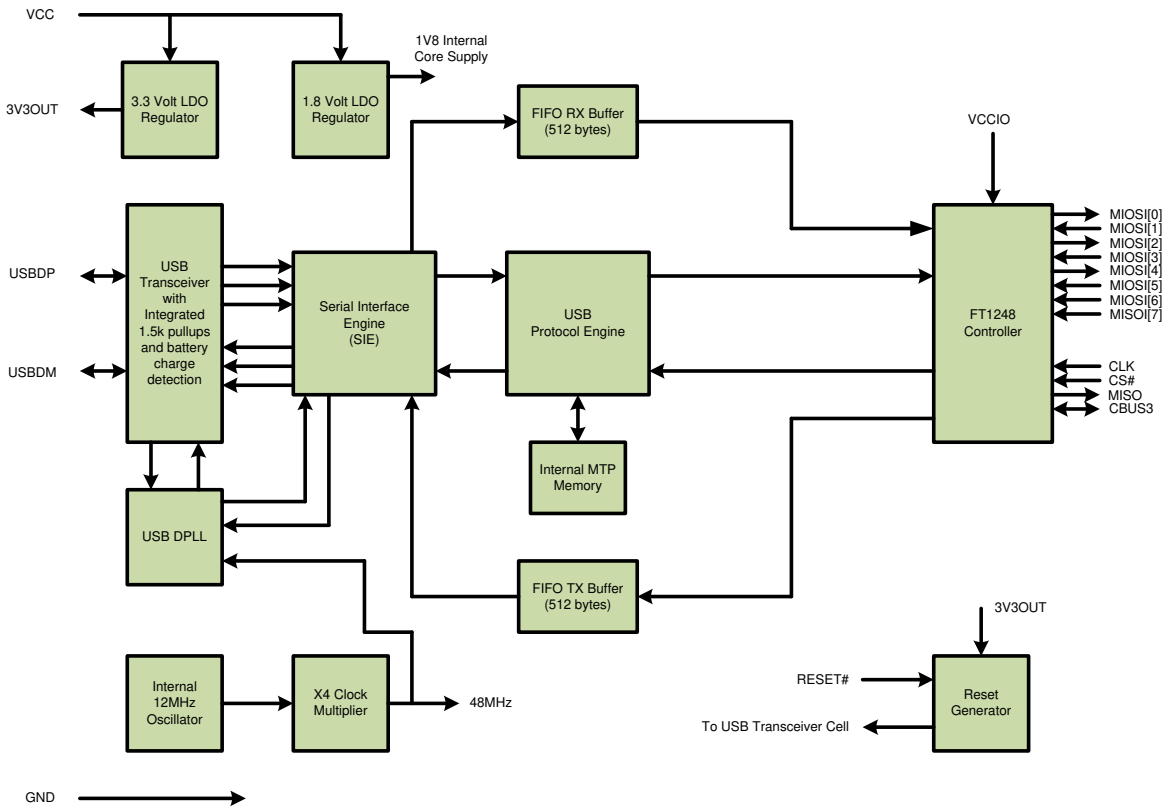


Figure 2.1 FT221X Block Diagram

For a description of each function please refer to Section 4.

Table of Contents

3 Device Pin Out and Signal Description

3.1 20-LD QFN Package

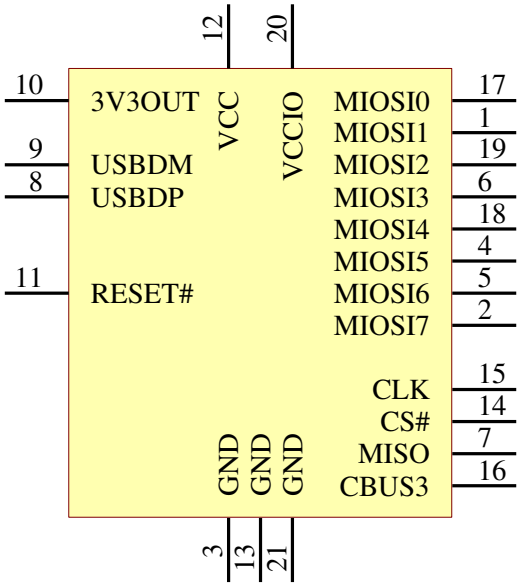


Figure 3.1 QFN Schematic Symbol

3.1.1 QFN Package PinOut Description

Note : # denotes an active low signal.

Pin No.	Name	Type	Description
12	** VCC	POWER Input	5 V (or 3V3) supply to IC
20	VCCIO	POWER Input	1V8 - 3V3 supply for the IO cells
10	** 3V3OUT	POWER Output	3V3 output at 50mA. May be used to power VCCIO. When VCC is 3V3; pin 10 is an input pin and should be connected to pin 12
3, 13	GND	POWER Input	0V Ground input.

Table 3.1 Power and Ground

*Pin 21 is the centre pad under the IC. Connect to GND.

** If VCC is 3V3 then 3V3OUT must also be driven with 3V3 input

Pin No.	Name	Type	Description
9	USBDM	INPUT	USB Data Signal Minus.
8	USBDP	INPUT	USB Data Signal Plus.
11	RESET#	INPUT	Reset input (active low).

Table 3.2 Common Function pins

Pin No.	Name	Type	Description
17	MIOSI[0]	I/O	Bi-Directional data bit 0
1	MIOSI[1]	I/O	Bi-Directional data bit 1
19	MIOSI[2]	I/O	Bi-Directional data bit 2
6	MIOSI[3]	I/O	Bi-Directional data bit 3
18	MIOSI[4]	I/O	Bi-Directional data bit 4
4	MIOSI[5]	I/O	Bi-Directional data bit 5
5	MIOSI[6]	I/O	Bi-Directional data bit 6
2	MIOSI[7]	I/O	Bi-Directional data bit 7
15	CLK	Input	Clock input from FT1248 interface master
14	CS#	Input	Chip select input to enable the device interface. Active low logic.
7	MISO	Output	Master In Serial Out. Used to provide status information to the FT1248 interface master.
16	CBUS3	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device MTP memory. See CBUS Signal Options, Table 3.7.

Table 3.3 FT1248 Interface and CBUS Group (see note 1)

Notes:
1. When used in Input Mode, the input pins are pulled to VCCIO via internal 75kΩ (approx) resistors. These pins can be programmed to gently pull low during USB suspend (PWREN# = "1") by setting an option in the MTP memory.

3.2 20-LD SSOP Package

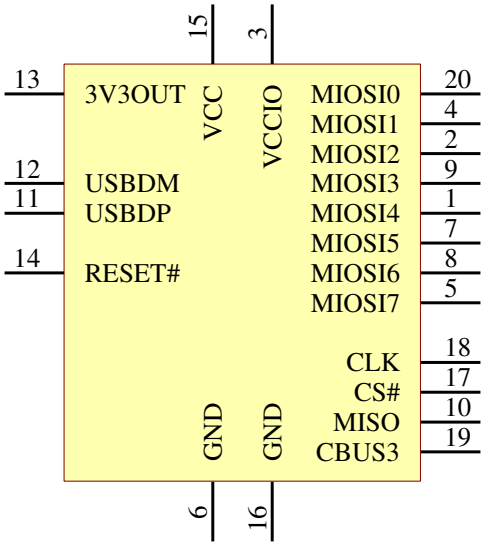


Figure 3.2 SSOP Schematic Symbol

3.2.1 SSOP Package PinOut Description

Note : # denotes an active low signal.

Pin No.	Name	Type	Description
15	** VCC	POWER Input	5 V (or 3V3) supply to IC
3	VCCIO	POWER Input	1V8 - 3V3 supply for the IO cells
13	** 3V3OUT	POWER Output	3V3 output at 50mA. May be used to power VCCIO. When VCC is 3V3; pin 13 is an input pin and should be connected to pin 15.
6, 16	GND	POWER Input	0V Ground input.

Table 3.4 Power and Ground

** If VCC is 3V3 then 3V3OUT must also be driven with 3V3 input

Pin No.	Name	Type	Description
12	USBDM	INPUT	USB Data Signal Minus.
11	USBDP	INPUT	USB Data Signal Plus.
14	RESET#	INPUT	Reset input (active low).

Table 3.5 Common Function pins

Pin No.	Name	Type	Description
20	MIOSI[0]	I/O	Bi-Directional data bit 0
4	MIOSI[1]	I/O	Bi-Directional data bit 1
2	MIOSI[2]	I/O	Bi-Directional data bit 2
9	MIOSI[3]	I/O	Bi-Directional data bit 3
1	MIOSI[4]	I/O	Bi-Directional data bit 4
7	MIOSI[5]	I/O	Bi-Directional data bit 5
8	MIOSI[6]	I/O	Bi-Directional data bit 6
5	MIOSI[7]	I/O	Bi-Directional data bit 7
18	CLK	Input	Clock input from FT1248 interface master
17	CS#	Input	Chip select input to enable the device interface. Active low logic.
10	MISO	Output	Master In Serial Out. Used to provide status information to the FT1248 interface master.
19	CBUS3	I/O	Configurable CBUS I/O Pin. Function of this pin is configured in the device MTP memory. See CBUS Signal Options, Table 3.7.

Table 3.6 FT1248 Interface and CBUS Group (see note 1)

Notes:
1. When used in Input Mode, the input pins are pulled to VCCIO via internal 75kΩ (approx) resistors. These pins can be programmed to gently pull low during USB suspend (PWREN# = "1") by setting an option in the MTP memory.

3.3 CBUS Signal Options

The following options can be configured on the CBUS I/O pin. CBUS signal options are common to both package versions of the FT221X. These options can be configured in the internal MTP memory using the software utility FT_PPROG, which can be downloaded from the FTDI Utilities (www.ftdichip.com). The default configuration is described in Section 9.

CBUS Signal Option	Available On CBUS Pin	Description
TRI-STATE	CBUS3	IO Pad is tri-stated
DRIVE 1	CBUS3	Output a constant 1
DRIVE 0	CBUS3	Output a constant 0
PWREN#	CBUS3	Output is low after the device has been configured by USB, then high during USB suspend mode. This output can be used to control power to external logic P-Channel logic level MOSFET switch. Enable the interface pull-down option when using the PWREN# in this way.
SLEEP#	CBUS3	Goes low during USB suspend mode. Typically used to power down external logic.
CLK24MHz	CBUS3	24 MHz Clock output.*
CLK12MHz	CBUS3	12 MHz Clock output.*
CLK6MHz	CBUS3	6 MHz Clock output.*
GPIO	CBUS3	CBUS bit bang mode option. Allows the CBUS pin to be used as general purpose I/O. Configured in the internal MTP memory. A separate application note, AN232R-01, available from FTDI website (www.ftdichip.com) describes in more detail how to use CBUS bit bang mode.
BCD Charger	CBUS3	Battery charge Detect, indicates when the device is connected to a dedicated battery charger host. Active high output.
BCD Charger#	CBUS3	Inverse of BCD Charger
BitBang_WR#	CBUS3	Synchronous and asynchronous bit bang mode WR# strobe output.
BitBang_RD#	CBUS3	Synchronous and asynchronous bit bang mode RD# strobe output.
VBUS Sense	CBUS3	Input to detect when VBUS is present.
Time Stamp	CBUS3	Toggle signal which changes state each time a USB SOF is received
Keep_Awake#	CBUS3	Prevents the device from entering suspend state when unplugged. May be used if programming the MTP memory over the FT1248 interface.

Table 3.7 CBUS Configuration Control

*When in USB suspend mode the outputs clocks are also suspended.

4 Function Description

The FT221X is a USB to FTDI Proprietary FT1248 interface device which simplifies USB implementations and reduces external component count by fully integrating into the device an MTP memory, and an integrated clock circuit which requires no external crystal. It has been designed to operate efficiently with USB host controllers by using as little bandwidth as possible when compared to the total USB bandwidth available.

4.1 Key Features

Functional Integration. Fully integrated MTP memory, USB termination resistors, clock generation, AVCC filtering, Power-On-Reset and LDO regulator.

Configurable CBUS I/O Pin Options. The fully integrated MTP memory allows configuration of the Control Bus (CBUS) functionality and drive strength selection. There is 1 configurable CBUS I/O pin. These configurable options are defined in section 3.3

The CBUS line can be configured with any one of these output options by setting bits in the internal MTP memory. The device is shipped with the most commonly used pin definitions pre-programmed - see Section 9 for details.

Asynchronous Bit Bang Mode with RD# and WR# Strobes. The FT221X supports FTDI's previous chip generation bit-bang mode. In bit-bang mode, the eight data lines can be switched from the regular interface mode to an 8-bit general purpose I/O port. Data packets can be sent to the device and they will be sequentially sent to the interface at a rate controlled by an internal timer (equivalent to the baud rate pre-scalar).

Synchronous Bit Bang Mode. The FT221X supports synchronous bit bang mode. This mode differs from asynchronous bit bang mode in that the interface pins are only read when the device is written to. This makes it easier for the controlling program to measure the response to an output stimulus as the data returned is synchronous to the output data. An application note, AN232R-01, available from FTDI website (www.ftdichip.com) describes this feature.

Source Power and Power Consumption. The FT221X is capable of operating at a voltage supply between +3.3V and +5.25V with a nominal operational mode current of 8mA and a nominal USB suspend mode current of 125µA. This allows greater margin for peripheral designs to meet the USB suspend mode current limit of 2.5mA. An integrated level converter within the device allows the FT221X to interface to logic running at +1.8V to +3.3V (5V tolerant).

4.2 Functional Block Descriptions

The following paragraphs detail each function within the FT221X. Please refer to the block diagram shown in Figure 2.1

Internal MTP Memory. The internal MTP memory in the FT221X is used to store USB Vendor ID (VID), Product ID (PID), device serial number, product description string and various other USB configuration descriptors. The internal MTP memory is also used to configure the CBUS pin functions. The FT221X is supplied with the internal MTP memory pre-programmed as described in Section 9. A user area of the internal MTP memory is available to system designers to allow storing additional data from the user application over USB. The internal MTP memory descriptors can be programmed in circuit, over USB without any additional voltage requirement. The descriptors can be programmed using the FTDI utility software called FT_PROG, which can be downloaded from FTDI Utilities on the FTDI website (www.ftdichip.com). In addition to programming over USB the MTP memory may be accessed via the FT1248 interface.

+1.8V LDO Regulator. The +1.8V LDO regulator generates the +1.8V reference voltage for driving the internal core of the IC.

+3.3V LDO Regulator. The +3.3V LDO regulator generates the +3.3V reference voltage for driving the USB transceiver cell output buffers. It requires an external decoupling capacitor to be attached to the 3V3OUT regulator output pin. It also provides +3.3V power to the 1.5kΩ internal pull up resistor on USBDP. The main function of the LDO is to power the USB Transceiver and the Reset Generator Cells rather than to power external logic. However, it can be used to supply external circuitry requiring a +3.3V nominal supply with a maximum current of 50mA.

USB Transceiver. The USB Transceiver Cell provides the USB 1.1 / USB 2.0 full-speed physical interface to the USB cable. The output drivers provide +3.3V level slew rate control signalling, whilst a differential input receiver and two single ended input receivers provide USB data in, Single-Ended-0 (SE0) and USB reset detection conditions respectfully. This function also incorporates a 1.5kΩ pull up resistor on USBDP. The block also detects when connected to a USB power supply which will not enumerate the device but still supply power and may be used for battery charging.

USB DPLL. The USB DPLL cell locks on to the incoming NRZI USB data and generates recovered clock and data signals for the Serial Interface Engine (SIE) block.

Internal 12MHz Oscillator - The Internal 12MHz Oscillator cell generates a 12MHz reference clock. This provides an input to the x4 Clock Multiplier function. The 12MHz Oscillator is also used as the reference clock for the SIE, USB Protocol Engine and UART FIFO controller blocks.

Clock Multiplier / Divider. The Clock Multiplier / Divider takes the 12MHz input from the Internal Oscillator function and generates the 48MHz, 24MHz, 12MHz and 6MHz reference clock signals. The 48Mz clock reference is used by the USB DPLL and the Baud Rate Generator blocks.

Serial Interface Engine (SIE). The Serial Interface Engine (SIE) block performs the parallel to serial and serial to parallel conversion of the USB data. In accordance with the USB 2.0 specification, it performs bit stuffing/un-stuffing and CRC5/CRC16 generation. It also checks the CRC on the USB data stream.

USB Protocol Engine. The USB Protocol Engine manages the data stream from the device USB control endpoint. It handles the low level USB protocol requests generated by the USB host controller and the commands for controlling the functional parameters of the UART in accordance with the USB 2.0 specification chapter 9.

FIFO RX Buffer (512 bytes). Data sent from the USB host controller to the FT1248 interface via the USB data OUT endpoint is stored in the FIFO RX (receive) buffer. Data is removed from the buffer to the FT1248 transmit register under control of the FT1248 FIFO controller. (Rx relative to the USB interface).

FIFO TX Buffer (512 bytes). Data from the FT1248 receive register is stored in the TX buffer. The USB host controller removes data from the FIFO TX Buffer by sending a USB request for data from the device data IN endpoint. (Tx relative to the USB interface).

FT1248 interface controller. Controls the FT1248 interface, dynamically switching the width of the bus as commanded by the external bus master.

RESET Generator - The integrated Reset Generator Cell provides a reliable power-on reset to the device internal circuitry at power up. The RESET# input pin allows an external device to reset the FT221X.

RESET# can be tied to VCC or left unconnected if not being used.

5 FT1248 Interface Description.

The FT1248 protocol has a dynamic bi-directional data bus interface that can be configured as 1, 2, 4, or 8-bits wide providing users with the flexibility to configure the interface with performance, pin count and PCB area in mind. For example, 1-bit mode it requires 8 clock cycles to get 8 data bits and in 8-bit mode all 8 bits are sent with one clock.

In the FT1248 there are 3 distinct phases:

While CS# is inactive, the FT1248 reflects the status of the write buffer and read buffers within the FT221X on the MIOSIO[0] and MISO wires respectively. The buffers are 512 Bytes each and the status will reflect if at least one byte of space is available for the external device to write to and whether at least one byte is available to be read by the external device.

Additionally, the FT1248 slave block supports multiple slave devices where a master can communicate with multiple SPI slave devices. When the slave is sharing buses with other SPI slave devices, the write and read buffer status cannot be reflected on the MIOSIO[0] and MISO wires during SS_n inactivity as this would cause bus contention. Therefore, it is possible for the user to select whether they wish to have the buffer status switched on or off during inactivity.

(This setting may be applied in the internal MTP memory with FT_PROG at the same time as selecting FT1248 mode).

When CS# is active a command/bus size phase occurs first. Following the command phase is the data phase, for each data byte transferred the FT1248 slave drives an ACK/NAK status onto the MISO wire. The master can send multiple data bytes so long as CS# is active, if an unsuccessful data transfer occurs, i.e. a NAK happens on the MISO wire then the master should immediately abort the transfer by de-asserting CS#.

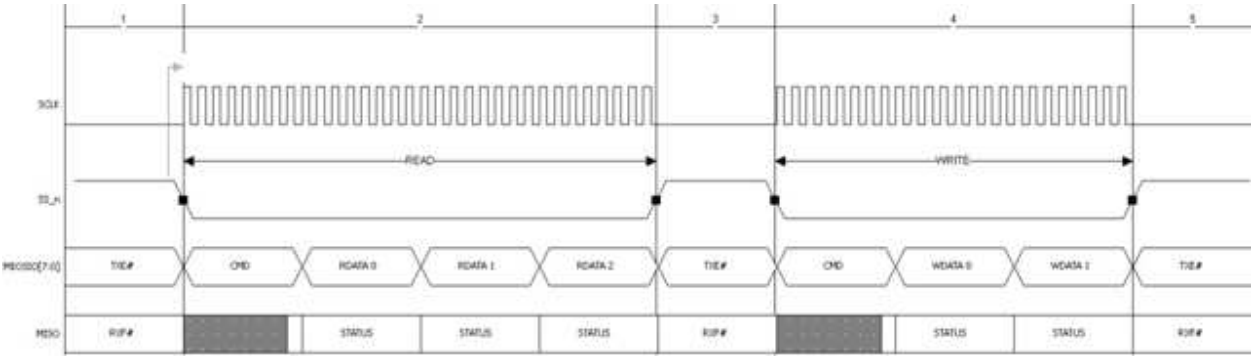


Figure 5.1: FT1248 Basic Waveform Protocol.

5.1 Determining the Dynamic Bus Width

The bus width is dynamic. In order for the FT221X, in FT1248 mode, to determine the bus width within the command phase, the bus width is encoded along with the actual commands on the first active clock edge when CS# is active and has a data width of 8-bits.

- If any of the MIOSIO[7:4] signals are driven low by the external host then the data transfer width equals 8-bits
- If any of the MIOSIO[3:2] signals are driven low by the external host then the data transfer width equals 4-bits
- If MIOSIO[1] signal is driven low by the external host then the data transfer width equals 2-bits
- Else the bus width is defaulted to 1-bit

In order to successfully decode the bus width, all MIOSIO signals must have pull up resistors. By default, all MIOSIO signals shall be seen by the FT221X in FT1248 mode as logic '1'from the internal resistors. This means that when a FT1248 master does not wish to use certain MIOSIO signals, the slave (FT221X) is still capable of determining the requested bus width since any unused MIOSIO signals shall be pulled up by default.

The remaining bits used during the command phase are used to contain the command itself which means that it is possible to define up to 16 unique commands.

	LSB							MSB
	CMD[3]	BWID 2-bit	BWID 4-bit	CMD[2]	BWID 8-bit	CMD[1]	CMD[0]	X
	0	1	2	3	4	5	6	7
1-bit Bus Width	CMD[3]	X	X	CMD[2]	X	CMD[1]	CMD[0]	X
	0	1	2	3	4	5	6	7
2-bit Bus Width	CMD[3]	0	X	CMD[2]	X	CMD[1]	CMD[0]	X
	0	1	2	3	4	5	6	7
4-bit Bus Width	CMD[3]	X	0	CMD[2]	X	CMD[1]	CMD[0]	X
	0	1	2	3	4	5	6	7
8-bit Bus Width	CMD[3]	X	X	CMD[2]	0	CMD[1]	CMD[0]	X
	0	1	2	3	4	5	6	7

Figure 5.2: FT1248 Command Structure

5.2 Supported Commands on the FT1248 Interface

The FT1248 interface can accept and decode up to 16 unique commands. At this time only 9 unique commands are implemented as shown below.

Command	Identifier	Description
write	0x00	Write request command
read	0x01	Read request command
read modem status	0x02	Read modem status command, users may wish to emulate modem status control. A RMS command returns status bits RTS and DTR
write modem status	0x03	Write modem status command, users may wish to emulate modem status control. A WMS command allows users to set status bits: DCD, RI, DSR, CTS
write buffer flush	0x04	Write buffer flush request – This command is used to indicate to the FT1248 slave that its write buffers should be flushed rather than wait for any latency timers to expire. If this command is received the FT1248 block will flag the upstream controllers (USB FIFOs etc) to flush their write buffers regardless of what content is present in the FT1248 write

		buffer
address eeprom	0x05	Address EEPROM command sets the address users wish to write or read from
write eeprom	0x06	Write EEPROM command sets the write data to be written into the EEPROM
read eeprom	0x07	Read EEPROM command reads
read usb status	0x08	Read USB Status: 00 = suspended, 01 = default, 10 = addressed, 11 = configured
Reserved	0x09 – 0xF	Unused Commands

Table 5.1: FT1248 Commands

5.3 LSB or MSB Selection

The data can be sent/received Least Significant Bit First (LSB) or Most Significant Bit First (MSB). To determine which mode is used by the FT1248 interface of the FT221X the MTP memory must be set.

This may be selected with FT_PROG.

5.4 Clock Phase/Polarity

The FT1248 slave does not need to have any knowledge of clock rate as this is supplied by the FT1248 master. However the relationship between clock and data needs to be controllable, to allow the slave to operate in the same way as the master such that data is correctly driven and sampled on the correct clock phases. By configuring the polarity and phase of CLK with respect to the data it is possible to match the FT1248 master.

There are 4 possible modes which are determined by the Clock Polarity (CPOL) and Clock Phase (CPHA) signals. The different combinations of these signals are commonly referred to as modes, see Table 5.2 below. For the FT1248 slave, only 2 of these 4 modes are supported. CPHA will always be set to 1 in the FT1248 slave because data is available or driven on to MIOSIO wires on the first clock edge after CS# is active and is therefore sampled on the trailing edge of the first clock pulse. When CPHA equals 0, it means data must be available or driven onto the MIOSIO wires on the first leading edge of the clock after CS# is active. However, during this period between CS# becoming active and the first leading clock edge is when the MIOSIO wires are being "turned around" as when CS# is inactive the FT1248 slave is driving the write buffer status. Supporting CPHA = 0 would result in bus contention and therefore, shall not be supported.

Mode	CPOL	CPHA	Supported
0	0	0	NO
1	0	1	YES
2	1	0	NO
3	1	1	YES

Table 5.2: CPOL & CPHA Mode Numbers

When CPOL is 1, the idle state of the clock is high. When CPOL is 0, the idle state of the clock is low. It should be noted that clock phase and polarity need to be identical for the master and attached slave device.

5.4.1 CPHA = 1

When CPHA is set to '1', the first edge after CS# goes low will be used to shift (or drive) the first data bit onto MIOSIO. Every odd numbered edge after this will shift out the next data bit. Incoming data will be sampled on the second or trailing SCLK edge and every even edge thereafter.

Figure 5.3 shows this for both CPOL = 0 and CPOL = 1.

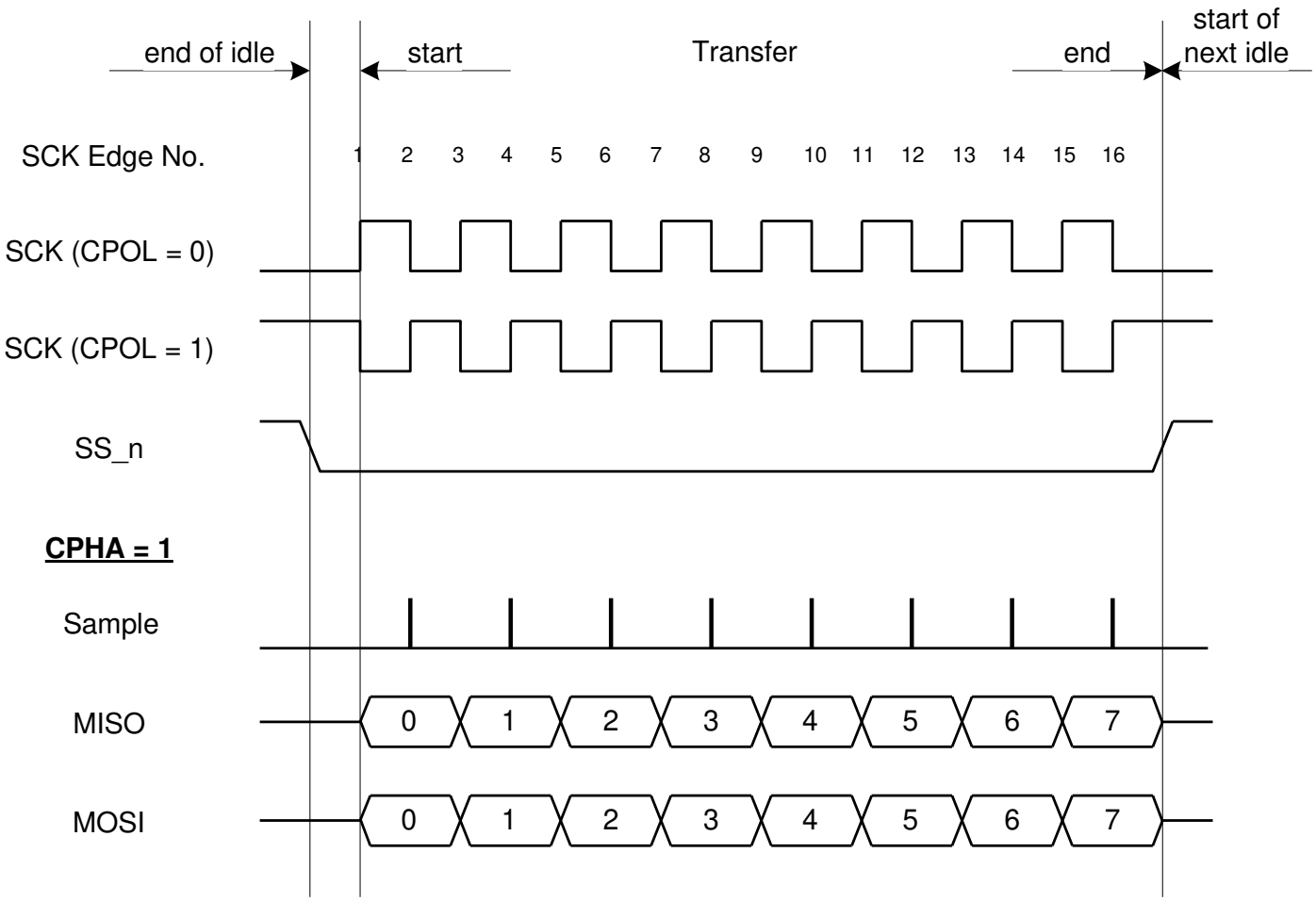


Figure 5.3: FT1248 Clock Format CPHA = 1

Note: The CPOL value may be selected in the MTP memory. This may be done with FT_PROG.

Note: Further information on this interface can be found in AN_167_FT1248 Parallel Serial Interface Basics from the FTDI website www.ftdichip.com.

5.5 FT1248 Timing

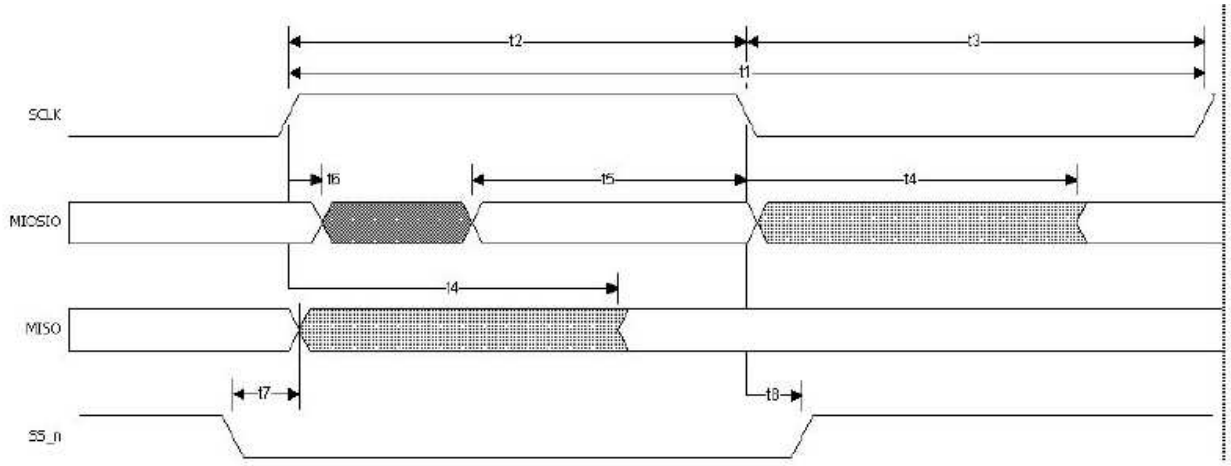


Figure 5.4: FT1248 Clock Format CPHA = 1

The timings will vary depending on VCCIO.

	Min (ns)	Typical (ns)	Max (ns)	Description
T1		83.33ns		SCLK Period
T2		41.67ns		SCLK HIGH
T3		41.67ns		SCLK LOW
T4		1	30	SCLK rising or falling driving edge to MIOSIO/MSIO
T5		25		MIOSIO setup time to rising or falling sample SCLK edge
T6		3		MIOSIO hold time from rising or falling sample SCLK edge
T7		5		SS_n setup time to rising or falling SCLK edge
T8		5		SS_n hold time from rising or falling sample SCLK edge

Table 5.3: 1V8 VCCIO timings

	Min (ns)	Typical (ns)	Max (ns)	Description
T1		83.33ns		SCLK Period
T2		41.67ns		SCLK HIGH
T3		41.67ns		SCLK LOW
T4		1	15	SCLK rising or falling driving edge to MIOSIO/MSIO

T5		22		MIOSIO setup time to rising or falling sample SCLK edge
T6		1		MIOSIO hold time from rising or falling sample SCLK edge
T7		5		SS_n setup time to rising or falling SCLK edge
T8		5		SS_n hold time from rising or falling sample SCLK edge

Table 5.4: 2V5 VCCIO timings

	Min (ns)	Typical (ns)	Max (ns)	Description
T1		83.33ns		SCLK Period
T2		41.67ns		SCLK HIGH
T3		41.67ns		SCLK LOW
T4		1	10	SCLK rising or falling driving edge to MIOSIO/MSIO
T5		20		MIOSIO setup time to rising or falling sample SCLK edge
T6		0		MIOSIO hold time from rising or falling sample SCLK edge
T7		5		SS_n setup time to rising or falling SCLK edge
T8		5		SS_n hold time from rising or falling sample SCLK edge

Table 5.5: 3V3 VCCIO timings

6 Devices Characteristics and Ratings

6.1 Absolute Maximum Ratings

The absolute maximum ratings for the FT221X devices are as follows. These are in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these may cause permanent damage to the device.

Parameter	Value	Unit	Conditions
Storage Temperature	-65°C to 150°C	Degrees C	
Floor Life (Out of Bag) At Factory Ambient (30°C / 60% Relative Humidity)	168 Hours (IPC/JEDEC J-STD-033A MSL Level 3 Compliant)*	Hours	
Ambient Operating Temperature (Power Applied)	-40°C to 85°C	Degrees C	
MTTF FT221XS	TBD	Hours	
MTTF FT221XQ	TBD	Hours	
VCC Supply Voltage	-0.3 to +5.5	V	
VCCIO IO Voltage	-0.3 to +4.0	V	
DC Input Voltage – USBDP and USBDM	-0.5 to +3.63	V	
DC Input Voltage – High Impedance Bi-directionals (powered from VCCIO)	-0.3 to +5.8	V	
DC Output Current – Outputs	22	mA	

Table 6.1 Absolute Maximum Ratings

* If devices are stored out of the packaging beyond this time limit the devices should be baked before use. The devices should be ramped up to a temperature of +125°C and baked for up to 17 hours.

6.2 ESD and Latch-up Specifications

Description	Specification
Human Body Mode (HBM)	**> ± 2kV**
Machine mode (MM)	**> ± 200V**
Charged Device Mode (CDM)	**> ± 500V**
Latch-up	**> ± 200mA**

Table 6.2 ESD and Latch-Up Specifications

6.3 DC Characteristics

DC Characteristics (Ambient Temperature = -40°C to +85°C)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
VCC	VCC Operating Supply Voltage	2.97	5	5.5	V	Normal Operation
VCC2	VCCIO Operating Supply Voltage	1.62	---	3.63	V	
Icc1	Operating Supply Current	8.1	11	13.1	mA	Normal Operation
Icc2	Operating Supply Current		125		µA	USB Suspend
3V3	3.3v regulator output	2.97	3.3	3.63	V	VCC must be greater than 3V3 otherwise 3V3OUT is an input which must be driven with 3.3V

Table 6.3 Operating Voltage and Current

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.97	VCCIO	VCCIO	V	Ioh = +/-2mA I/O Drive strength* = 4mA
		2.97	VCCIO	VCCIO	V	I/O Drive strength* = 8mA
		2.97	VCCIO	VCCIO	V	I/O Drive strength* = 12mA
		2.97	VCCIO	VCCIO	V	I/O Drive strength* = 16mA
Vol	Output Voltage Low		0	0.4	V	Iol = +/-2mA I/O Drive strength* = 4mA
			0	0.4	V	I/O Drive strength* = 8mA
			0	0.4	V	I/O Drive strength* = 12mA
			0	0.4	V	I/O Drive strength* = 16mA
Vil	Input low Switching Threshold			0.8	V	LVTTL
Vih	Input High Switching Threshold	2.0			V	LVTTL
Vt	Switching Threshold		1.49		V	LVTTL
Vt-	Schmitt trigger negative going threshold voltage		1.15		V	
Vt+	Schmitt trigger positive going threshold voltage		1.64		V	
Rpu	Input pull-up resistance	40	75	190	KΩ	Vin = 0
Rpd	Input pull-down resistance	40	75	190	KΩ	Vin =VCCIO
Iin	Input Leakage Current	-10	+/-1	10	µA	Vin = 0
Ioz	Tri-state output leakage current	-10	+/-1	10	µA	Vin = 5.5V or 0

Table 6.4 I/O Pin Characteristics VCCIO = +3.3V (except USB PHY pins)
* The I/O drive strength and slow slew-rate are configurable in the MTP memory.

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.25	VCCIO	VCCIO	V	Ioh = +/-2mA I/O Drive strength* = 4mA
		2.25	VCCIO	VCCIO	V	I/O Drive strength* = 8mA
		2.25	VCCIO	VCCIO	V	I/O Drive strength* = 12mA
		2.25	VCCIO	VCCIO	V	I/O Drive strength* = 16mA
Vol	Output Voltage Low		0	0.4	V	Iol = +/-2mA I/O Drive strength* = 4mA
			0	0.4	V	I/O Drive strength* = 8mA
			0	0.4	V	I/O Drive strength* = 12mA
			0	0.4	V	I/O Drive strength* = 16mA
Vil	Input low Switching Threshold			0.8	V	LVTTL
Vih	Input High Switching Threshold	0.8			V	LVTTL
Vt	Switching Threshold		1.1		V	LVTTL
Vt-	Schmitt trigger negative going threshold voltage		0.8		V	
Vt+	Schmitt trigger positive going threshold voltage		1.2		V	
Rpu	Input pull-up resistance	40	75	190	KΩ	Vin = 0
Rpd	Input pull-down resistance	40	75	190	KΩ	Vin =VCCIO
Iin	Input Leakage Current	-10	+/-1	10	µA	Vin = 0
Ioz	Tri-state output leakage current	-10	+/-1	10	µA	Vin = 5.5V or 0

Table 6.5 I/O Pin Characteristics VCCIO = +2.5V (except USB PHY pins)
* The I/O drive strength and slow slew-rate are configurable in the MTP memory.

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	1.62	VCCIO	VCCIO	V	Ioh = +/-2mA I/O Drive strength* = 4mA
		1.62	VCCIO	VCCIO	V	I/O Drive strength* = 8mA
		1.62	VCCIO	VCCIO	V	I/O Drive strength* = 12mA
		1.62	VCCIO	VCCIO	V	I/O Drive strength* = 16mA
Vol	Output Voltage Low		0	0.4	V	Iol = +/-2mA I/O Drive strength* = 4mA
			0	0.4	V	I/O Drive strength* = 8mA
			0	0.4	V	I/O Drive strength* = 12mA
			0	0.4	V	I/O Drive strength* = 16mA
Vil	Input low Switching Threshold			0.77	V	LVTTL
Vih	Input High Switching Threshold	1.6			V	LVTTL
Vt	Switching Threshold		0.77		V	LVTTL
Vt-	Schmitt trigger negative going threshold voltage		0.557		V	
Vt+	Schmitt trigger positive going threshold voltage		0.893		V	
Rpu	Input pull-up resistance	40	75	190	KΩ	Vin = 0
Rpd	Input pull-down resistance	40	75	190	KΩ	Vin =VCCIO
Iin	Input Leakage Current	-10	+/-1	10	µA	Vin = 0
Ioz	Tri-state output leakage current	-10	+/-1	10	µA	Vin = 5.5V or 0

Table 6.6 I/O Pin Characteristics VCCIO = +1.8V (except USB PHY pins)
* The I/O drive strength and slow slew-rate are configurable in the MTP memory.

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	VCC-0.2			V	
Vol	Output Voltage Low			0.2	V	
Vil	Input low Switching Threshold		-	0.8	V	
Vih	Input High Switching Threshold	2.0	-		V	

Table 6.7 USB I/O Pin (USBDP, USBDM) Characteristics

6.4 MTP Memory Reliability Characteristics

The internal 2048 Byte MTP memory has the following reliability characteristics:

Parameter	Value	Unit
Data Retention	10	Years
Write Cycle	2,000	Cycles
Read Cycle	Unlimited	Cycles

Table 6.8 MTP Memory Characteristics

6.5 Internal Clock Characteristics

The internal Clock Oscillator has the following characteristics:

Parameter	Value			Unit
	Minimum	Typical	Maximum	
Frequency of Operation (see Note 1)	11.98	12.00	12.02	MHz
Clock Period	83.19	83.33	83.47	ns
Duty Cycle	45	50	55	%

Table 6.9 Internal Clock Characteristics

Note 1: Equivalent to +/-1667ppm