Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

1.0 Introduction

The FT2232C is the 3rd generation of FTDI's popular USB UART / FIFO I.C. family. This device features two Multi-Purpose UART / FIFO controllers which can be configured individually in several different modes. As well as a UART interface, FIFO interface and Bit-Bang IO modes of the 2nd generation FT232BM and FT245BM devices, the FT2232C offers a variety of additional new modes of operation, including a Multi-Protocol Synchronous Serial Engine interface which is designed specifically for synchronous serial protocols such as JTAG and SPI bus.

1.1 Features Summary

HARDWARE FEATURES

- Single Chip USB ⇔ Dual Channel Serial / Parallel Ports with a variety of configurations
- Entire USB protocol handled on the chip...no USB-specific firmware programming required
- FT232BM-style UART interface option with full Handshaking & Modem interface signals
- UART Interface supports 7 / 8 bit data, 1 / 2 stop bits, and Odd / Even / Mark / Space / No Parity
- Transfer Data Rate 300 to 1 Mega Baud (RS232)
- Transfer Data Rate 300 to 3 Mega Baud (TTL and RS422 / RS485)
- Auto Transmit Enable control for RS485 serial applications using TXDEN pin
- FT245BM-style FIFO interface option with bi-directional data bus and simple 4 wire handshake interface
- Transfer Data Rate up to 1 MegaByte / Second
- Enhanced Bit-Bang Mode interface option
- New Synchronous Bit-Bang Mode interface option
- New Multi-Protocol Synchronous Serial Engine (MPSSE) interface option
- New MCU Host Bus Emulation Mode option
- New Fast Opto-Isolated Serial Interface Mode option
- Interface mode and USB Description strings configurable in external EEPROM
- EEPROM Configurable on board via USB
- Support for USB Suspend and Resume conditions via PWREN#, and SI / WU pins
- Support for bus powered, self powered, and high-power bus powered USB configurations
- Integrated Power-On-Reset circuit, with optional Reset input and Reset Output pins
- 5V and 3.3V logic IO Interfacing with independent level conversion on each channel
- Integrated 3.3V LDO Regulator for USB IO
- Integrated 6MHz – 48Mhz clock multiplier PLL
- USB Bulk or Isochronous data transfer modes
- 4.35V to 5.25V single supply operating voltage range
- UHCI / OHCI / EHCI host controller compatible
- USB 2.0 Full Speed (12 Mbits / Second) compatible
- Compact 48-LD LQFP package

VIRTUAL COM PORT (VCP) DRIVERS for

- Windows 98 / 98 SE / 2000 / ME / XP
- Linux 2.40 and greater
- Windows CE
- MAC OS-8 and OS-9**
- MAC OS-X

D2XX (USB Direct Drivers + DLL S/W Interface)

- Windows 98 / 98 SE / 2000 / ME / XP
- Linux 2.4 and Greater

APPLICATION AREAS

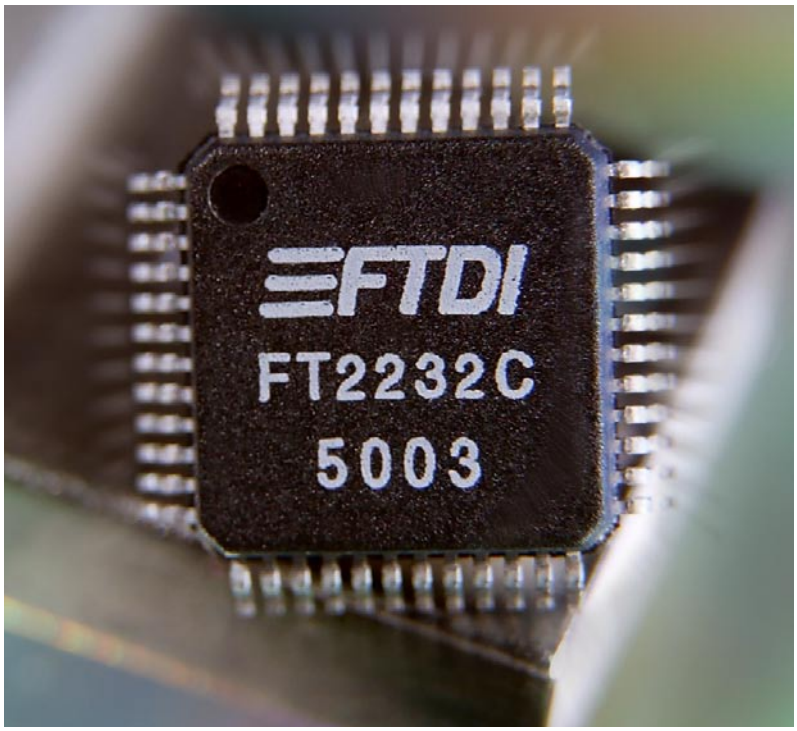
- USB ⇔Dual Port RS232 Converters
- USB ⇔ Dual Port RS422 / RS485 Converters
- Upgrading Legacy Peripheral Designs to USB
- USB Instrumentation
- USB JTAG Programming
- USB to SPI Bus Interfaces
- USB Industrial Control
- Field Upgradable USB Products
- Galvanically Isolated Products with USB Interface

[** = In planning or under development]

1.2 General Description

The FT2232C is a USB interface which incorporates the functionallity of two of FTDI's second generation BM chips into a single device. A single downstream USB port is converted to two IO channels which can each be individually configured as a FT232BM-style UART interface, or a FT245BM-style FIFO interface, without the need to add a USB hub. There are also several new special modes which are either enabled in the external EEPROM, or by using driver commands. These include Synchronous Bit-Bang Mode, a CPU-Style FIFO Interface Mode, a Multi-Protocol Synchronous Serial Engine Interface Mode, MCU Host Bus Emulation Mode, and Fast Opto-Isolated Serial Interface Mode. In addition a new high drive level option means that the device UART / FIFO IO pins will drive out at around three times the normal power level, meaning that the bus can be shared by several devices. Classic BM-style Asynchronous Bit-Bang Mode is also supported, but has been enhanced to give the user access to the device's internal RD# and WR# strobes.

FTDI provide a royalty free Virtual Com Port (V.C.P) driver that makes the peripheral ports look like a standard COM port to the PC. Most existing software applications should be able interface with the Virtual Com Port simply by reconfiguring them to use the new ports created by the driver. Using the VCP drivers an application programmer would communicate with the device in exactly the same way as they would a regular PC COM port - using the Windows VCOMM API calls or a COM port library. The FT2232C driver also incorporates the functions defined for FTDI's D2XX drivers, allowing applications programmers to interface software directly to the device using a Windows DLL. Details of the driver and the programming interface can be found on FTDI's website at **www.ftdichip.com**.



2.0 Features and Enhancements

The FT2232C incorporates all of the enhancements introduced for the second generation FT232BM and FT245BM chips. These are summarised as follows :-

- **Two Individually Configurable IO Channels**
  Each of the FT2232C's Channels (A and B) can be individually configured as a FT232BM-style UART interface, or as a FT245BM-style FIFO interface. In addition these channel can be configured in a number of special IO modes.

- **Integrated Power-On-Reset (POR) circuit**
  The device incorporates an internal POR function. A RESET# pin is available to allow external logic to reset the device where required, however for most applications this pin can simply be hardwired to Vcc. A RSTOUT# pin is provided in order to allow the new POR circuit to provide a stable reset to external MCU and other devices.

- **Integrated RCCLK circuit**
  Used to ensure that the oscillator and clock multiplier PLL frequency are stable prior to USB enumeration.

- **Integrated level converter on UART / FIFO interface and control signals**
  Each channel of the FT2232C has its own independent VCCIO pin that can be supplied by between 3V to 5V. This allows each channel's output voltage drive level to be individually configured. Thus allowing, for example 3.3V logic to be interfaced to the device without the need for external level converter I.C.'s.

- **Improved power management control for high-power USB Bus Powered devices**
  The PWREN# pin will become active when the device is enumerated by USB, and be deactivated when the device is in USB suspend. This can be used to directly drive a transistor or P-Channel MOSFET in applications where power switching of external circuitry is required. The BM pull down enable feature (configured in the external EEPROM) is also retained. This will make the device gently pull down on the FIFO / UART IO lines when the power is shut off (PWREN# is high). In this mode any residual voltage on external circuitry is bled to GND when power is removed, thus ensuring that external circuitry controlled by PWREN# resets reliably when power is restored.

- **Support for Isochronous USB Transfers**
  Whilst USB Bulk transfer is usually the best choice for data transfer, the scheduling time of the data is not guaranteed. For applications where scheduling latency takes priority over data integrity such as transferring audio and low bandwidth video data, the FT2232C offers the option of USB Isochronous transfer via configuration of bit in the EEPROM.

- **Send Immediate / Wake Up Signal Pin on each channel**
  There is a Send Immediate / Wake Up (SI/WU) signal pins on each of the chips channels. These combine two functions on one pin. If USB is in suspend mode (and remote wakeup is enabled in the EEPROM), strobing this pin low will cause the device to request a resume from suspend (WakeUp) on the USB Bus. Normally, this can be used to wake up the Host PC. During normal operation, if this pin is strobed low any data in the device RX buffer will be sent out over USB on the next Bulk-IN request from the drivers regardless of the packet size. This can be used to optimise USB transfer speed for some applications.

- **Low suspend current**
  The suspend current of the FT2232C is typically under 100 µA (excluding the 1.5K pull up resistor on USBDP) in USB suspend mode. This allows greater margin for peripherals to meet the USB Suspend current limit of 500uA.

- **Programmable Receive Buffer Timeout**
  The TX buffer timeout is programmable over USB in 1ms increments from 1ms to 255ms, thus allowing the device to be better optimised for protocols requiring faster response times from short data packets.

- **Relaxed VCC Decoupling**
  The improved level of Vcc decoupling that was incorporated into BM devices has also been implemented in the FT2232C device.

- **Baud Rate Pre-Scaler Divisors**
  The FT2232C (UART mode) baud rate pre-scaler supports division by (n+0), (n+0.125), (n+0.25), (n+0.375), (n+0.5), (n+0.625), (n+0.75) and (n+0.875) where n is an integer between 2 and 16,384 (2^{14}).

- **Extended EEPROM Support**
  The FT2232C supports 93C46 (64 x 16 bit), 93C56 (128 x 16 bit), and 93C66 (256 x 16 bit) EEPROMs. The extra space is not used by the device, however it is available for use by other external MCU / logic whilst the FT2232C is being held in reset. There is now an adiitional 64 words of space available (128 bytes total) in the user area when a 93C56 or 93C66 is used.

- **USB 2.0 (full speed option)**
  An EEPROM based option allows the FT2232C to return a USB 2.0 device descriptor as opposed to USB 1.1. Note : The device would be a USB 2.0 Full Speed device (12Mb/s) as opposed to a USB 2.0 High Speed device (480Mb/s).

In addition to the BM chip features, the FT2232C incorporates the following new features and interface modes :-

- **Enhanced Asynchronous Bit-Bang Interface**
  The FT2232C supports FTDI's BM chip Bit Bang mode. In Bit Bang mode, the eight FIFO data lines can be switched between FIFO interface mode and an 8-bit Parallel IO port. Data packets can be sent to the device and they will be sequentially sent to the interface at a rate controlled by an internal timer (equivalent to the baud rate prescaler). With the FT2232C device this mode has been enhanced so that the internal RD# and WR# strobes are now brought out of the device which can be used to allow external logic to be clocked by accesses to the Bit-Bang IO bus.

- **Synchronous Bit-Bang Interface**
  Synchronous Bit-Bang Mode differs from Asynchronous Bit-Bang mode in that the device is only read when it is written to. Thus making it easier for the controlling program to measure the response to an output stimulus as the data returned is synchronous to the output data.

- **High Output Drive Level Capabillity**
  The IO interface pins can be made to drive out at three times the standard drive level thus allowing multiple devices, or devices that require a greater drive strength to be interfaced to the FT2232C. This option is configured in the external EEPROM, ad can be set individually for each channel.

- **Multi-Protocol Synchronous Serial Engine Interface (M.P.S.S.E.)**
  The Multi-Protocol Synchronous Serial Engine (MPSSE) interface is a new option designed to interface efficiently with synchronous serial protocols such as JTAG and SPI Bus. It is very flexible in that it can be configured for different industry standards, or proprietary bus protocols. For instance, it is possible to connect one of the FT2232C's channels to an SRAM configurable FPGA as supplied by vendors such as Altera and Xilinx. The FPGA device would normally be un-configured (i.e. have no defined function) at power-up. Application software on the PC could use the MPSSE to download configuration data to the FPGA over USB. This data would define the hardware's function on power up. The other FT2232 channel would be available for other devices.
  This approach would allow a customer to create a "generic" USB peripheral, who's hardware function can be defined under control of the application software. The FPGA based hardware could be easily upgraded or totally changed simply by changing the FPGA configuration data file. (See FTDI's MORPH-IC development module for a practicle example, **www.morph-ic.com**)

- **MCU Host Bus Emulation**
  This new mode combines the 'A' and 'B' bus interface to make the FT2232C interface emulate a standard 8048 / 8051 style MCU bus. This allows peripheral devices for these MCU families to be directly attached to the FT2232C with IO being performed over USB with the help of MPSSE interface technology.

- **Fast Opto-Isolated Serial Interface**
  A new proprietary FTDI protocol is designed to allow galvanically isolated devices to communicate sychronously with the FT2232C using just 4 signal wires (over two dual opto-isolators), and two power lines. The peripheral circuitry controls the data transfer rate in both directions, whilst maintaining full data integrity. Maximum USB full speed data rates can be acheived. Both 'A' and 'B' channels can communicate over the same 4 wire interface if desired.

3.0 Simplified Block Diagram

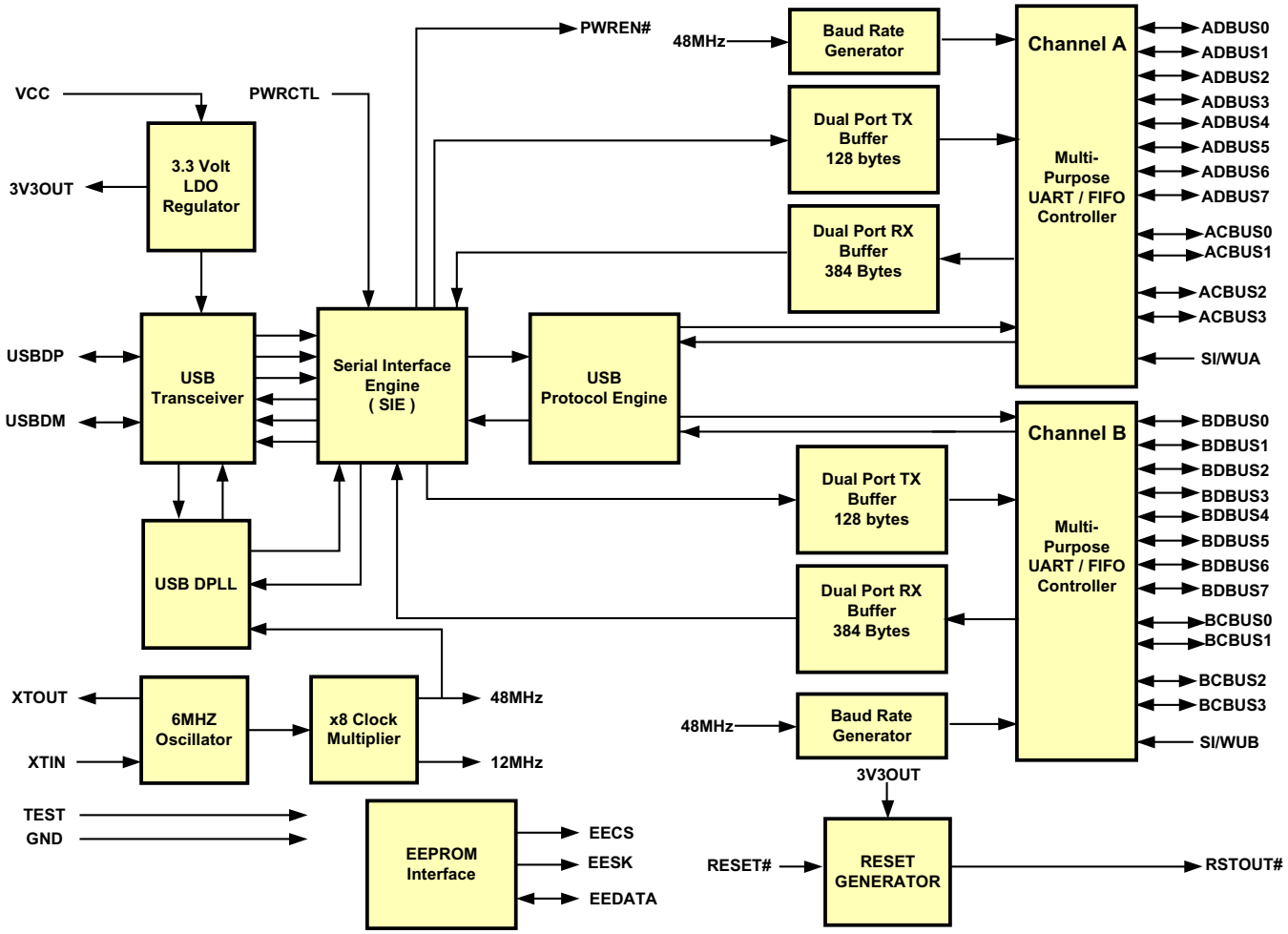


Figure 1 - FT2232C Simplified Block Diagram

3.1 Functional Block Descriptions

- **3.3V LDO Regulator**

  The 3.3V LDO Regulator generates the 3.3 volt reference voltage for driving the USB transceiver cell output buffers. It requires an external decoupling capacitor to be attached to the 3V3OUT regulator output pin. It also provides 3.3V power to the RSTOUT# pin. The main function of this block is to power the USB Transceiver and the Reset Generator Cells rather than to power external logic. However, external circuitry requiring 3.3V nominal at a current of not greater than 5mA could also draw its power from the 3V3OUT pin if required.

- **USB Transceiver**

  The USB Transceiver Cell provides the USB 1.1 / USB 2.0 full-speed physical interface to the USB cable. The output drivers provide 3.3 volt level slew rate control signalling, whilst a differential receiver and two single ended receivers provide USB data in, SEO and USB Reset condition detection.

- **USB DPLL**

  The USB DPLL cell locks on to the incoming NRZI USB data and provides separate recovered clock and data signals to the SIE block.

- **6MHz Oscillator**
  The 6MHz Oscillator cell generates a 6MHz reference clock input to the x8 Clock multiplier from an external 6MHz crystal or ceramic resonator.

- **x8 Clock Multiplier**
  The x8 Clock Multiplier takes the 6MHz input from the Oscillator cell and generates a 48MHz reference clock for the USB DPPL and the Baud Rate Generator blocks.

- **Serial Interface Engine (SIE)**
  The Serial Interface Engine (SIE) block performs the Parallel to Serial and Serial to Parallel conversion of the USB data. In accordance to the USB 2.0 specification, it performs bit stuffing / un-stuffing and CRC5 / CRC16 generation / checking on the USB data stream.

- **USB Protocol Engine**
  The USB Protocol Engine manages the data stream from the device USB control endpoint. It handles the low level USB protocol (Chapter 9) requests generated by the USB host controller and the commands for controlling the functional parameters of the UART / FIFO controller blocks.

- **Dual Port TX Buffers (128 bytes)**
  Data from the USB data out endpoint is stored in the Dual Port TX buffer and removed from the buffer to the transmit register under control of the UART FIFO controller.

- **Dual Port RX Buffers (384 bytes)**
  Data from the UART / FIFO controller receive register is stored in the Dual Port RX buffer prior to being removed by the SIE on a USB request for data from the device data in endpoint.

- **Multi-Purpose UART / FIFO Controllers**
  The Multi-purpose UART / FIFO controllers handle the transfer of data between the Dual Port RX and TX buffers and the UART / FIFO transmit and receive registers. When configured as a UART it performs asynchronous 7 / 8 bit Parallel to Serial and Serial to Parallel conversion of the data on the RS232 (RS422 and RS485) interface. Control signals supported by UART mode include RTS, CTS, DSR , DTR, DCD and RI. There are also transmitter enable control signal pins (TXDEN) provided to assist with interfacing to RS485 transceivers. RTS/CTS, DSR/DTR and Xon/Xoff handshaking options are also supported. Handshaking, where required, is handled in hardware to ensure fast response times. The UART's also supports the RS232 BREAK setting and detection conditions.

- **Baud Rate Generator**
  The Baud Rate Generator provides a x16 clock input to the UART's from the 48MHz reference clock and consists of a 14 bit prescaler and 3 register bits which provide fine tuning of the baud rate (used to divide by a number plus a fraction). This determines the Baud Rate of the UART which is programmable from 183 baud to 3 million baud.

- **RESET Generator**
  The Reset Generator Cell provides a reliable power-on reset to the device internal circuitry on power up. An additional RESET# input and RSTOUT# output are provided to allow other devices to reset the FT2232C, or the FT2232C to reset other devices respectively. During reset, RSTOUT# is driven low, otherwise it drives out at the 3.3V provided by the onboard regulator. RSTOUT# can be used to control the 1.5K pull-up on USBDP directly where delayed USB enumeration is required. It can also be used to reset other devices. RSTOUT# will stay high-impedance for approximately 5ms after VCC has risen above 3.5V AND the device oscillator is running AND RESET# is high. RESET# should be tied to VCC unless it is a requirement to reset the device from external logic or an external reset generator I.C.

- **EEPROM Interface**

  When used without an external EEPROM the FT2232C be configured as a USB to dual serial port device. Adding an external 93C46 (93C56 or 93C66) EEPROM allows each of the chip's channels to be independently configured as a serial UART (232 mode), or a parallel FIFO (245 mode). The external EEPROM is used to enable the Fast Opto-Isolated Serial interface mode. The external EEPROM can also be used to customise the USB VID, PID, Serial Number, Product Description Strings and Power Descriptor value of the FT2232C for OEM applications. Other parameters controlled by the EEPROM include Remote Wake Up, Isochronous Transfer Mode, Soft Pull Down on Power-Off and USB 2.0 descriptor modes.

  The EEPROM should be a 16 bit wide configuration such as a MicroChip 93LC46B or equivalent capable of a 1Mb/s clock rate at VCC = 4.35V to 5.25V. The EEPROM is programmable-on board over USB using a utility program available from FTDI's web site (**www.ftdichip.com**). This allows a blank part to be soldered onto the PCB and programmed as part of the manufacturing and test process.

  If no EEPROM is connected (or the EEPROM is blank), the FT2232C will default to dual serial ports. The device use its built-in default VID, PID Product Description and Power Descriptor Value. In this case, the device will not have a serial number as part of the USB descriptor.

4.0 Device Pin-Out

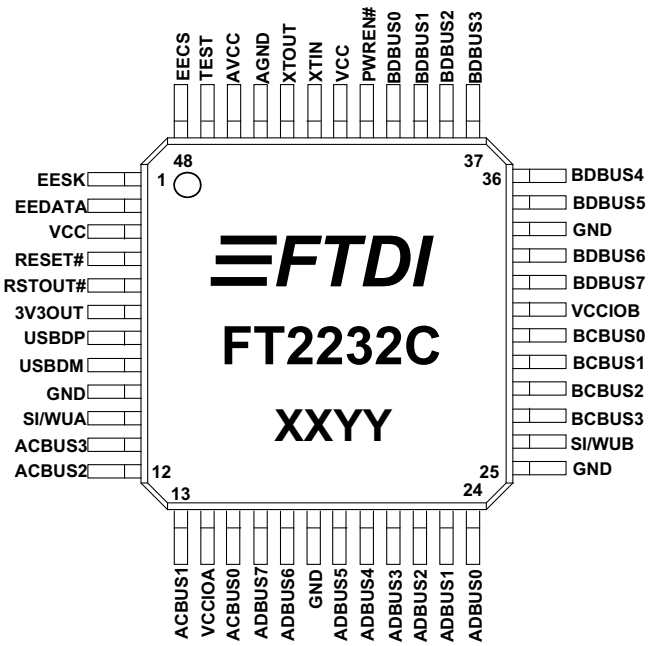


Figure 2
Pin-Out
(LQFP-48 Package)

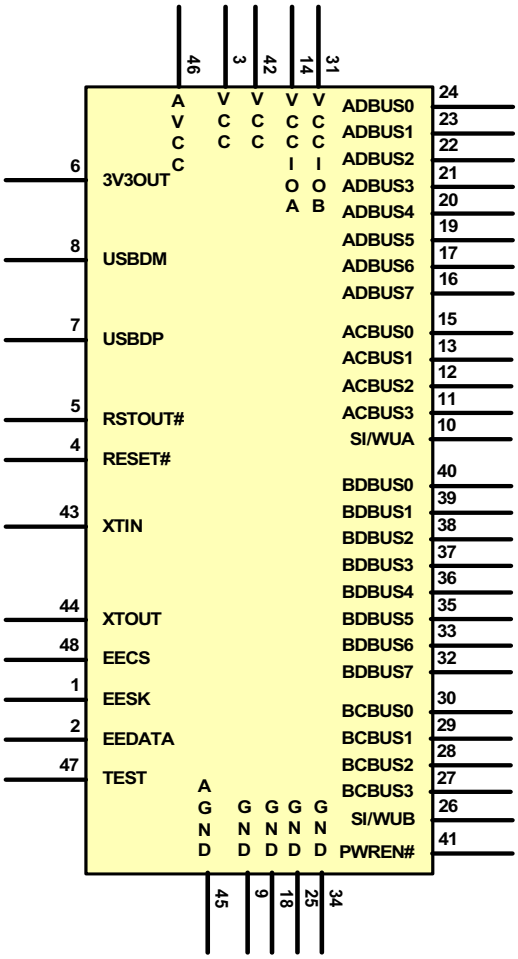


Figure 3
Pin-Out
(Schematic Symbol)

5.0 Pin Definitions

This section decribes the operation of the FT2232C pins. Common pins are defined in the first section, then the I/O pins are defined, by chip mode. More detailed descriptions of the operation of the I/O pins are provided in section 9.

5.1 Common Pins

The operation of the following FT2232C pins stay the same, regardless of the chip mode :-

USB INTERFACE GROUP

Pin#	Signal	Type	Description
7	USBDP	I/O	USB Data Signal Plus (Requires 1.5K pull-up to 3V3OUT or RSTOUT#)
8	USBDM	I/O	USB Data Signal Minus

EEPROM INTERFACE GROUP

Pin#	Signal	Type	Description
48	EECS	I/O	EEPROM – Chip Select. Tri-State during device reset. **Note 1
1	EESK	OUTPUT	Clock signal to EEPROM. Tri-State during device reset, else drives out. **Note 1
2	EEDATA	I/O	EEPROM – Data I/O Connect directly to Data-In of the EEPROM and to Data-Out of the EEPROM via a 2.2K resistor. Also, pull Data-Out of the EEPROM to VCC via a 10K resistor for correct operation. Tri-State during device reset. **Note 1

MISCELLANEOUS SIGNAL GROUP

Pin#	Signal	Type	Description
4	RESET#	INPUT	Can be used by an external device to reset the FT2232C. If not required, tie to VCC. **Note 1
5	RSTOUT#	OUTPUT	Output of the internal Reset Generator. Drives low for 5.6 ms after VCC > 3.5V and the internal clock starts up, then clamps it's output to the 3.3V output of the internal regulator. Taking RESET# low will also force RSTOUT# to drive low. RSTOUT# is NOT affected by a USB Bus Reset.
47	TEST	INPUT	Puts device into I.C. test mode – must be tied to GND for normal operation.
41	PWREN#	OUTPUT	Goes Low after the device is configured via USB, then high during USB suspend. Can be used to control power to external logic using a P-Channel Logic Level MOSFET switch. Enable the Interface Pull-Down Option in EEPROM when using the PWREN# pin in this way.
43	XTIN	INPUT	Input to 6MHz Crystal Oscillator Cell. This pin can also be driven by an external 6MHz clock if required. Note : Switching threshold of this pin is VCC/2, so if driving from an external source, the source must be driving at 5V CMOS level or a.c. coupled to centre around VCC/2.
44	XTOUT	OUTPUT	Output from 6MHz Crystal Oscillator Cell. XTOUT stops oscillating during USB suspend, so take care if using this signal to clock external logic.

**Note 1 - *During device reset, these pins are tri-state but pulled up to VCC via internal 200K resistors.*

POWER AND GND GROUP

Pin#	Signal	Type	Description
6	3V3OUT	OUTPUT	3.3 volt Output from the integrated L.D.O. regulator This pin should be decoupled to GND using a 33nF ceramic capacitor in close proximity to the device pin. It's prime purpose is to provide the internal 3.3V supply to the USB transceiver cell and the RSTOUT# pin. A small amount of current (<= 5mA) can be drawn from this pin to power external 3.3V logic if required.
3, 42	VCC	PWR	+4.35 volt to +5.25 volt VCC to the device core, LDO and non-UART / FIFO controller interface pins.
14	VCCIOA	PWR	+3.0 volt to +5.25 volt VCC to the UART / FIFO A Channel interface pins 10..13, 15..17 and 19..24. When interfacing with 3.3V external logic in a bus powered design connect VCCIO to a 3.3V supply generated from the USB bus. When interfacing with 3.3V external logic in a self powered design connect VCCIO to the 3.3V supply of the external logic. Otherwise connect to VCC to drive out at 5V CMOS level.
31	VCCIOB	PWR	+3.0 volt to +5.25 volt VCC to the UART / FIFO B Channel interface pins 26..30, 32..33 and 35..40. When interfacing with 3.3V external logic in a bus powered design connect VCCIO to a 3.3V supply generated from the USB bus. When interfacing with 3.3V external logic in a self powered design connect VCCIO to the 3.3V supply of the external logic. Otherwise connect to VCC to drive out at 5V CMOS level.
9,18, 25, 34	GND	PWR	Device - Ground Supply Pins
46	AVCC	PWR	Device - Analog Power Supply for the internal x8 clock multiplier. A low pass filter consisting of a 470 Ohm series resistor and a 100 nF to GND should be used on the supply to this pin.
45	AGND	PWR	Device - Analog Ground Supply for the internal x8 clock multiplier

5.2 IO Pin Definitions by Chip Mode

The FT2232C will default to dual serial mode (232 UART mode on both channel A and B, if no external EEPROM is used, or the external EEPROM is blank. The definition of the following pins vary according to the chip's mode :-

Channel A

Pin#	*Generic Pin Name*	*Pin Definitions by Chip Mode* **Note 2					
		232 UART Mode	*245 FIFO Mode*	*Enhanced Asynchronous and Synchronous Bit-Bang Modes*	*MPSSE* **Note 4	*MCU Host Bus Emulation Mode* **Note 5	*Fast Opto-Isolated Serial Mode*
24	ADBUS0	TXD	D0	D0	TCK/SK	AD0	**Note 3
23	ADBUS1	RXD	D1	D1	TDI/D0	AD1	
22	ADBUS2	RTS#	D2	D2	TDO/DI	AD2	
21	ADBUS3	CTS#	D3	D3	TMS/CS	AD3	
20	ADBUS4	DTR#	D4	D4	GPIOL0	AD4	
19	ADBUS5	DSR#	D5	D5	GPIOL1	AD5	
17	ADBUS6	DCD#	D6	D6	GPIOL2	AD6	
16	ADBUS7	RI#	D7	D7	GPIOL3	AD7	
15	ACBUS0	TXDEN	RXF#	WR# **Note 6	GPIOH0	I/O0	
13	ACBUS1	SLEEP#	TXE#	RD# **Note 6	GPIOH1	I/O1	
12	ACBUS2	RXLED#	RD#	WR# **Note 7	GPIOH2	IORDY	
11	ACBUS3	TXLED#	WR	RD# **Note 7	GPIOH3	OSC	
10	SI/WUA	SI/WUA	SI/WUA	SI/WUA	**Note 8	**Note 8	

***Note 2 :** 232 UART, 245 FIFO, CPU FIFO Interface, and Fast Opto-Isolated modes are enabled in the external EEPROM. Enhanced Asynchronous and Synchronous Bit-Bang modes, MPSSE, and MCU Host Bus Emulation modes are enabled using the driver command set bit mode. See Section 5.2 for details.*

***Note 3 :** Channel A can be configured in another IO mode if channel B is in Fast Opto-Isolated Serial Mode. If both Channel A and Channel B are in Fast Opto-Isolated Serial Mode all of the IO will be on Channel B.*

***Note 4 :** MPSSE is Channel A only.*

***Note 5 :** MCU Host Bus Emulation requires both Channels.*

***Note 6 :** The Bit-Bang Mode (synchronous and asynchronous) WR# and RD# strobes are on these pins when the main Channel mode is 245 FIFO, CPU FIFO interface, or Fast Opto-Isolated Serial Modes.*

***Note 7 :** The Bit-Bang Mode (synchronous and asynchronous) WR# and RD# strobes are on these pins when the main Channel mode is 232 UART Mode.*

***Note 8 :** SI/WU is not available in these modes.*

Channel B

Pin#	Generic Pin Name	Pin Definitions by Chip Mode **Note 2					
		232 UART Mode	245 FIFO Mode	Enhanced Asynchronous and Synchronous Bit-Bang Modes	MPSSE **Note 4	MCU Host Bus Emulation Mode **Note 5	Fast Opto-Isolated Serial Mode
40	BDBUS0	TXD	D0	D0		A8	FSDI
39	BDBUS1	RXD	D1	D1		A9	FSCLK
38	BDBUS2	RTS#	D2	D2		A10	FSDO
37	BDBUS3	CTS#	D3	D3		A11	FSCTS
36	BDBUS4	DTR#	D4	D4		A12	**Note 3
35	BDBUS5	DSR#	D5	D5		A13	
33	BDBUS6	DCD#	D6	D6		A14	
32	BDBUS7	RI#	D7	D7		A15	
30	BCBUS0	TXDEN	RXF#	WR# **Note 9		CS#	
29	BCBUS1	SLEEP#	TXE#	RD# **Note 9		ALE	
28	BCBUS2	RXLED#	RD#	WR# **Note 7		RD#	
27	BCBUS3	TXLED#	WR	RD# **Note 7		WR#	
26	SI/WUB	SI/WUB	SI/WUB	SI/WUB	**Note 8	**Note 8	SI/WUB

***Note 2 :** 232 UART, 245 FIFO, CPU FIFO Interface, and Fast Opto-Isolated modes are enabled in the external EEPROM. Enhanced Asynchronous and Synchronous Bit-Bang modes, MPSSE, and MCU Host Bus Emulation modes are enabled using the driver command set bit mode. See Section 5.2 for details.*

***Note 3 :** Channel A can be configured in another IO mode if channel B is in Fast Opto-Isolated Serial Mode. If both Channel A and Channel B are in Fast Opto-Isolated Serial Mode all of the IO will be on Channel B.*

***Note 4 :** MPSSE is Channel A only.*

***Note 5 :** MCU Host Bus Emulation requires both Channels.*

***Note 6 :** The Bit-Bang Mode (synchronous and asynchronous) WR# and RD# strobes are on these pins when the main Channel mode is 245 FIFO, CPU FIFO interface, or Fast Opto-Isolated Serial Modes.*

***Note 7 :** The Bit-Bang Mode (synchronous and asynchronous) WR# and RD# strobes are on these pins when the main Channel mode is 232 UART Mode.*

***Note 8 :** SI/WU is not available in these modes.*

***Note 9 :** The Bit-Bang Mode (synchronous and asynchronous) WR# and RD# strobes are on these pins when the main Channel mode is 245 FIFO, CPU FIFO interface. Bit-Bang mode is not available on Channel B when Fast Opto-Isolated Serial Mode is enabled.*

5.3 IO Mode Command Hex Values

Enhanced Asynchronous and Synchronous Bit-Bang modes, MPSSE, and MCU Host Bus Emulation modes are enabled using the D2XX driver command FT_SetBitMode. The hex values used with this command to enable these modes are as follows-

Mode	*Value (hex)*
Reset the IO bit Mode	0
Asynchronous Bit Bang Mode	1
MPSSE	2
Synchronous Bit bang Mode	4
MCU Host bus Emulation	8
Fast Opto-Isolated Serial Mode	10

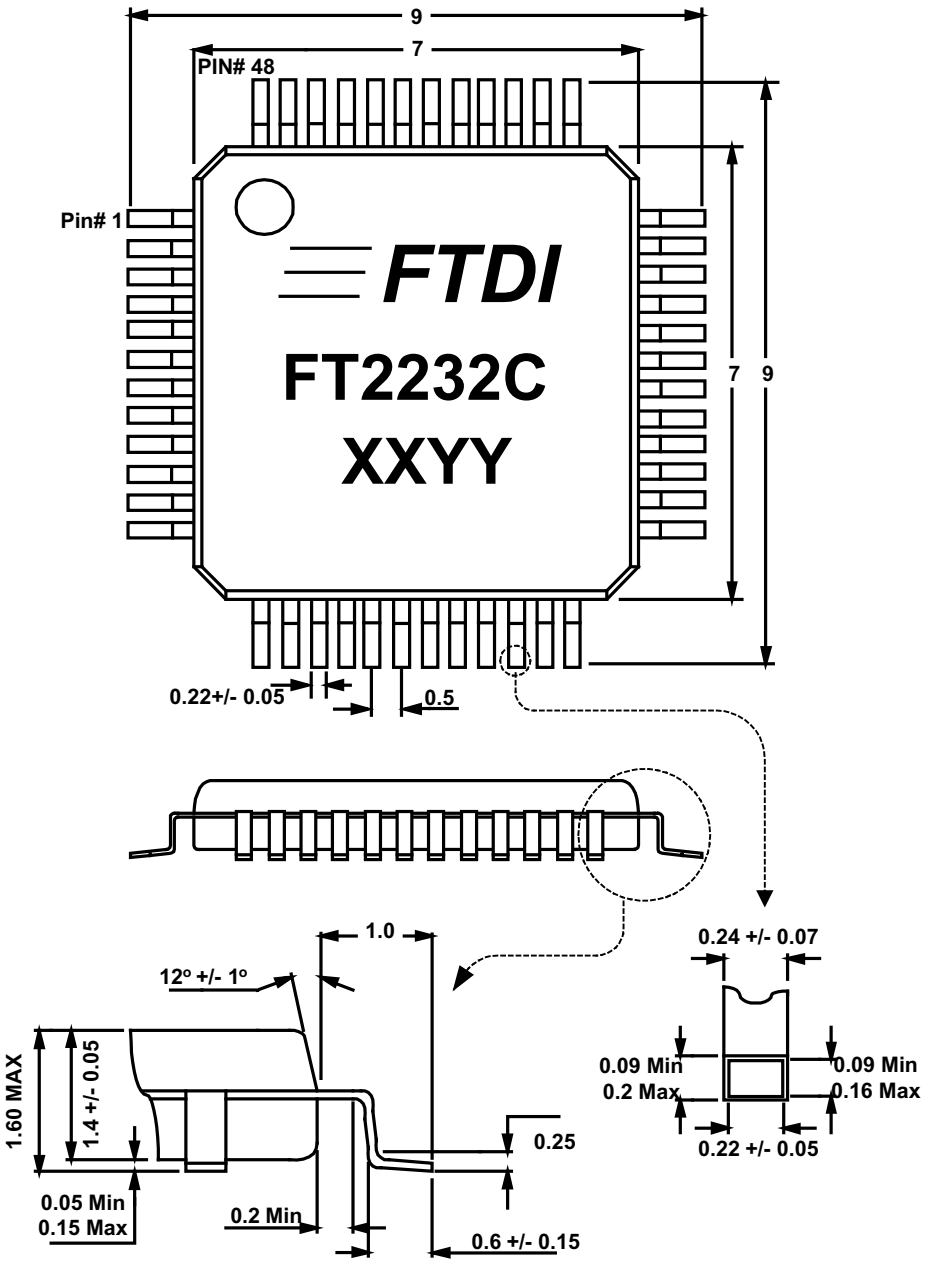
See application note **AN2232C-02 "Bit Mode Functions for the FT2232C"** for more details and examples.

Note that all other device modes can be enabled in the external EEPROM, and do not require these values to be configured.

In the case of Fast Opto-Isolated Serial mode sending a value of 10 will hold this device mode in reset, and sending a value of 0 will release this mode from reset.

6.0 Package Outline

Figure 4 - 48 LD LQFP Package Dimensions



The FT2232C is supplied in a 48 LD LQFP package as standard. This package has a 7mm x 7mm body (9mm x 9mm including leads) with leads on a 0.5mm pitch.

The above drawing shows the LQFP-48 package – all dimensions are in millimetres.

A Lead free version of this package is also available, part number FT2232L.

XXYY = Date Code (XX = 2 digit week number, YY = 1 or 2 digit year number.

7.0 Absolute Maximum Ratings

These are the absolute maximum ratings for the FT2232C device in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these may cause permanent damage to the device.

- Storage Temperature ..... –65°C to + 150°C
- Floor Life (Out of Bag) at Factory Ambient (30°C/60% Relative Humidity).....192 Hours **Note 10 (Level 3 Compliant)
- Ambient Temperature (Power Applied)..... 0°C to + 70°C
- VCC Supply Voltage ..... -0.5V to +6.00V
- DC Input Voltage - Inputs ..... -0.5V to VCC + 0.5V
- DC Input Voltage - High Impedance Bidirectionals ..... -0.5V to VCC + 0.5V
- DC Output Current – Outputs 24mA
- DC Output Current – Low Impedance Bidirectionals 24mA
- Power Dissipation (VCC = 5.25V) 500mW
- Electrostatic Discharge Voltage (Human Body Model) (I < 1µA) ..... +/- 3000V
- Latch Up Current (Vi = +/- 10V maximum, for 10 ms) ..... +/-200mA

**Note 10 – *If devices are stored out of the packaging beyond this time limit the devices should be baked before use. The devices should be ramped up to a temperature of 110°C and baked for 8 to 10 hours.*

7.1 D.C. Characteristics

DC Characteristics (Ambient Temperature = 0 to 70°C)

Operating Voltage and Current

Parameter	Description	Min	Typ	Max	Units	Conditions
Vcc1	VCC Operating Supply Voltage	4.35	5.0	5.25	V	
Vcc2	VCCIO Operating Supply Voltage	3.0	-	5.25	V	
Icc1	Operating Supply Current	-	30	-	mA	Normal Operation
Icc2	Operating Supply Current	-	100	200	µA	USB Suspend **Note 11

***Note 11** – *Supply current excludes the 200µA nominal drawn by the external pull-up resistor on USBDP.*

IO Pin Characteristics (VCCIO = 5.0V, Standard Drive Level) **Note 12

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	3.2	4.1	4.9	V	I source = 2mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 2mA
Vin	Input Switching Threshold	1.3	1.6	1.9	V	
VHys	Input Switching Hysteresis	50	55	60	mV	

IO Pin Characteristics (VCCIO = 3.0 - 3.6V, Standard Drive Level) **Note 12

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	2.2	2.7	3.2	V	I source = 1 mA
Vol	Output Voltage Low	0.3	0.4	0.5	V	I sink = 2 mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	
VHys	Input Switching Hysteresis	20	25	30	mV	

IO Pin Characteristics (VCCIO = 5.0V, High Drive Level) **Note 12, **Note 13

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	3.2	4.1	4.9	V	I source = 6 mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 6 mA
Vin	Input Switching Threshold	1.3	1.6	1.9	V	
VHys	Input Switching Hysteresis	50	55	60	mV	

IO Pin Characteristics (VCCIO = 3.0 - 3.6V, High Drive Level) **Note 12, **Note 13

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	2.2	2.8	3.2	V	I source = 3mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 8 mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	
VHys	Input Switching Hysteresis	20	25	30	mV	

***Note 12 :** *Inputs have an internal 200K pull-up resistor to VCCIO, which can alternativly be programmed to pull down using a configuration bit in the external EEPROM.*

***Note 12 :** *The high output drive level is configured in the external EEPROM. Each channel can be configured individually.*

XTIN / XTOUT Pin Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	4.0	-	5.0	V	Fosc = 6MHz
Vol	Output Voltage Low	0.1	-	1.0	V	Fosc = 6MHz
Vin	Input Switching Threshold	1.8	2.5	3.2	V	

RESET#, TEST, EECS, EESK, EEDATA Pin Characteristics **Note 14

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	3.2	4.1	4.9	V	I source = 2mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 2 mA
Vin	Input Switching Threshold	1.3	1.6	1.9	V	
VHys	Input Switching Hysteresis	50	55	60	mV	

***Note 14** – *EECS, EESK, EEDATA and RESET# pins have an internal 200K pull-up resistor to VCC*

RSTOUT# Pin Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	3.0	-	3.6	V	I source = 2mA
Vol	Output Voltage Low	0.3	-	0.6	V	I sink = 2mA

USB IO Pin Characteristics **Note 15

Parameter	Description	Min	Typ	Max	Units	Conditions
UVoh	IO Pins Static Output (High)	2.8	-	3.6	V	RI = 1.5K to 3V3Out (D+) RI = 15K to GND (D-)
UVol	IO Pins Static Output (Low)	0	-	0.3	V	RI = 1.5K to 3V3Out (D+) RI = 15K to GND (D-)
UVse	Single Ended Rx Threshold	0.8	-	2.0	V	
UCom	Differential Common Mode	0.8	-	2.5	V	
UVDif	Differential Input Sensitivity	0.2	-	-	V	
UDrvZ	Driver Output Impedance	29	-	44	Ohm	

***Note 15** – *Driver Output Impedance includes the external 27R series resistors on USBDP and USBDM pins.*

8.0 Standard Device Configuration Examples

8.1 Oscillator Configurations

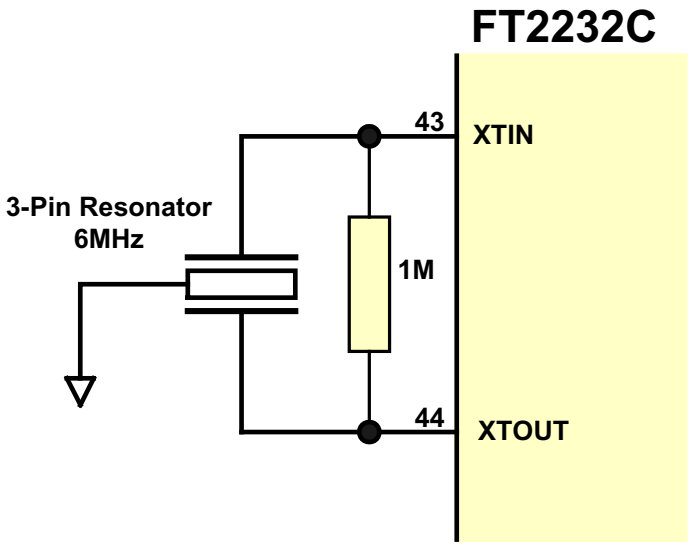


Figure 5
3-Pin Ceramic Resonator Configuration

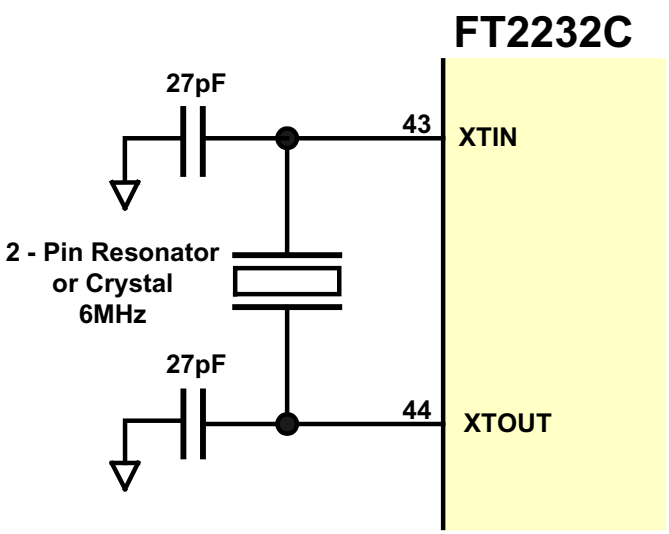


Figure 6
Crystal or 2-Pin Ceramic Resonator Configuration

Figure 5 illustrates how to use the FT2232C with a 3-Pin Ceramic Resonator. A suitable part would be a ceramic resonator from Murata's CERALOCK range. (Murata Part Number CSTCR6M00G15), or equivalent. 3-Pin ceramic resonators have the load capacitors built into the resonator so no external loading capacitors are required. This makes for an economical configuration. The accuracy of this Murata ceramic resonator is +/- 0.25% and it is specifically designed for USB full speed applications. A 1 MegaOhm loading resistor across XTIN and XTOUT is recommended in order to guarantee this level of accuracy.

Other ceramic resonators with a lesser degree of accuracy (typically +/- 0.5%) are technically out-with the USB specification, but it has been calculated that using such a device will work satisfactorily in practice with a FT2232C design. An example of such a device is Murata's CSTLSM00G53.

Figure 6 illustrates how to use the FT2232C with a 6MHz Crystal or 2-Pin Ceramic Resonator. In this case, these devices do not have in-built loading capacitors so these have to be added between XTIN, XTOUT and GND as shown. A value of 27pF is shown as the capacitor in the example – this will be good for many crystals and some resonators but do select the value based on the manufacturers recommendations wherever possible. If using a crystal, use a parallel cut type. If using a resonator, see the previous note on frequency accuracy.

It is also possible to use a 6 MHz Oscillator with the FT2232C. In this case the output of the oscillator would be connected to XTIN, and XTOUT should be left unconnected. The oscillator must have a CMOS output.

8.2 EEPROM Configuration

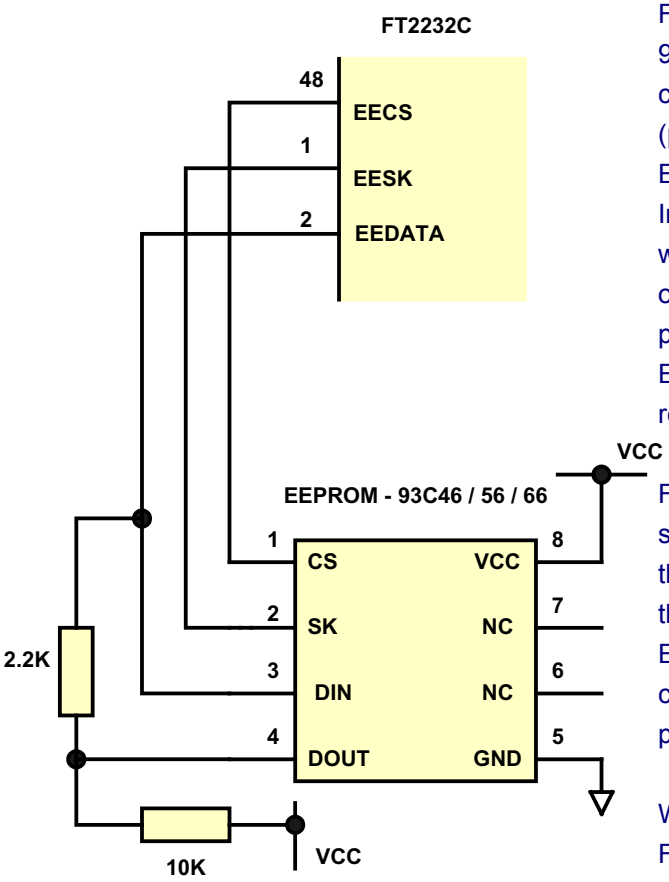


Figure 7
EEPROM Configuration

Figure 7 illustrates how to connect the FT2232C to the 93C46 (93C56 or 93C66) EEPROM. EECS (pin 48) is directly connected to the chip select (CS) pin of the EEPROM. EESK (pin 1) is directly connected to the clock (SK) pin of the EEPROM. EEDATA (pin 2) is directly connected to the Data In (Din) pin of the EEPROM. There is a potential condition whereby both the Data Output (Dout) of the EEPROM can drive out at the same time as the EEDATA pin of the FT2232C. To prevent potential data clash in this situation, the Dout of the EEPROM is connected to EEDATA of the FT2232C via a 2.2K resistor.

Following a power-on reset or a USB reset, the FT2232C will scan the EEPROM to find out (a) if an EEPROM is attached to the Device and (b) if the data in the device is valid. If both of these are the case, then the FT2232C will use the data in the EEPROM, otherwise it will use its built-in default values and configuration. The default port configuration of the FT2232C puts both Channel A and Channel B into serial UART mode.

When a valid command is issued to the EEPROM from the FT2232C, the EEPROM will acknowledge the command by pulling its Dout pin low. In order to check for this condition, it is necessary to pull Dout high using a 10K resistor. If the command acknowledge doesn't happen then EEDATA will be pulled high by the 10K resistor during this part of the cycle and the device will detect an invalid command or no EEPROM present.

There are two varieties of 93C46/56/66 EEPROM's on the market – one is configured as being 16 bits wide, the other is configured as being 8 bits wide. These are available from many sources such as Microchip, STMicro, ISSI etc. The FT2232C requires EEPROM's with a 16-bit wide configuration such as the Microchip 93LC46B device. The EEPROM must be capable of reading data at a 1Mb clock rate at a supply voltage of 4.35V to 5.25V. Most available parts are capable of this. Check the manufacturers data sheet to find out how to connect pins 6 and 7 of the EEPROM. Some devices specify these as no-connect, others use them for selecting 8 / 16 bit mode or for test functions. Some other parts have their pinout rotated by 90° so please select the required part and its options carefully.

It is possible to "share" the EEPROM between the FT2232C and another external device such as an MCU. However, this can only be done when the FT2232C is in its reset condition as it tri-states its EEPROM interface at that time. A typical configuration would use four bits of an MCU IO Port. One bit would be used to hold the FT2232C reset (using RESET#) on power-up, the other three would connect to the EECS, EESK and EEDATA pins of the FT2232C in order to read / write data to the EEPROM at this time. Once the MCU has read / written the EEPROM, it would take RESET# high to allow the FT2232C to configure itself and enumerate over USB.

The external EEPROM can be programmed over USB using utility software provided by FTDI. The external EEPROM is used to enable 245 FIFO, and Fast Opto-Isolated Serial interface modes on each channel.

8.3 USB Bus Powered and Self Powered Configuration

Figure 8 - USB Bus Powered Configuration

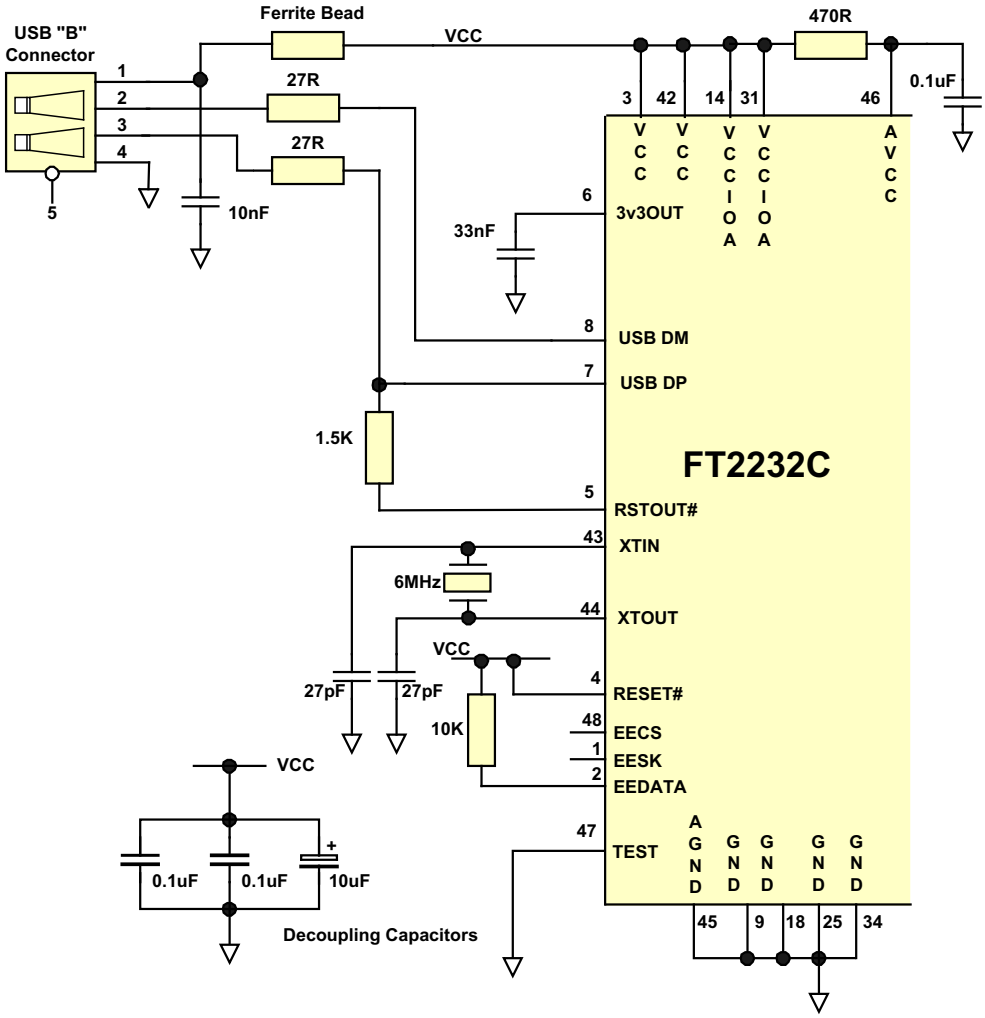


Figure 8 illustrates the FT2232C in a typical USB bus powered configuration. A USB Bus Powered device gets its power from the USB bus. Basic rules for USB Bus power devices are as follows –

a) On plug-in, the device must draw no more than 100mA
b) On USB Suspend the device must draw no more than 500µA.
c) A High Power USB Bus Powered Device (one that draws more than 100mA) should use the PWREN# pin to keep the current below 100mA on plug-in and 500µA on USB suspend.
d) A device that consumes more than 100mA can not be plugged into a USB Bus Powered Hub
e) No device can draw more that 500mA from the USB Bus.

The power descriptor in the EEPROM should be programmed to match the current draw required by the device.
A Ferrite Bead is connected in series with USB power to prevent noise from the device and associated circuitry (EMI) being radiated down the USB cable to the Host. The value of the Ferrite Bead depends on the total current required by the circuit – a suitable range of Ferrite Beads is available from Steward (**www.steward.com**) for example Steward Part # MI0805K400R-00 also available from **DigiKey,** Part # 240-1035-1.

Figure 9 - USB Self Powered Configuration

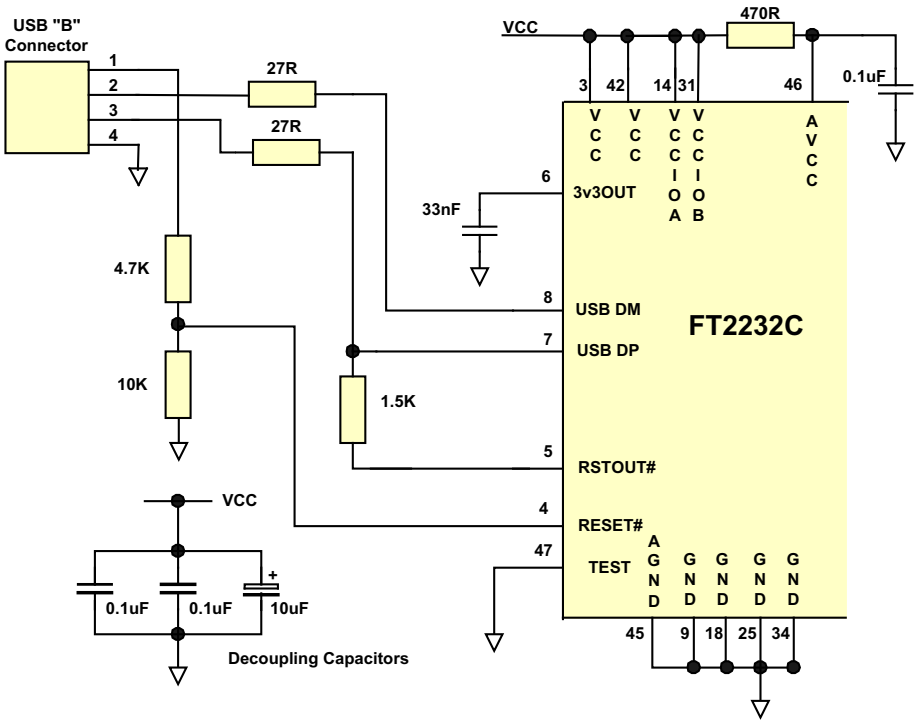


Figure 9 illustrates the FT2232C in a typical USB self powered configuration. A USB Self Powered device gets its power from its own POWER SUPPLY and does not draw current from the USB bus. The basic rules for USB Self power devices are as follows –

a) A Self-Powered device should not force current down the USB bus when the USB Host or Hub Controller is powered down.
b) A Self Powered Device can take as much current as it likes during normal operation and USB suspend as it has its own POWER SUPPLY.
c) A Self Powered Device can be used with any USB Host and both Bus and Self Powered USB Hubs.

The USB power descriptor option in the EEPROM should be programmed to a value of zero (self powered).
To meet requirement a) the 1.5K pull-up resistor on USBDP is connected to RSTOUT# as per the bus-power circuit. However, the USB Bus Power is used to control the RESET# Pin of the FT2232C device. When the USB Host or Hub is powered up RSTOUT# will pull the 1.5K resistor on USBDP to 3.3V, thus identifying the device as a full speed device to USB. When the USB Host or Hub power is off, RESET# will go low and the device will be held in reset. As RESET# is low, RSTOUT# will also be low, so no current will be forced down USBDP via the 1.5K pull-up resistor when the host or hub is powered down. Failure to do this may cause some USB host or hub controllers to power up erratically.

Note : When the FT2232C is in reset, the I/O interface pins all go tri-state. These pins have internal 200K pull-up resistors to VCCIO, so they will gently pull high unless driven by some external logic.

8.4 Interfacing to 3.3V Logic

Figure 10 - Bus Powered Circuit with 3.3V logic drive and IO supply voltage

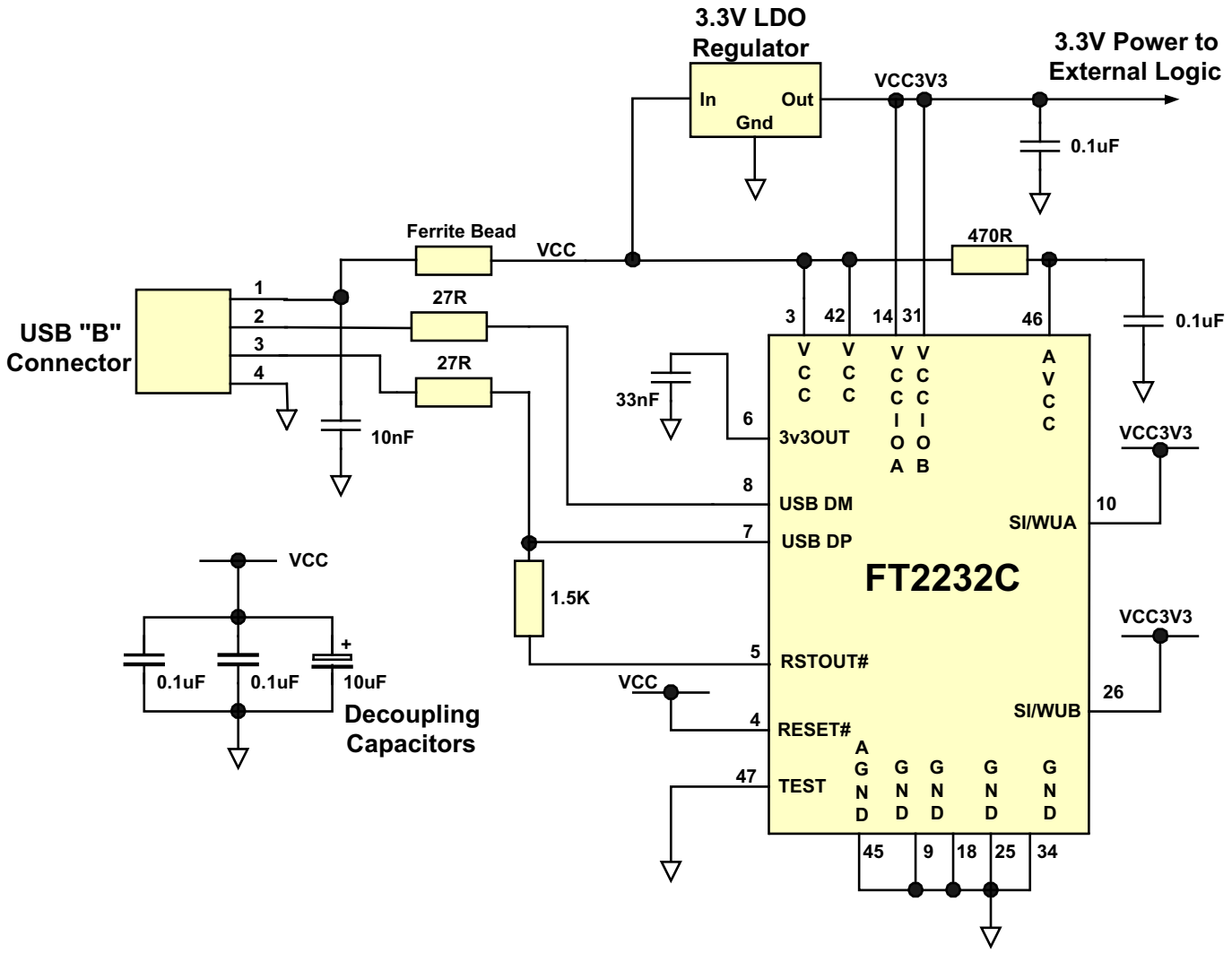


Figure 10 shows how to configure the FT2232C to interface with a 3.3V logic devices. In this example, a discrete 3.3V regulator is used to supply the 3.3V logic from the USB supply. VCCIOA and VCCIOB are connected to the output of the 3.3V regulator, which in turn will cause the device interface IO pins on both channels to drive out at 3.3V level. It is also possible to have one IO interface channel driving out at 5V level, and the other at 3.3V level. In this case one of the VCCIO pins would be connected to 5V, and the other connected to 3.3V.

For USB bus powered circuits some considerations have to be taken into account when selecting the regulator –

a) The regulator must be capable of sustaining its output voltage with an input voltage of 4.35 volts. A Low Drop Out (LDO) regulator must be selected.

b) The quiescent current of the regulator must be low in order to meet the USB suspend total current requirement of <= 500µA during USB suspend.

An example of a regulator family that meets these requirements is the MicroChip (Telcom) TC55 Series. These devices can supply up to 250mA current and have a quiescent current of under 1µA.

In some cases, where only a small amount of current is required (< 5mA) , it may be possible to use the in-built regulator of the FT2232C to supply the 3.3V without any other components being required. In this case, connect VCCIOA or VCCIOB to the 3V3OUT pin of the FT2232C.

Note : It should be emphasised that the 3.3V supply for VCCIO in a bus powered design with a 3.3V logic interface should come from an LDO which is supplied by the USB bus, or from the 3V3OUT pin of the FT232BM, and not from any other source. Please also note that if the SI/WU pins are not being used they should be pulled up to the same supply as their respective VCCIO pin.

Figure 11 - Self Powered Circuit with 3.3V logic drive and IO supply voltage

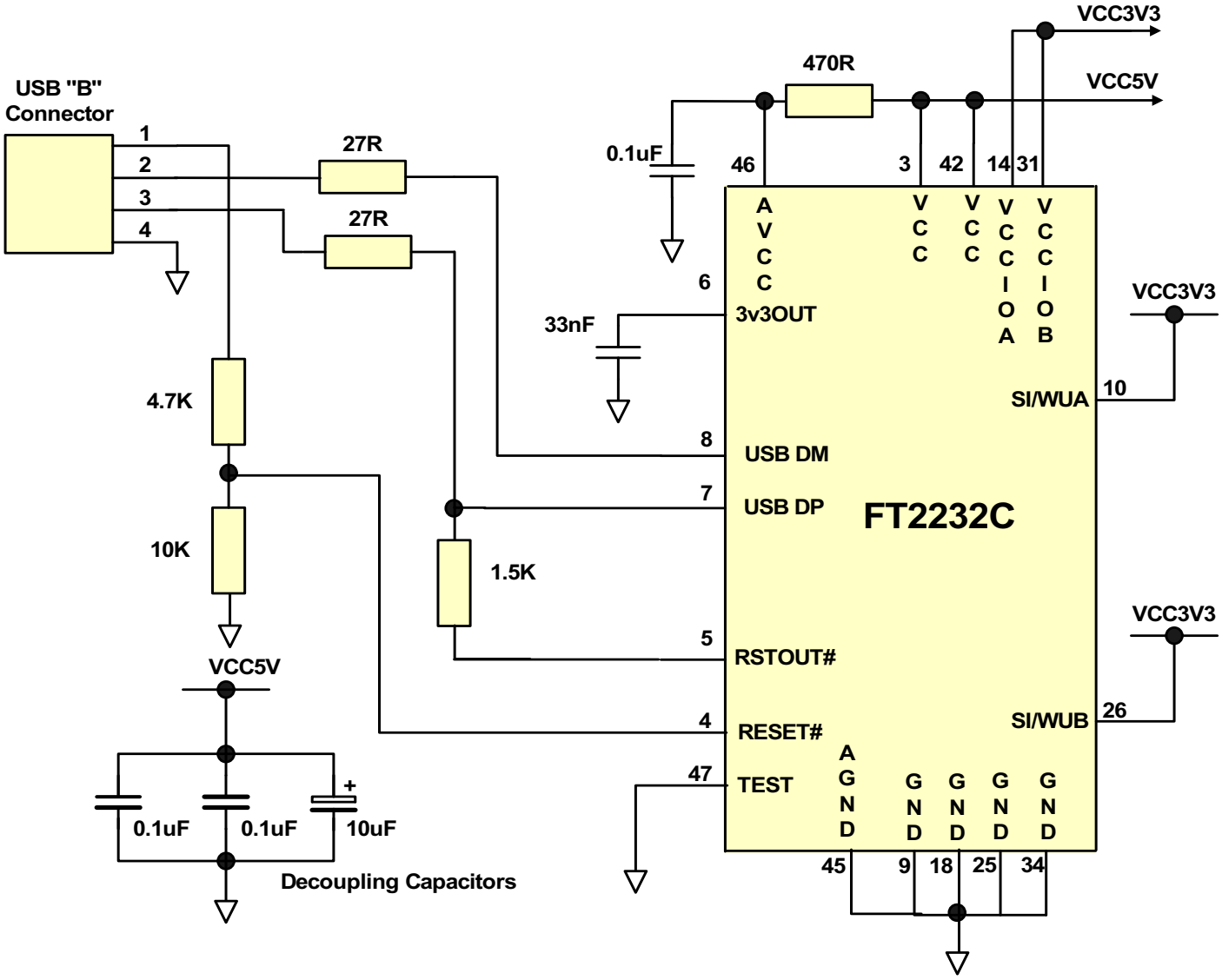


Figure 11 is an example of a FT2232C USB self powered design with 3.3V interface. In this case the VCCIOA and VCCIOB pins are supplied by an external 3.3V supply in order to make both of the device's IO channels drive out at 3.3V logic level, thus allowing them to be connected to a 3.3V MCU or other external logic. It is also possible to have one IO interface channel driving out at 5V level, and the other at 3.3V level. In this case one of the VCCIO pins would be connected to 5V, and the other connected to 3.3V.

A USB self powered design uses its own power supplies, and does not draw any of its power from the USB bus. In such cases, no special care need be taken to meet the USB suspend current (0.5 mA) as the device does not get its power from the USB port.

As with bus powered 3.3V interface designs, in some cases, where only a small amount of current is required (<5mA), it may be possible to use the in-built regulator of the FT2232C to supply the 3.3V without any other components being required. In this case, connect VCCIOA or VCCIOB to the 3V3OUT pin of the FT2232C.

Note that if the SI/WU pins are not being used they should be pulled up to the same supply as their respective VCCIO pin.