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Future Technology Devices International Ltd

FT2232D Dual USB to Serial UART/FIFO IC

The FT2232D is a dual USB to serial UART or FIFO interface with the following advanced features:

- Single chip USB to dual channel serial / parallel ports with a variety of configurations.
- Entire USB protocol handled on the chip. No USB specific firmware programming required.
- Transfer Data Rate 300 to 3 Mbaud.
- USB to parallel FIFO transfer data rate up to 1 megabyte / second.
- Multi-Protocol Synchronous Serial Engine (**MPSSE**) to simplify synchronous serial protocol (USB to JTAG, USB to I^2C, USB to SPI) design.
- CPU-style FIFO interface mode simplifies CPU interface design.
- MCU host bus emulation mode configuration option.
- Fast Opto-Isolated serial interface option.
- FTDI's royalty-free Virtual Com Port (VCP) and Direct (D2XX) drivers eliminate the requirement for USB driver development in most cases.
- Highly integrated design includes 3.3V LDO regulator for USB I/O, integrated POR function and on chip clock multiplier PLL (6MHz – 48MHz).
- Asynchronous serial UART interface option with full hardware handshaking and modem interface signals.
- Enhanced bit-bang Mode interface option with RD# and WR# strobes.
- Configurable I/O drive strength.
- Fully assisted hardware or X-On / X-Off software handshaking.
- UART Interface supports 7/8 bit data, 1/2 stop bits, and Odd/Even/Mark/Space/No Parity.
- Operational configuration mode and USB Description strings configurable in external EEPROM over the USB interface.
- Low operating and USB suspend current.
- Supports bus powered, self powered and high-power bus powered USB configurations.
- UHCI/OHCI/EHCI host controller compatible.
- USB 2.0 Full Speed (12Mbits/Second) compatible.
- Extended -40°C to 85°C industrial operating temperature range.
- Compact 48-LD Lead Free LQFP package
- +4.35V to +5.25V single supply operating voltage range.
- Dedicated Windows DLLs available for USB to JTAG, USB to SPI, and USB to I^2C applications.
- ESD protection for FT2232D IO's:
  Human Body Model (HBM) ±2kV,
  Machine Mode (MM) ±100V,
  Charge Device Model (CDM) ±500V,
  Latch-up free..

1 Typical Applications

- USB to Dual Port RS232 Converters
- USB to Dual Port RS422 / RS485 Converters
- Upgrading Legacy Peripheral Designs to USB
- USB Instrumentation
- USB JTAG Programming
- USB to SPI Bus Interfaces
- USB Industrial Control
- Field Upgradable USB Products
- Galvanically Isolated Products with USB Interface
- USB to synchronous serial interface
- Cellular and cordless phone USB data transfer cables and interfaces.
- USB Audio and Low Bandwidth Video data transfer
- PDA to USB data transfer
- USB Smart Card Readers
- USB Instrumentation
- USB Industrial Control
- USB MP3 Player Interface
- USB FLASH Card Reader / Writers
- Set Top Box PC - USB interface
- USB Digital Camera Interface
- USB Bar Code Readers
- Interfacing MCU / PLD / FPGA based designs to USB

1.0 Driver Support

The FT2232D requires USB drivers (listed below), available free from **http://www.ftdichip.com**, which are used to make the FT2232D appear as a virtual COM port (VCP). This then allows the user to communicate with the USB interface via a standard PC serial emulation port (for example TTY). Another FTDI USB driver, the D2XX driver, can also be used with application software to directly access the FT2232D though a DLL.

Royalty free VIRTUAL COM PORT (VCP) DRIVERS for...

- Windows 98, 98SE, ME, 2000, Server 2003, XP and Server 2008
- Windows XP and XP 64-bit
- Windows Vista and Vista 64-bit
- Windows XP Embedded
- Windows CE 4.2, 5.0 and 6.0
- Mac OS 8/9, OS-X
- Windows 7 32,64 bit
- Linux 2.4 and greater

Royalty free D2XX Direct Drivers (USB Drivers + DLL S/W Interface)

- Windows 98, 98SE, ME, 2000, Server 2003, XP and Server 2008
- Windows XP and XP 64-bit
- Windows Vista and Vista 64-bit
- Windows XP Embedded
- Windows CE 4.2, 5.0 and 6.0
- Windows 7 32,64 bit
- Linux 2.4 and greater

For driver installation, please refer to the application note AN232B-10.

1.1 Part Numbers

Part Number	Package
FT2232D	48 Pin LQFP

Table 1.1 Part Numbers

1.2 USB Compliant

The FT2232D is fully compliant with the USB 2.0 specification and has been given the USB-IF Test-ID (TID) 40680003.

2 FT2232D Block Diagram

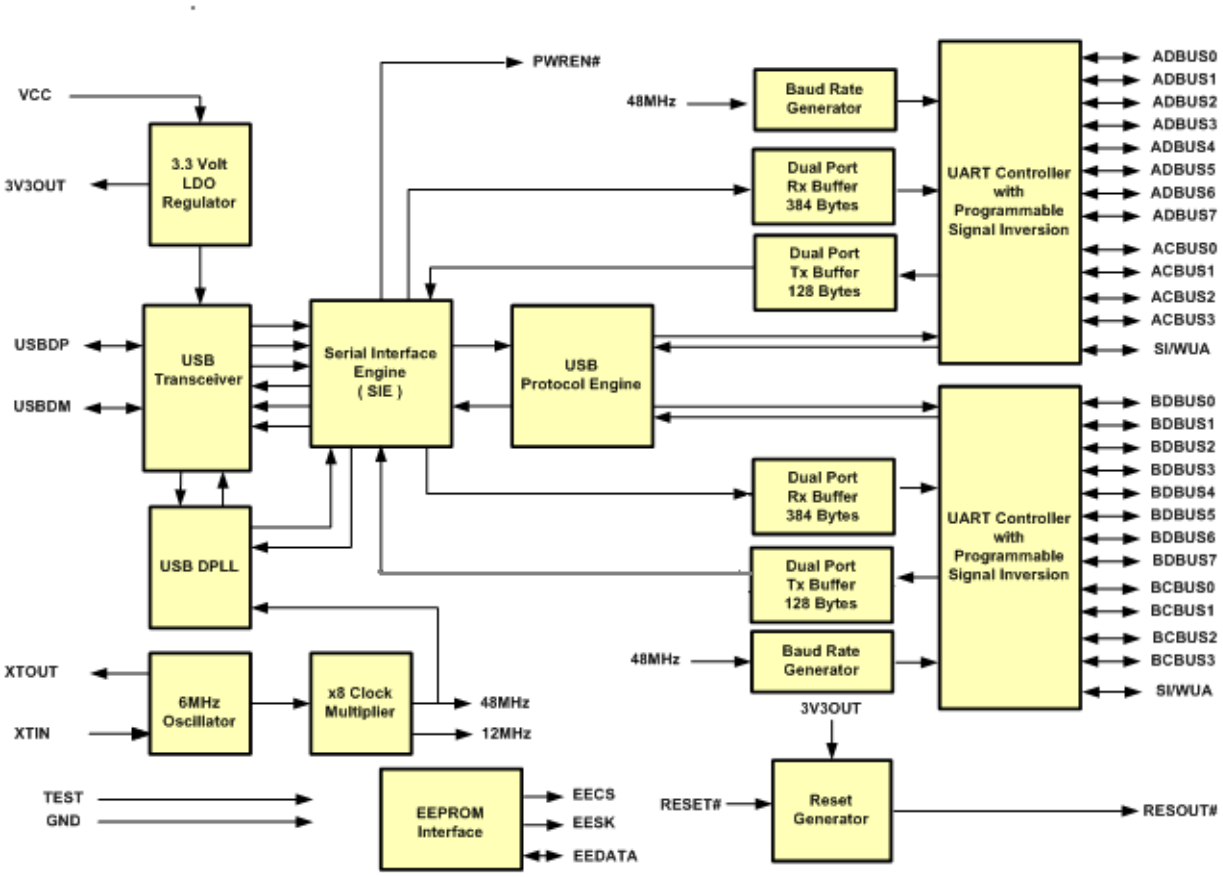

Figure 2.1 FT2232D Block Diagram

For a description of each function please refer to Section 4.1.

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3 Device Pin Out and Signal Description

3.0 48-Pin LQFP Package

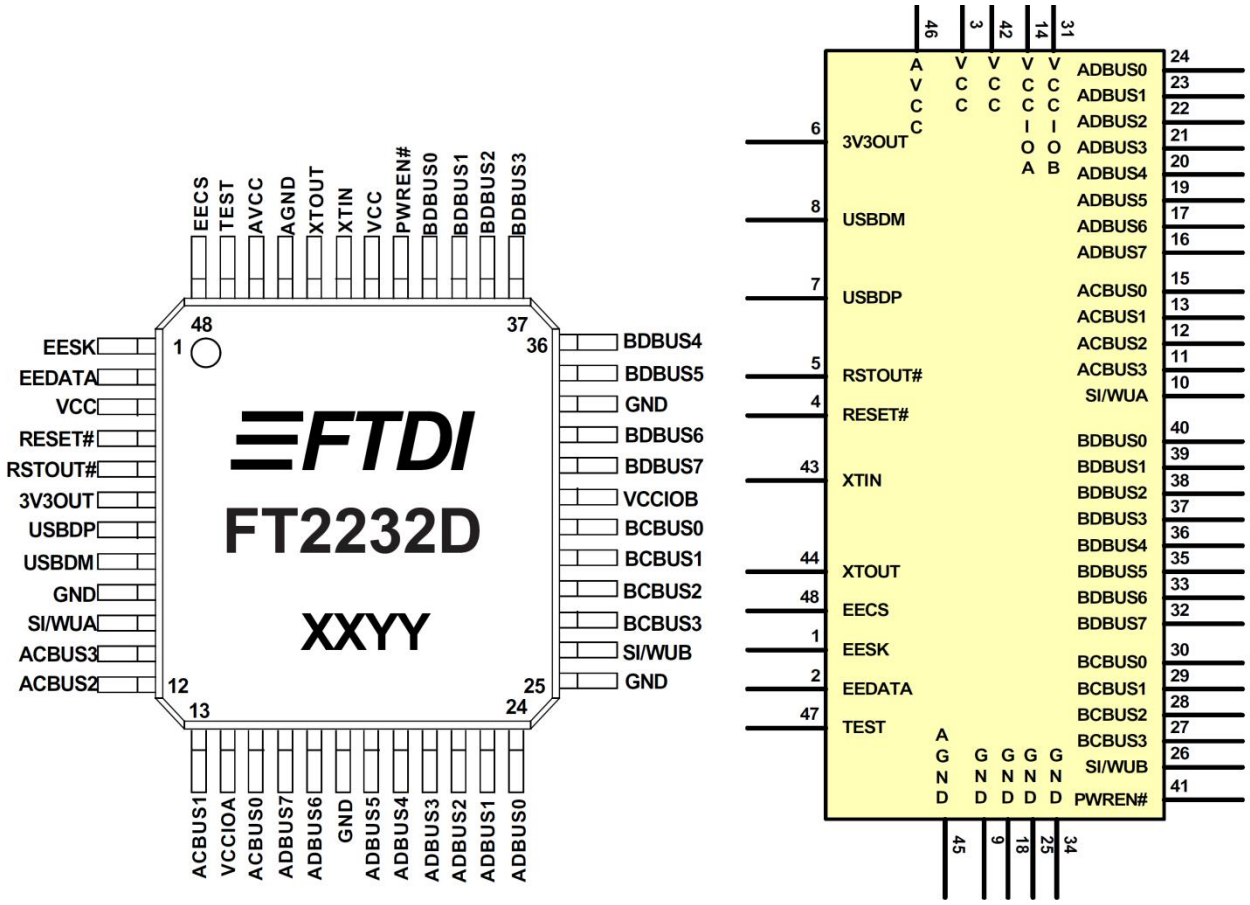

Figure 3.1 48 pin LQFP Package Pin Out and Schematic Symbol

3.1 Pin Out Description

This section describes the operation of the FT2232D pins. Common pins are defined in the first section, and then the I/O pins are defined by chip mode.

Note: The convention used throughout this document for active low signals is the signal name followed by#

3.2 Common Pins

The operation of the following FT2232D pins do not change regardless of the configured mode:-

Pin No.	Name	Type	Description
7	USBDP	I/O	USB Data Signal Plus (Requires 1.5K pull-up to 3V3OUT or RSTOUT#)
8	USBDM	I/O	USB Data Signal Minus

Table 3.1.1 USB Interface Group

Pin No.	Name	Type	Description
48	EECS	I/O	EEPROM – Chip Select. Tri-State during device reset. ****Note 1**
1	EESK	OUTPUT	Clock signal to EEPROM. Tri-State during device reset, else drives out. ****Note 1**
2	EEDATA	I/O	EEPROM – Data I/O Connect directly to Data-In of the EEPROM and to Data-Out of the EEPROM via a 2.2K resistor. Also, pull Data-Out of the EEPROM to VCC via a 10K resistor for correct operation. Tri-State during device reset. ****Note 1**

Table 3.2.2 EEPROM Interface Group

Pin No.	Name	Type	Description
4	RESET#	INPUT	Can be used by an external device to reset the FT2232D. If not required, tie to VCC. ****Note 1**
5	RSTOUT#	OUTPUT	Output of the internal Reset Generator. Drives low for 5.6 ms after VCC > 3.5V and the internal clock starts up, then clamps it's output to the 3.3V output of the internal regulator. Taking RESET# low will also force RSTOUT# to drive low. RSTOUT# is NOT affected by a USB Bus Reset.
47	TEST	INPUT	Puts device into I.C. test mode – must be tied to GND for normal operation.
41	PWREN#	OUTPUT	Goes Low after the device is configured via USB, then high during USB suspend. Can be used to control power to external logic using a P-Channel Logic Level MOSFET switch. Enable the Interface Pull-Down Option in EEPROM when using the PWREN# pin in this way.
43	XTIN	INPUT	Input to 6MHz Crystal Oscillator Cell. This pin can also be driven by an external 6MHz clock if required. Note: Switching threshold of this pin is VCC/2, so if driving from an external source, the source must be driving at 5V CMOS level or a.c. coupled to centre around VCC/2.
44	XTOUT	OUTPUT	Output from 6MHz Crystal Oscillator Cell. XTOUT stops oscillating during USB suspend, so take care if using this signal to clock external logic.

Table 3.3.3 Miscellaneous Signal Group

****Note 1 -** *During device reset, these pins are tri-state but pulled up to VCC via internal 200K resistors.*

Pin No.	Name	Type	Description
6	3V3OUT	OUTPUT	3.3 volt Output from the integrated L.D.O. regulator This pin should be decoupled to GND using a 33nF ceramic capacitor in close proximity to the device pin. It's prime purpose is to provide the internal 3.3V supply to the USB transceiver cell and the RSTOUT# pin. A small amount of current (<= 5mA) can be drawn from this pin to power external 3.3V logic if required.
3, 42	VCC	PWR	+4.35 volt to +5.25 volt VCC to the device core, LDO and non-UART / FIFO controller interface pins.
14	VCCIOA	PWR	+3.0 volt to +5.25 volt VCC to the UART / FIFO A Channel interface pins 10..13, 15..17 and 19..24. When interfacing with 3.3V external logic in a bus powered design connect VCCIO to a 3.3V supply generated from the USB bus. When interfacing with 3.3V external logic in a self powered design connect VCCIO to the 3.3V supply of the external logic. Otherwise connect to VCC to drive out at 5V CMOS level.
31	VCCIOB	PWR	+3.0 volt to +5.25 volt VCC to the UART / FIFO B Channel interface pins 26..30, 32..33 and 35..40. When interfacing with 3.3V external logic in a bus powered design connect VCCIO to a 3.3V supply generated from the USB bus. When interfacing with 3.3V external logic in a self powered design connect VCCIO to the 3.3V supply of the external logic. Otherwise connect to VCC to drive out at 5V CMOS level.
9,18, 25, 34	GND	PWR	Device - Ground Supply Pins
46	AVCC	PWR	Device - Analog Power Supply for the internal x8 clock multiplier. A low pass filter consisting of a 470 Ohm series resistor and a 100 nF to GND should be used on the supply to this pin.
45	AGND	PWR	Device - Analog Ground Supply for the internal x8 clock multiplier

Table 3.4.4 Power and Ground Group

3.3 IO Pin Definitions by Chip Mode

The FT2232D will default to dual serial mode (232 UART mode on both channel A and B, if no external EEPROM is used, or the external EEPROM is blank. The definition of the following pins varies according to the chip's mode:-

Channel A

Pin#	*Generic Pin name*	*Pin Definitions by Chip Mode **Note 2*						
		232 UART Mode	*245 FIFO*	*Enhanced Asynchronous and Synchronous Serial*	*MPSSE **Note 4*	*MCU Host Bus Emulation Mode **Note 5*	*Fast Opto-Isolated Serial Mode*	*CPU FIFO Interface Mode*
24	ADBUS0	TXD	D0	D0	TCK/SK AD0	**Note 3	D0	D0
23	ADBUS1	RXD	D1	D1	TDI/D0	AD1	D1	D1
22	ADBUS2	RTS#	D2	D2	TDO/DI	AD2	D2	D2
21	ADBUS3	CTS#	D3	D3	TMS/CS AD3	D3		D3
20	ADBUS4	DTR#	D4	D4	GPIOL0	AD4	D4	D4
19	ADBUS5	DSR#	D5	D5	GPIOL1	AD5	D5	D5
17	ADBUS6	DCD#	D6	D6	GPIOL2	AD6	D6	D6
16	ADBUS7	RI#	D7	D7	GPIOL3	AD7	D7	D7
15	ACBUS0	TXDEN	RXF#	WR# **Note 6	GPIOH0	I/O0	CS#	CS#
13	ACBUS1	SLEEP#	TXE#	RD# **Note 6	GPIOH1	I/O1	A0	A0
12	ACBUS2	RXLED#	RD#	WR# **Note 7	GPIOH2	IORDY	RD#	RD#
24	ADBUS0	TXD	D0	D0	TCK/SK AD0	**Note 3	D0	
11	ACBUS3	TXLED#	WR	RD# **Note 7	GPIOH3	OSC	WR#	WR#
10	SI/WUA	SI/WUA	SI/WUA	SI/WUA	**Note 8	**Note 8	**Note 8	**Note 8

Table 3.5.5 Pin Definition by Chip Mode (Channel A)

****Note 2:** 232 UART, 245 FIFO, CPU FIFO Interface, and Fast Opto-Isolated modes are enabled in the external EEPROM. Enhanced Asynchronous and Synchronous Bit-Bang modes, MPSSE, and MCU Host Bus Emulation modes are enabled using the driver command set bit mode. See Section 3.3 for details.

****Note 3:** Channel A can be configured in another IO mode if channel B is in Fast Opto-Isolated Serial Mode. If both Channel A and Channel B are in Fast Opto-Isolated Serial Mode all of the IO will be on Channel B.

****Note 4:** MPSSE is Channel A only.

****Note 5:** MCU Host Bus Emulation requires both Channels.

****Note 6:** The Bit-Bang Mode (synchronous and asynchronous) WR# and RD# strobes are on these pins when the main Channel mode is 245 FIFO, CPU FIFO interface, or Fast Opto-Isolated Serial Modes.

****Note 7:** The Bit-Bang Mode (synchronous and asynchronous) WR# and RD# strobes are on these pins when the main Channel mode is 232 UART Mode.

Note 8: SI/WU is not available in these modes.

Channel B

Pin#	Generic Pin name	Pin Definitions by Chip Mode **Note 2						
		232 UART Mode	245 FIFO	Enhanced Asynchronous and Synchronous Serial	MPSSE **Note 4	MCU Host Bus Emulation Mode **Note 5	Fast Opto-Isolated Serial Mode	CPU FIFO Interface Mode
40	BDBUS0	TXD	D0	D0	A8	FSDI	D0	D0
39	BDBUS1	RXD	D1	D1	A9	FSCLK	D1	D1
38	BDBUS2	RTS#	D2	D2	A10	FSDO	D2	D2
37	BDBUS3	CTS#	D3	D3	A11	FSCTS	D3	D3
36	BDBUS4	DTR#	D4	D4	A12	**Note 3	D4	D4
35	BDBUS5	DSR#	D5	D5	A13	D5		D5
33	BDBUS6	DCD#	D6	D6	A14	D6		D6
32	BDBUS7	RI#	D7	D7	A15	D7		D7
30	BCBUS0	TXDEN	RXF#	WR# **Note 9	CS#	CS#		CS#
29	BCBUS1	SLEEP#	TXE#	RD# **Note 9	ALE	A0		A0
28	BCBUS2	RXLED#	RD#	WR# **Note 7	RD#	RD#		RD#
27	BCBUS3	TXLED#	WR	RD# **Note 7	WR#	WR#		WR#
26	SI/WUB	SI/WUB	SI/WUB	SI/WUB	**Note 8	**Note 8	SI/WUB	**Note 8
40	BDBUS0	TXD	D0	D0	A8	FSDI	D0	

Table 3.6.6 Pin Definition by Chip Mode (Channel B)

Note 2: 232 UART, 245 FIFO, CPU FIFO Interface, and Fast Opto-Isolated modes are enabled in the external EEPROM. Enhanced Asynchronous and Synchronous Bit-Bang modes, MPSSE, and MCU Host Bus Emulation modes are enabled using the driver command set bit mode. See Section 3.3 for details.

Note 3: Channel A can be configured in another IO mode if channel B is in Fast Opto-Isolated Serial Mode. If both Channel A and Channel B are in Fast Opto-Isolated Serial Mode all of the IO will be on Channel B.

Note 4: MPSSE is Channel A only.

Note 5: MCU Host Bus Emulation requires both Channels.

Note 6: The Bit-Bang Mode (synchronous and asynchronous) WR# and RD# strobes are on these pins when the main Channel mode is 245 FIFO, CPU FIFO interface, or Fast Opto-Isolated Serial Modes.

Note 7: The Bit-Bang Mode (synchronous and asynchronous) WR# and RD# strobes are on these pins when the main Channel mode is 232 UART Mode.

Note 8: SI/WU is not available in these modes.

Note 9: The Bit-Bang Mode (synchronous and asynchronous) WR# and RD# strobes are on these pins when the main Channel mode is 245 FIFO, CPU FIFO interface. Bit-Bang mode is not available on Channel B when Fast Opto-Isolated Serial Mode is enabled.

3.4 IO Mode Command Hex Values

Enhanced Asynchronous and Synchronous Bit-Bang modes, MPSSE, and MCU Host Bus Emulation modes are enabled using the D2XX driver command FT_SetBitMode. The hex values used with this command to enable these modes are as follows-

Mode	Value (Hex)
Reset the IO bit Mode	0
Asynchronous Bit Bang Mode	1
MPSSE	2
Synchronous Bit bang Mode	4
MCU Host bus Emulation	8
Fast Opto-Isolated Serial Mode	10

Table 3.7.7 IO Mode Command Hex Values

See application note **AN2232-02, "Bit Mode Functions for the FT2232D"** for more details and examples.

Note that all other device modes can be enabled in the external EEPROM, and do not require these values to be configured.

In the case of Fast Opto-Isolated Serial mode sending a value of 10 will hold this device mode in reset, and sending a value of 0 will release this mode from reset.

4 Function Description

The FT2232D is a USB to serial UART interface device which incorporates the functionality of two of FTDI's second generation FT232BM and FT245BM chips into a single device. A single downstream USB port is converted to two IO channels which can each be individually configured as a FT232BM-style UART interface, or a FT245BM-style FIFO interface, without the need to add a USB hub. In addition a new high drive level option means that the device UART / FIFO IO pins will drive out at around three times the normal power level, meaning that the bus can be shared by several devices.

4.0 Key Features

Two Individually Configurable IO Channels: Each of the FT2232D's Channels (A and B) can be individually configured as a FT232BM-style UART interface, or as a FT245BM-style FIFO interface. In addition these channels can be configured in a number of special IO modes.
Integrated Power-On-Reset (POR) circuit: The device incorporates an internal POR function. A RESET# pin is available to allow external logic to reset the device where required, however for most applications this pin can simply be hardwired to Vcc. A RSTOUT# pin is provided in order to allow the new POR circuit to provide a stable reset to external MCU and other devices.
Integrated RCCLK circuit: Used to ensure that the oscillator and clock multiplier PLL frequency are stable prior to USB enumeration.
Integrated level converter on UART / FIFO interface and control signals: Each channel of the FT2232D has its own independent VCCIO pin that can be supplied by between 3V to 5V. This allows each channel's output voltage drive level to be individually configured. Thus allowing, for example 3.3V logic to be interfaced to the device without the need for external level converter I.C.'s.
Improved power management control for high-power USB Bus Powered devices: The PWREN# pin will become active when the device is enumerated by USB, and be deactivated when the device is in USB suspend. This can be used to directly drive a transistor or P-Channel MOSFET in applications where power switching of external circuitry is required. The BM pull down enable feature (configured in the external EEPROM) is also retained. This will make the device gently pull down on the FIFO / UART IO lines when the power is shut off (PWREN# is high). In this mode any residual voltage on external circuitry is bled to GND when power is removed, thus ensuring that external circuitry controlled by PWREN# resets reliably when power is restored.
Send Immediate / Wake Up Signal Pin on each channel: There is a Send Immediate / Wake Up (SI/WU) signal pins on each of the chips channels. These combine two functions on one pin. If USB is in suspend mode (and remote wakeup is enabled in the EEPROM), strobing this pin low will cause the device to request a resume from suspend (WakeUp) on the USB Bus. Normally, this can be used to wake up the Host PC. During normal operation, if this pin is strobed low any data in the device RX buffer will be sent out over USB on the next Bulk-IN request from the drivers regardless of the packet size. This can be used to optimise USB transfer speed for some applications.
Low suspend current: The suspend current of the FT2232D is typically under 100 µA (excluding the 1.5K pull up resistor on USBDP) in USB suspend mode. This allows greater margin for peripherals to meet the USB Suspend current limit of 500uA.
Programmable Receive Buffer Timeout: The TX buffer timeout is programmable over USB in 1ms increments from 1ms to 255ms, thus allowing the device to be better optimised for protocols requiring faster response times from short data packets.
Relaxed VCC Decoupling: The improved level of Vcc decoupling that was incorporated into BM devices has also been implemented in the FT2232D device.
Baud Rate Pre-Scaler Divisors: The FT2232D (UART mode) baud rate pre-scaler supports division by (n+0), (n+0.125), (n+0.25), (n+0.375), (n+0.5), (n+0.625), (n+0.75) and (n+0.875) where n is an integer between 2 and 16,384 (2^{14}).
Extended EEPROM Support: The FT2232D supports 93C46 (64 x 16 bit), 93C56 (128 x 16 bit), and 93C66 (256 x 16 bit) EEPROMs. The extra space is not used by the device. However it is available for use by other external MCU / logic whilst the FT2232D is being held in reset. There is now an additional 64 words of space available (128bytes total) in the user area when a 93C56 or 93C66 is used.
USB 2.0 (full speed option): An EEPROM based option allows the FT2232D to return a USB 2.0 device descriptor as opposed to USB 1.1. Note: The device would be a USB 2.0 Full Speed device (12Mb/s) as opposed to a USB 2.0 High Speed device (480Mb/s).

In addition to the BM chip features, the FT2232D incorporates the following new features and interface modes:-

Enhanced Asynchronous Bit-Bang Interface: The FT2232D supports FTDI's BM chip Bit Bang mode. In Bit Bang mode, the eight FIFO data lines can be switched between FIFO interface mode and an 8-bit Parallel IO port. Data packets can be sent to the device and they will be sequentially sent to the interface at a rate controlled by an internal time (equivalent to the baud rate prescaler). With the FT2232D device this mode has been enhanced so that the internal RD# and WR# strobes are now brought out of the device which can be used to allow external logic to be clocked by accesses to the Bit-Bang IO bus.

Synchronous Bit-Bang Interface: Synchronous Bit-Bang Mode differs from Asynchronous Bit-Bang mode in that the device is only read when it is written to. Thus making it easier for the controlling program to measure the response to an output stimulus as the data returned is synchronous to the output data.

High Output Drive Level Capability: The IO interface pins can be made to drive out at three times the standard drive level thus allowing multiple devices, or devices that require a greater drive strength to be interfaced to the FT2232D. This option is configured in the external EEPROM, ad can be set individually for each channel.

Multi-Protocol Synchronous Serial Engine Interface (M.P.S.S.E.): The Multi-Protocol Synchronous Serial Engine (MPSSE) interface is a new option designed to interface efficiently with synchronous serial protocols such as JTAG and SPI Bus. It is very flexible in that it can be configured for different industry standards, or proprietary bus protocols. For instance, it is possible to connect one of the FT2232D's channels to an SRAM configurable FPGA as supplied by vendors such as Altera and Xilinx. The FPGA device would normally be un-configured (i.e. have no defined function) at power-up. Application software on the PC could use the MPSSE to download configuration data to the FPGA over USB. This data would define the hardware's function on power up. The other FT2232 channel would be available for other devices. This approach would allow a customer to create a "generic" USB peripheral, whose hardware function can be defined under control of the application software. The FPGA based hardware could be easily upgraded or totally changed simply by changing the FPGA configuration data file. (See FTDI's MORPH-IC development module for a practical example, **www.morph-ic.com**)

MCU Host Bus Emulation: This new mode combines the 'A' and 'B' bus interface to make the FT2232D interface emulate a standard 8048 / 8051 style MCU bus. This allows peripheral devices for these MCU families to be directly attached to the FT2232D with IO being performed over USB with the help of MPSSE interface technology.

CPU-Style FIFO Interface: The CPU style FIFO interface is essentially the same function as the classic FT245 interface; however the bus signals have been redefined to make them easier to interface to a CPU bus.

Fast Opto-Isolated Serial Interface: A new proprietary FTDI protocol is designed to allow galvanically isolated devices to communicate synchronously with the FT2232D using just 4 signal wires (over two dual opto-isolators), and two power lines. The peripheral circuitry controls the data transfer rate in both directions, whilst maintaining full data integrity. Maximum USB full speed data rates can be achieved. Both 'A' and 'B' channels can communicate over the same 4 wire interface if desired.

4.1 Functional Block Descriptions

The following paragraphs detail each function within the FT2232D. Please refer to the block diagram shown in Figure 2.1.

3.3V LDO Regulator: The 3.3V LDO Regulator generates the 3.3 volt reference voltage for driving the USB transceiver cell output buffers. It requires an external decoupling capacitor to be attached to the 3V3OUT regulator output pin. It also provides 3.3V power to the RSTOUT# pin. The main function of this block is to power the USB Transceiver and the Reset Generator Cells rather than to power external logic. However, external circuitry requiring 3.3V nominal at a current of not greater than 5mA could also draw its power from the 3V3OUT pin if required

USB Transceiver: The USB Transceiver Cell provides the USB 1.1 or USB 2.0 full-speed physical interface to the USB cable. The output drivers provide 3.3 volt level slew rate control signalling, whilst a differential receiver and two single ended receivers provide USB data in, SEO and USB Reset condition detection.

USB DPLL: The USB DPLL cell locks on to the incoming NRZI USB data and provides separate recovered clock and data signals to the SIE block.

6MHz Oscillator: The 6MHz Oscillator cell generates a 6MHz reference clock input to the x8 Clock multiplier from an external 6MHz crystal or ceramic resonator.

x8 Clock Multiplier: The x8 Clock Multiplier takes the 6MHz input from the Oscillator cell and generates a 48MHz reference clock for the USB DPPL and the Baud Rate Generator blocks.

Serial Interface Engine (SIE): The Serial Interface Engine (SIE) block performs the Parallel to Serial and Serial to Parallel conversion of the USB data. In accordance to the USB 2.0 specification, it performs bit stuffing / un- stuffing and CRC5 / CRC16 generation / checking on the USB data stream.

USB Protocol Engine: The USB Protocol Engine manages the data stream from the device USB control endpoint. It handles the low level USB protocol (Chapter 9) requests generated by the USB host controller and the commands for controlling the functional parameters of the UART / FIFO controller blocks.

Dual Port TX Buffers (128 bytes): Data from the USB data out endpoint is stored in the Dual Port TX buffer and removed from the buffer to the transmit register under control of the UART FIFO controller.

Dual Port RX Buffers (384 bytes): Data from the UART / FIFO controller receive register is stored in the Dual Port RX buffer prior to being removed by the SIE on a USB request for data from the device data in endpoint.

Multi-Purpose UART / FIFO Controllers: The Multi-purpose UART / FIFO controllers handle the transfer of data between the Dual Port RX and TX buffers and the UART / FIFO transmit and receive registers. When configured as a UART it performs asynchronous 7 / 8 bit Parallel to Serial and Serial to Parallel conversion of the data on the RS232 (RS422 and RS485) interface. Control signals supported by UART mode include RTS, CTS, DSR, DTR, DCD and RI. There are also transmitter enable control signal pins (TXDEN) provided to assist with interfacing to RS485 transceivers. RTS/CTS, DSR/DTR and Xon/Xoff handshaking options are also supported. Handshaking, where required, is handled in hardware to ensure fast response times. The UART's also supports the RS232 BREAK setting and detection conditions.

Baud Rate Generator: The Baud Rate Generator provides a x16 clock input to the UART's from the 48MHz reference clock and consists of a 14 bit prescaler and 3 register bits which provide fine tuning of the baud rate (used to divide by a number plus a fraction). This determines the Baud Rate of the UART which is programmable from 183 baud to 3 million baud.

RESET Generator: The Reset Generator Cell provides a reliable power-on reset to the device internal circuitry on power up. An additional RESET# input and RSTOUT# output are provided to allow other devices to reset the FT2232D, or the FT2232D to reset other devices respectively. During reset, RSTOUT# is driven low, otherwise it drives out at the 3.3V provided by the onboard regulator. RSTOUT# can be used to control the 1.5K pull-up on USBDP directly where delayed USB enumeration is required. It can also be used to reset other devices. RSTOUT# will stay high- impedance for approximately 5ms after VCC has risen above 3.5V AND the device oscillator is running AND RESET# is high. RESET# should be tied to VCC unless it is a requirement to reset the device from external logic or an external reset generator I.C.

EEPROM Interface: When used without an external EEPROM the FT2232D be configured as a USB to dual serial port device. Adding an external 93C46 (93C56 or 93C66) EEPROM allows each of the chip's channels to be independently configured as a serial UART (232 mode), or a parallel FIFO (245 mode). The external EEPROM is used to enable the Fast Opto-Isolated Serial interface mode.

The external EEPROM can also be used to customise the USB VID, PID, Serial Number, Product Description Strings and Power Descriptor value of the FT2232D for OEM applications. Other parameters controlled by the EEPROM include Remote Wake Up, Soft Pull Down on Power-Off and USB 2.0 descriptor modes. The EEPROM should be a 16 bit wide

configuration such as a MicroChip 93LC46B or equivalent capable of a 1Mb/s clock rate at VCC = 4.35V to 5.25V. The EEPROM is programmable-on board over USB using a utility program available from FTDI's web site (**www.ftdichip. com**). This allows a blank part to be soldered onto the PCB and programmed as part of the manufacturing and test process. If no EEPROM is connected (or the EEPROM is blank), the FT2232D will default to dual serial ports. The device uses its built-in default VID, PID Product Description and Power Descriptor Value. In this case, the device will not have a serial number as part of the USB descriptor.

5 Devices Characteristics and Ratings

5.0 Absolute Maximum Ratings

These are absolute maximum ratings for the for the FT2232D device in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these may cause permanent damage to the device.

Parameter	Value	Unit
Storage Temperature	-65°C to 150°C	Degrees C
Floor Life (Out of Bag) At Factory Ambient (30°C / 60% Relative Humidity)	192 (IPC/JEDEC J-STD-033A MSL Level 3 Compliant)**Note 10	Hours
Ambient Temperature (Power Applied)	-40°C to 85°C	Degrees C
VCC Supply Voltage	-0.5 to +6.00	V
DC Input Voltage – USBDP and USBDM	-0.5 to +3.8	V
DC Input Voltage – High Impedance Bidirectional	-0.5 to + (VCC +0.5)	V
DC Input Voltage – All Other Inputs	-0.5 to + (VCC +0.5)	V
DC Output Current – Outputs	24	mA
DC Output Current – Low Impedance Bidirectional	24	mA
Power Dissipation (VCC = 5.25V)	500	mW
Electrostatic Discharge Voltage (Human Body Model) (I < 1µA)	+/- 3000	V
Latch Up Current (Vi = +/- 10V maximum, for 10 ms	200	mA

Table 5.1 Absolute Maximum Ratings

****Note 10** if devices are stored out of the packaging beyond this time limit the devices should be baked before use. The devices should be ramped up to a temperature of 110°C and baked for 8 to 10 hours.

5.1 DC Characteristics

DC Characteristics (Ambient Temperature = -40°C to +85°C)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
VCC1	VCC Operating Supply Voltage	4.35	5.0	5.25	V	
VCC2	VCCIO Operating Supply Voltage	3.0	-	5.25	V	
Icc1	Operating Supply Current	---	30	---	mA	Normal Operation
Icc2	Operating Supply Current	---	100	200	µA	USB Suspend ****Note 11**

Table 5.2 Operating Voltage and Current

****Note 11** - Supply current excludes the 200µA nominal drawn by the external pull-up resistor on USBDP.

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	3.2	4.1	4.9	V	I source = 2mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 2mA
Vin	Input Switching Threshold	1.3	1.2	1.5	V	
VHys	Input Switching Hysteresis	50	25	30	mV	

Table 5.3 IO Pin Characteristics (VCCIO = 5.0V, Standard Drive Level) **Note 12

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.2	2.7	3.2	V	I source = 1mA
Vol	Output Voltage Low	0.3	0.4	0.5	V	I sink = 2mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	
VHys	Input Switching Hysteresis	20	25	30	mV	

Table 5.4 IO Pin Characteristics (VCCIO = 3.0V – 3.6V, Standard Drive Level) **Note 12

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	3.2	4.1	4.9	V	I source
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 6 mA
Vin	Input Switching Threshold	1.3	1.6	1.9	V	
VHys	Input Switching Hysteresis	50	55	60	mV	

Table 5.5 IO Pin Characteristics (VCCIO = 5.0V, High Drive Level) **Note 12 and 13

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	2.2	2.8	3.2	V	I source = 3mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 8 mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	
VHys	Input Switching Hysteresis	20	25	30	mV	

Table 5.6 IO Pin Characteristics (VCCIO = 3.0V -3.6V, High Drive Level) **Note 12 and 13

****Note 12:** Inputs have an internal 200K pull-up resistor to VCCIO, which can alternativly be programmed to pull down using a configuration bit in the external EEPROM.

****Note 13:** The high output drive level is configured in the external EEPROM. Each channel can be configured individually.

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	4.0	-	5.0	V	Fosc = 6MHz
Vol	Output Voltage Low	0.1	-	1.0	V	Fosc = 6MHz
Vin	Input Switching Threshold	1.8	2.5	3.2	V	
Voh	Output Voltage High	4.0	-	5.0	V	Fosc = 6MHz

Table 5.7 XTIN / XTOUT Pin Characteristics

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	3.2	4.1	4.9	V	I source = 2mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 2 mA
Vin	Input Switching Threshold	1.3	1.6	1.9	V	
VHys	Input Switching Hysteresis	50	55	60	mV	

Table 5.8 RESET# and TEST EECS, EESK, EEDATA Pin Characteristics **Note 14

****Note 14** - EECS, EESK, EEDATA and RESET# pins have an internal 200K pull-up resistor to VCC

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
Voh	Output Voltage High	3.0	-	3.6	V	I source = 2mA
Vol	Output Voltage Low	0.3	-	0.6	V	I sink = 2mA

Table 5.9 RSTOUT# Pin Characteristics

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
UVoh	I/O Pins Static Output (High)	2.8	-	3.6	V	RI = 1.5kΩ to 3V3OUT (D+) RI = 15KΩ to GND (D-)
UVol	I/O Pins Static Output (Low)	0	-	0.3	V	RI = 1.5kΩ to 3V3OUT (D+) RI = 15kΩ to GND (D-)
UVse	Single Ended Rx Threshold	0.8	-	2.0	V	
UCom	Differential Common Mode	0.8	-	2.5	V	
UVDif	Differential Input Sensitivity	0.2	-	-	V	
UDrvZ	Driver Output Impedance	26	-	44	Ohms	

Table 5.10 USB I/O Pin (USBDP, USBDM) Characteristics **Note 15

****Note 15** - Driver Output Impedance includes the external 27R series resistors on USBDP and USBDM pins.

5.2 ESD Tolerance

ESD protection for FT2232D IO's

Parameter	Reference	Minimum	Typical	Maximum	Units
Human Body Model (HBM)	JEDEC EIA/JESD22-A114-B, Class 2		±2kV		kV
Machine Mode (MM)	JEDEC EIA/JESD22-A115-A, Class A		±100V		V
Charge Device Model (CDM)	JEDEC EIA/ JESD22-C101-D, Class-III		±500V		V
Latch-up	JESD78, Trigger Class-II		±200mA		mA

Table 5.11 ESD Tolerance

6 USB Power Configurations

The following sections illustrate possible USB power configurations for the FT2232D.

6.0 USB Bus Powered Configuration

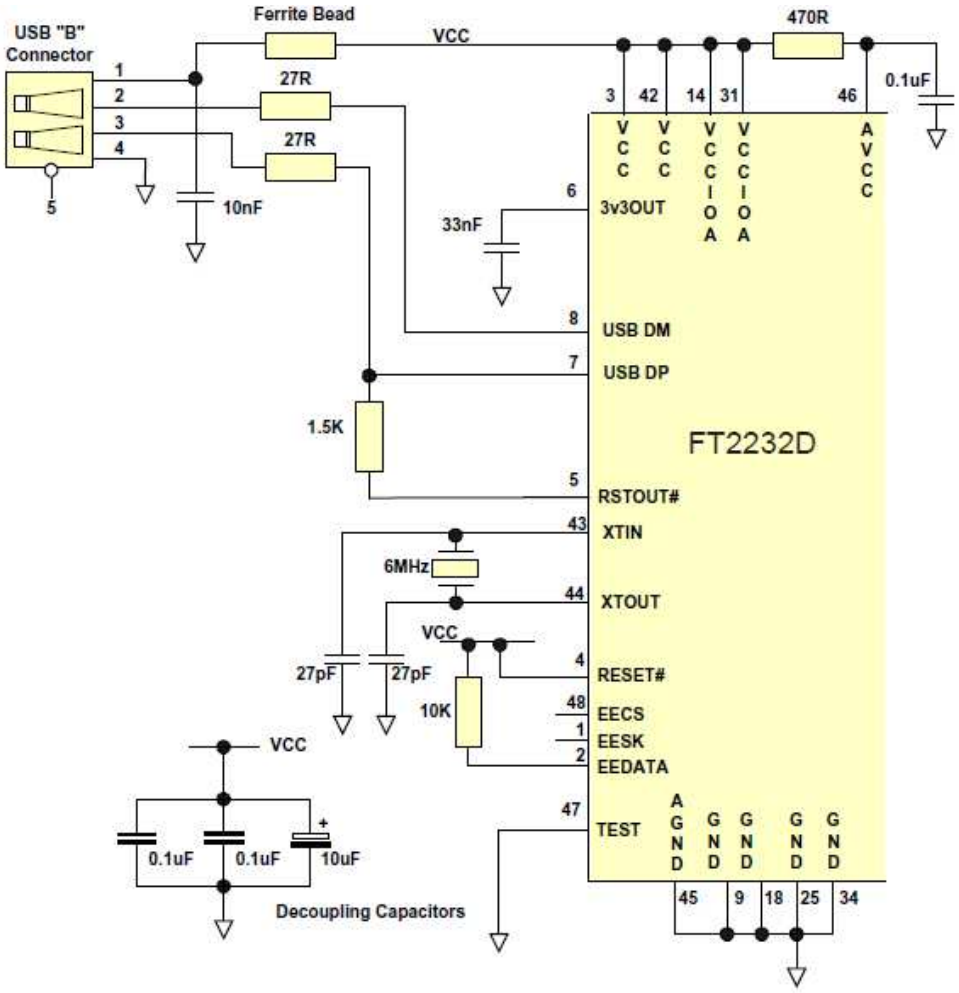

Figure 6.1 Bus Powered Configuration

Figure 6.1 illustrates the FT2232D in a typical USB bus powered configuration. A USB Bus Powered device gets its power from the USB bus. Basic rules for USB Bus power devices are as follows:-

a) On plug-in, the device must draw no more than 100mA

b) On USB Suspend the device must draw no more than 500µA.

c) A High Power USB Bus Powered Device (one that draws more than 100mA) should use the PWREN# pin to keep the current below 100mA on plug-in and 500µA on USB suspend.

d) A device that consumes more than 100mA cannot be plugged into a USB Bus Powered Hub

e) No device can draw more that 500mA from the USB Bus.

The power descriptor in the EEPROM should be programmed to match the current draw required by the device. A Ferrite Bead is connected in series with USB power to prevent noise from the device and associated circuitry (EMI) being radiated down the USB cable to the Host. The value of the Ferrite Bead depends on the total current required by the circuit - a suitable range of Ferrite Beads is available from Steward (**www.steward.com**) for example Steward Part # MI0805K400R-00 also available from DigiKey, Part # 240-1035-1.

6.1 USB Self Powered Configuration

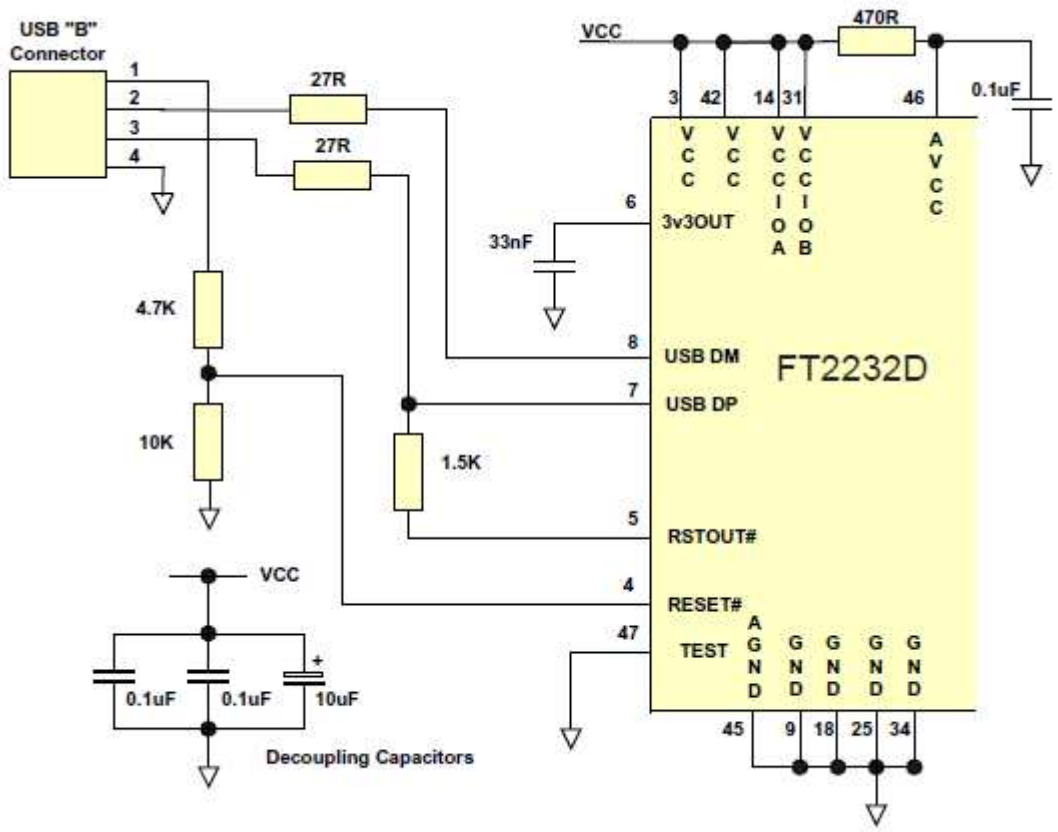

Figure 6.2 Self Powered Configuration

Figure 6.2 illustrates the FT2232D in a typical USB self powered configuration. A USB Self Powered device gets its power from its own POWER SUPPLY and does not draw current from the USB bus. The basic rules for USB Self power devices are as follows –

a) A Self-Powered device should not force current down the USB bus when the USB Host or Hub Controller is powered down.
b)A Self Powered Device can take as much current as it likes during normal operation and USB suspend as it has its own POWER SUPPLY.
c)A Self Powered Device can be used with any USB Host and both Bus and Self Powered USB Hubs.

The USB power descriptor option in the EEPROM should be programmed to a value of zero (self powered). To meet requirement a) the 1.5 K pull-up resistors on USBDP is connected to RSTOUT# as per the bus-power circuit. However, the USB Bus Power is used to control the RESET# Pin of the FT2232D device. When the USB Host or Hub is powered up RSTOUT# will pull the 1.5K resistor on USBDP to 3.3V, thus identifying the device as a full speed device to USB. When the USB Host or Hub power is off, RESET# will go low and the device will be held in reset. As RESET# is low, RSTOUT# will also be low, so no current will be forced down USBDP via the 1.5K pull-up resistor when the host or hub is powered down. Failure to do this may cause some USB host or hub controllers to power up erratically. Note: When the FT2232D is in reset, the I/O interface pins all go tri-state. These pins have internal 200K pull-up resistors to VCCIO, so they will gently pull high unless driven by some external logic.

6.2 Interfacing to 3.3V Logic

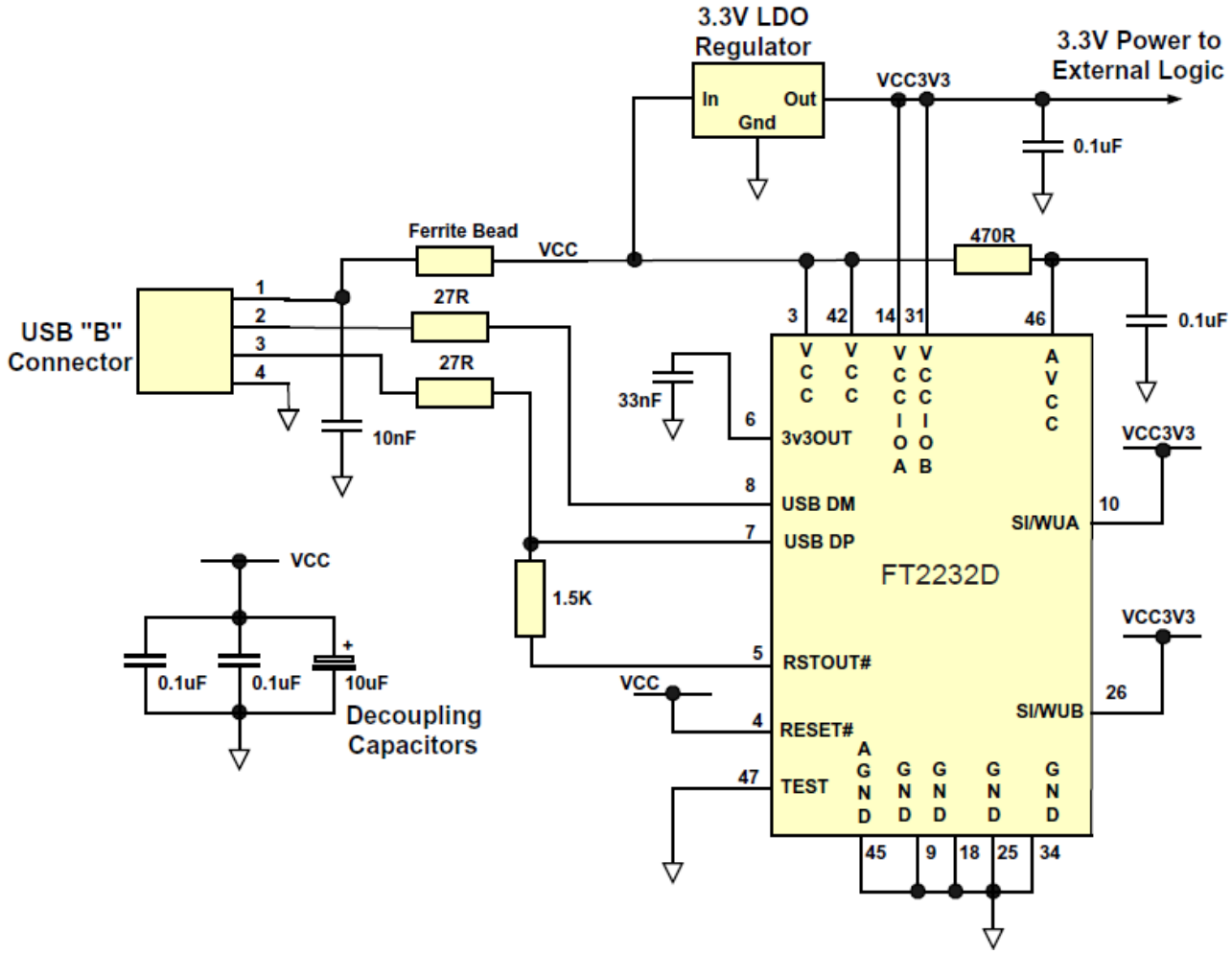

Figure 6.3 Bus Powered Circuit with 3.3V logic drive and IO supply voltage

Figure 6.3 shows how to configure the FT2232D to interface with 3.3V logic devices. In this example, a discrete 3.3V regulator is used to supply the 3.3V logic from the USB supply. VCCIOA and VCCIOB are connected to the output of the 3.3V regulator, which in turn will cause the device interface IO pins on both channels to drive out at 3.3V level. It is also possible to have one IO interface channel driving out at 5V level, and the other at 3.3V level. In this case one of the VCCIO pins would be connected to 5V, and the other connected to 3.3V.

For USB bus powered circuits some considerations have to be taken into account when selecting the regulator:-

a) The regulator must be capable of sustaining its output voltage with an input voltage of 4.35 volts. A Low Drop Out (LDO) regulator must be selected.

b) The quiescent current of the regulator must be low in order to meet the USB suspend total current requirement of <= 500µA during USB suspend.

An example of a regulator family that meets these requirements is the MicroChip (Telcom) TC55 Series. These devices can supply up to 250mA current and have a quiescent current of under 1µA. In some cases, where only a small amount of current is required (< 5mA) , it may be possible to use the in-built regulator of the FT2232D to supply the 3.3V without any other components being required. In this case, connect VCCIOA or VCCIOB to the 3V3OUT pin of the FT2232D.

Note: It should be emphasised that the 3.3V supply for VCCIO in a bus powered design with a 3.3V logic interface should come from an LDO which is supplied by the USB bus, or from the 3V3OUT pin of the FT232BM, and not from any other source. Please also note that if the SI/WU pins are not being used they should be pulled up to the same supply as their respective VCCIO pin.

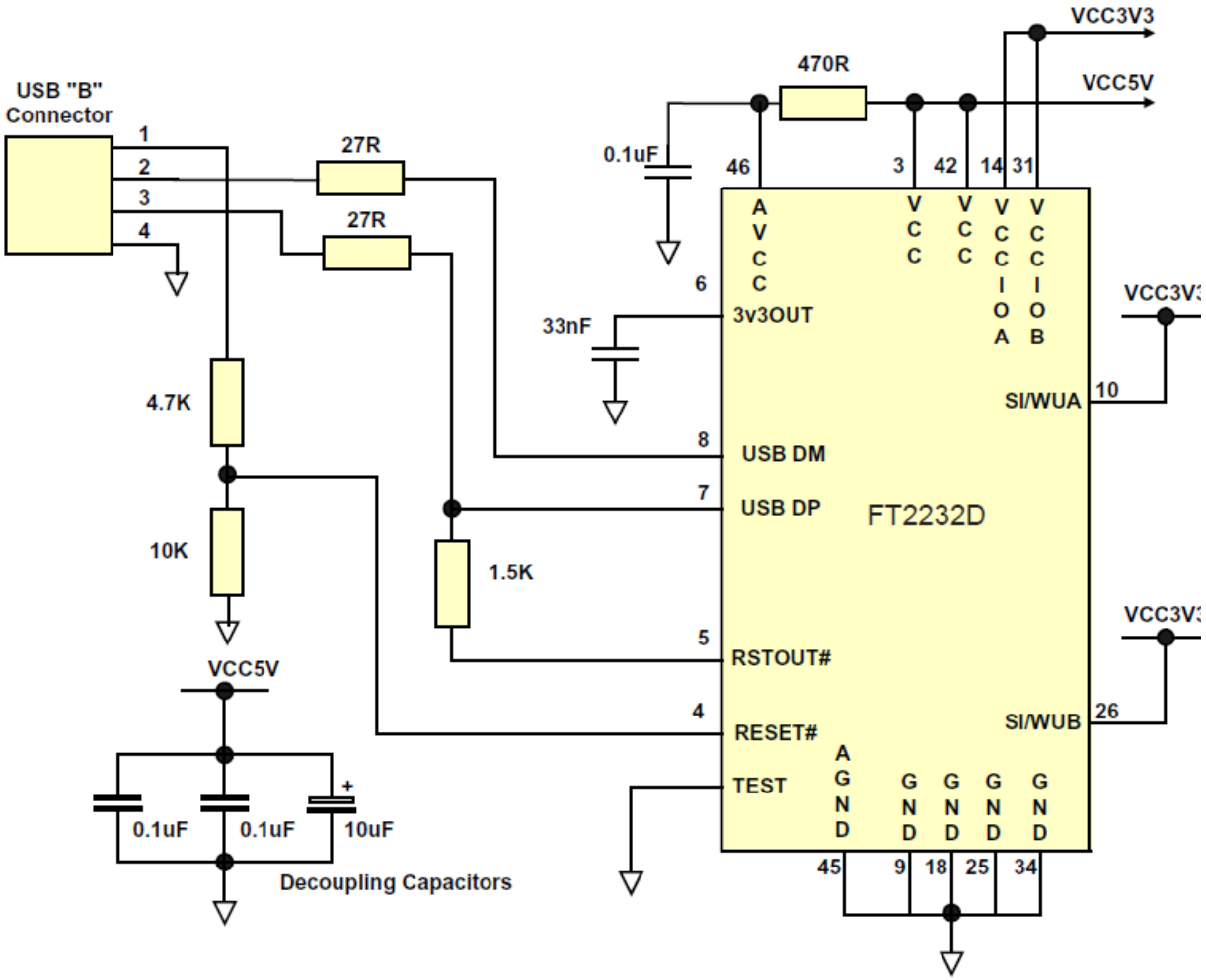

Figure 6.4 Self Powered Circuit with 3.3V logic drive and IO supply voltage

Figure 6.4 is an example of a FT2232D USB self powered design with 3.3V interface. In this case the VCCIOA and VCCIOB pins are supplied by an external 3.3V supply in order to make both of the device's IO channels drive out at 3.3V logic level, thus allowing them to be connected to a 3.3V MCU or other external logic. It is also possible to have one IO interface channel driving out at 5V level, and the other at 3.3V level. In this case one of the VCCIO pins would be connected to 5V, and the other connected to 3.3V. A USB self powered design uses its own power supplies, and does not draw any of its power from the USB bus. In such cases, no special care need be taken to meet the USB suspend current (0.5 mA) as the device does not get its power from the USB port. As with bus powered 3.3V interface designs, in some cases, where only a small amount of current is required (<5mA), it may be possible to use the in-built regulator of the FT2232D to supply the 3.3V without any other components being required. In this case, connect VCCIOA or VCCIOB to the 3V3OUT pin of the FT2232D. Note that if the SI/WU pins are not being used they should be pulled up to the same supply as their respective VCCIO pin.

6.3 Power Switching Configuration

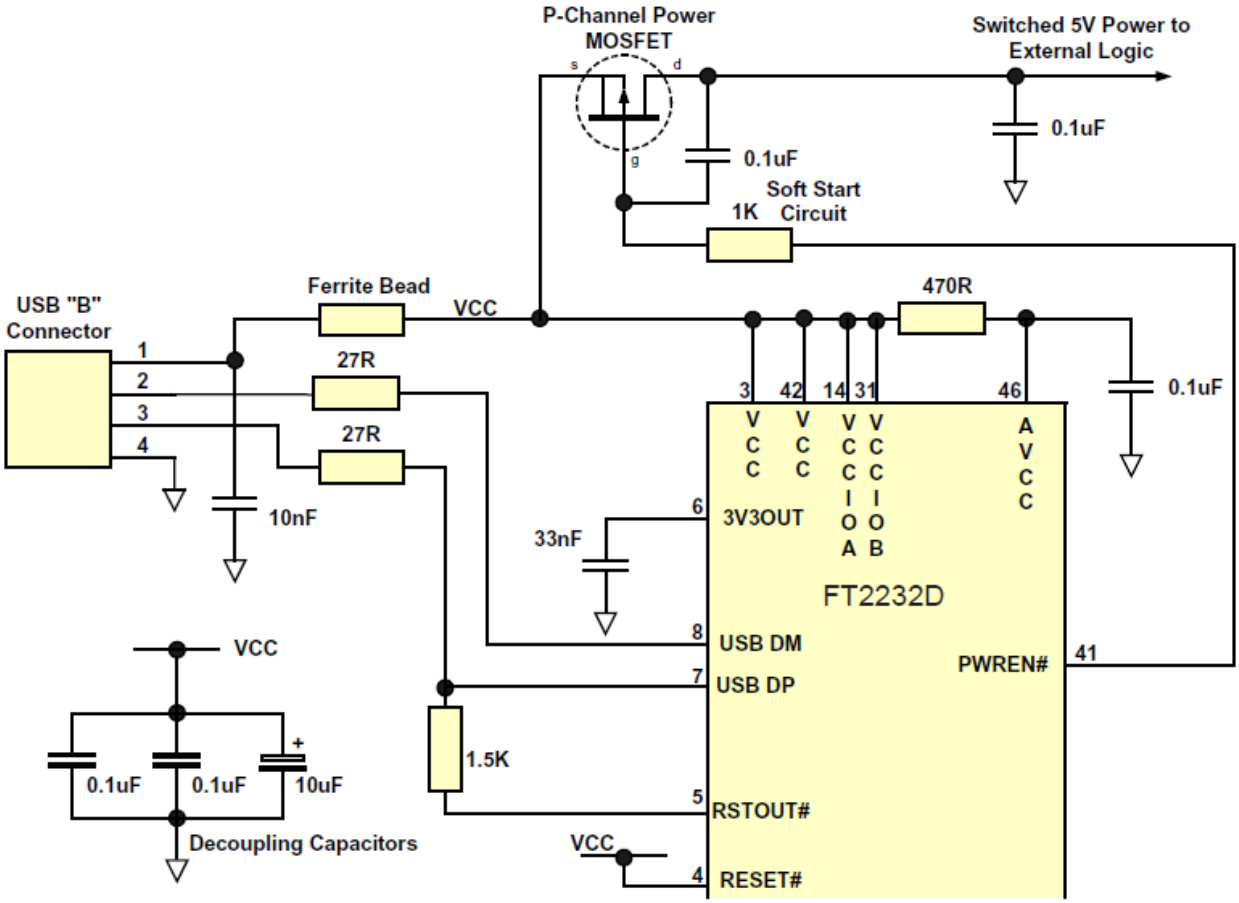

Figure 6.5 Bus Powered Circuit with Power Control

USB Bus powered circuits need to be able to power down in USB suspend mode in order to meet the <= 500µA total suspend current requirement (including external logic). Some external logic can power itself down into a low current state by monitoring the PWREN# pin. For external logic that cannot power itself down in that way, the FT2232D provides a simple but effective way of turning off power to external circuitry during USB suspend.

Figure 6.5 shows how to use a discrete P-Channel Logic Level MOSFET to control the power to external logic circuits. A suitable device would be an International Rectifier (**www.irf.com**) IRLML6402, or equivalent. It is recommended that a "soft start" circuit consisting of a 1K series resistor and a 0.1 µF capacitor are used to limit the current surge when the MOSFET turns on. Without the soft start circuit there is a danger that the transient power surge of the MOSFET turning on will reset the FT2232D, or the USB host / hub controller. The values used here allow attached circuitry to power up with a slew rate of ~12.5 V per millisecond, in other words the output voltage will transition from GND to 5V in approximately 400 microseconds.

Alternatively, a dedicated power switches I.C. with inbuilt "soft-start" can be used instead of a MOSFET. A suitable power switch I.C. for such an application would be a Micrel (**www.micrel.com**) MIC2025-2BM or equivalent. Please note the following points in connection with power controlled designs: –

a)The logic to be controlled must have its own reset circuitry so that it will automatically reset itself when power is re-applied on coming out of suspend.

b)Set the Pull-down on Suspend option in the FT2232D's EEPROM.

c)For USB high-power bus powered device (one that consumes greater than 100 mA, and up to 500 mA of current from the USB bus), the power consumption of the device should be set in the max power field in the EEPROM. A high-power bus powered device must use this descriptor in the EEPROM to inform the system of its power requirements.

d)For 3.3V power controlled circuits the VCCIO pins must not be powered down with the external circuitry. Either connect the power switch between the output of the 3.3V regulator and the external 3.3V logic, or if appropriate power the VCCIO pin from the 3V3OUT pin of the FT2232D.