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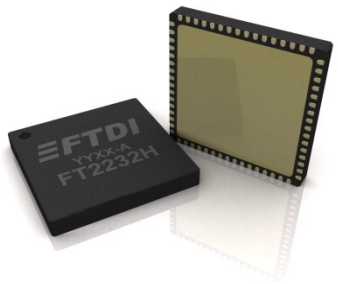
Future Technology Devices International Ltd

FT2232H Dual High Speed USB to Multipurpose UART/FIFO IC



The FT2232H is FTDI's 5th generation of USB devices. The FT2232H is a USB 2.0 High Speed (480Mb/s) to UART/FIFO IC. It has the capability of being configured in a variety of industry standard serial or parallel interfaces. The FT2232H has the following advanced features:

- Single chip USB to dual serial / parallel ports with a variety of configurations.
- Entire USB protocol handled on the chip. No USB specific firmware programming required.
- USB 2.0 High Speed (480Mbits/Second) and Full Speed (12Mbits/Second) compatible.
- Dual Multi-Protocol Synchronous Serial Engine (MPSSE) to simplify synchronous serial protocol (USB to JTAG, I^2C, SPI or bit-bang) design.
- Dual independent UART or FIFO or MPSSE ports.
- Independent Baud rate generators.
- RS232/RS422/RS485 UART Transfer Data Rate up to 12Mbaud. (RS232 Data Rate limited by external level shifter).
- USB to parallel FIFO transfer data rate up to 8 Mbyte/Sec.
- Single channel synchronous FIFO mode for transfers upto 40 Mbytes/Sec
- CPU-style FIFO interface mode simplifies CPU interface design.
- MCU host bus emulation mode configuration option.
- Fast Opto-Isolated serial interface option.
- FTDI's royalty-free Virtual Com Port (VCP) and Direct (D2XX) drivers eliminate the requirement for USB driver development in most cases.
- Adjustable receive buffer timeout.
- Option for transmit and receive LED drive signals on each channel.
- Enhanced bit-bang Mode interface option with RD# and WR# strobes
- FT245B-style FIFO interface option with bi-directional data bus and simple 4 wire handshake interface.
- Highly integrated design includes +1.8V LDO regulator for VCORE, integrated POR function and on chip clock multiplier PLL (12MHz – 480MHz).
- Asynchronous serial UART interface option with full hardware handshaking and modem interface signals.
- Fully assisted hardware or X-On / X-Off software handshaking.
- UART Interface supports 7/8 bit data, 1/2 stop bits, and Odd/Even/Mark/Space/No Parity.
- Auto-transmit enable control for RS485 serial applications using TXDEN pin.
- Operational configuration mode and USB Description strings configurable in external EEPROM over the USB interface.
- Configurable I/O drive strength (4, 8, 12 or 16mA) and slew rate.
- Low operating and USB suspend current.
- Supports bus powered, self powered and high-power bus powered USB configurations.
- UHCI/OHCI/EHCI host controller compatible.
- USB Bulk data transfer mode (512 byte packets in High Speed mode).
- +1.8V (chip core) and +3.3V I/O interfacing (+5V Tolerant).
- Extended -40°C to 85°C industrial operating temperature range.
- Compact 64-LD Lead Free LQFP or QFN package
- +3.3V single supply operating voltage range.
- ESD protection for FT2232H IO's:
  Human Body Model (HBM) ±2kV,
  Machine Mode (MM) ±200V,
  Charge Device Model (CDM) ±500V,
  Latch-up free.

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1 Typical Applications

- Single chip USB to dual channel UART (RS232, RS422 or RS485).
- Single chip USB to dual channel FIFO.
- Single chip USB to dual channel JTAG.
- Single chip USB to dual channel SPI.
- Single chip USB to dual channel I2C.
- Single chip USB to dual channel Bit-Bang.
- Single chip USB to dual combination of any of above interfaces.
- Single chip USB to Fast Serial Optic Interface.
- Single chip USB to CPU target interface (as memory), double and independent.
- Single chip USB to Host Bus Emulation (as CPU).
- PDA to USB data transfer
- USB Smart Card Readers
- USB Instrumentation
- USB Industrial Control
- USB MP3 Player Interface
- USB FLASH Card Reader / Writers
- Set Top Box PC - USB interface
- USB Digital Camera Interface
- USB Bar Code Readers

1.1 Driver Support

The FT2232H requires USB drivers (listed below) , available free from **http://www.ftdichip.com**, which are used to make the FT2232H appear as a virtual COM port (VCP). This allows the user to communicate with the USB interface via a standard PC serial emulation port (for example TTY). Another FTDI USB driver, the D2XX driver, can also be used with application software to directly access the FT2232H through a DLL.

Royalty free VIRTUAL COM PORT (VCP) DRIVERS for...

- Windows 2000, Server 2003, Server 2008
- Windows XP and XP 64-bit
- Windows Vista and Vista 64-bit
- Windows XP Embedded
- Windows CE 4.2, 5.0, 5.2 and 6.0
- Mac OS-X
- Linux (2.6.39 or later)
- Windows 7 and Windows 7 64-bit

Royalty free D2XX *Direct* Drivers (USB Drivers + DLL S/W Interface)

- Windows 2000, Server 2003, Server 2008
- Windows XP and XP 64-bit
- Windows Vista and Vista 64-bit
- Windows XP Embedded
- Windows CE 4.2, 5.0, 5.2 and 6.0
- Linux (2.4 or later) and Linux x86_64
- Windows 7 and Windows 7 64-bit

For driver installation, please refer to the application note:

- **AN_107, "Advanced Driver Options"**.
- **AN_103, "FTDI Drivers Installation Guide for VISTA".**
- **AN_119, "FTDI Drivers Installation Guide for Windows7".**
- **AN_104, "FTDI Drivers Installation Guide for WindowsXP".**

The following additional installation guides application notes and technical notes are also available:

- **AN_113, "Interfacing FT2232H Hi-Speed Devices To I2C Bus".**
- **AN_109 – "Programming Guide for High Speed FTCI2C DLL"**
- **AN_110 – "Programming Guide for High Speed FTCJTAG DLL"**
- **AN_111 – "Programming Guide for High Speed FTCSPI DLL"**
- **AN 113 – "Interfacing FT2232H Hi-Speed Devices To I2C Bus"**
- **AN114 – "Interfacing FT2232H Hi-Speed Devices To SPI Bus"**

- **AN135 – MPSSE Basics**
- **AN108 - Command Processor For MPSSE and MCU Host Bus Emulation Modes**
- **TN_104, "Guide to Debugging Customers Failed Driver Installation"**

1.2 Part Numbers

Part Number	Package
FT2232HL-xxxx	64 Pin LQFP
FT2232HQ-xxxx	64 Pin QFN

Note: Packaging code for xxxx is:

- Reel: Taped and Reel (LQFP =1000 pcs per reel, QFN =4000 pcs per reel)

-Tray: Tray packing, (LQFP =160 pcs per tray, QFN =260 pcs per tray)

Please refer to section 8 for all package mechanical parameters.

1.3 USB Compliant

The FT2232H is fully compliant with the USB 2.0 specification and has been given the USB-IF Test-ID (TID) 40720019.

The timing of the rise/fall time of the USB signals is not only dependant on the USB signal drivers, it is also dependant system and is affected by factors such as PCB layout, external components and any transient protection present on the USB signals. For USB compliance these may require a slight adjustment. This timing can be modified through a programmable setting stored in the same external EEPROM that is used for the USB descriptors. Timing can also be changed by adding appropriate passive components to the USB signals.

2 FT2232H Block Diagram

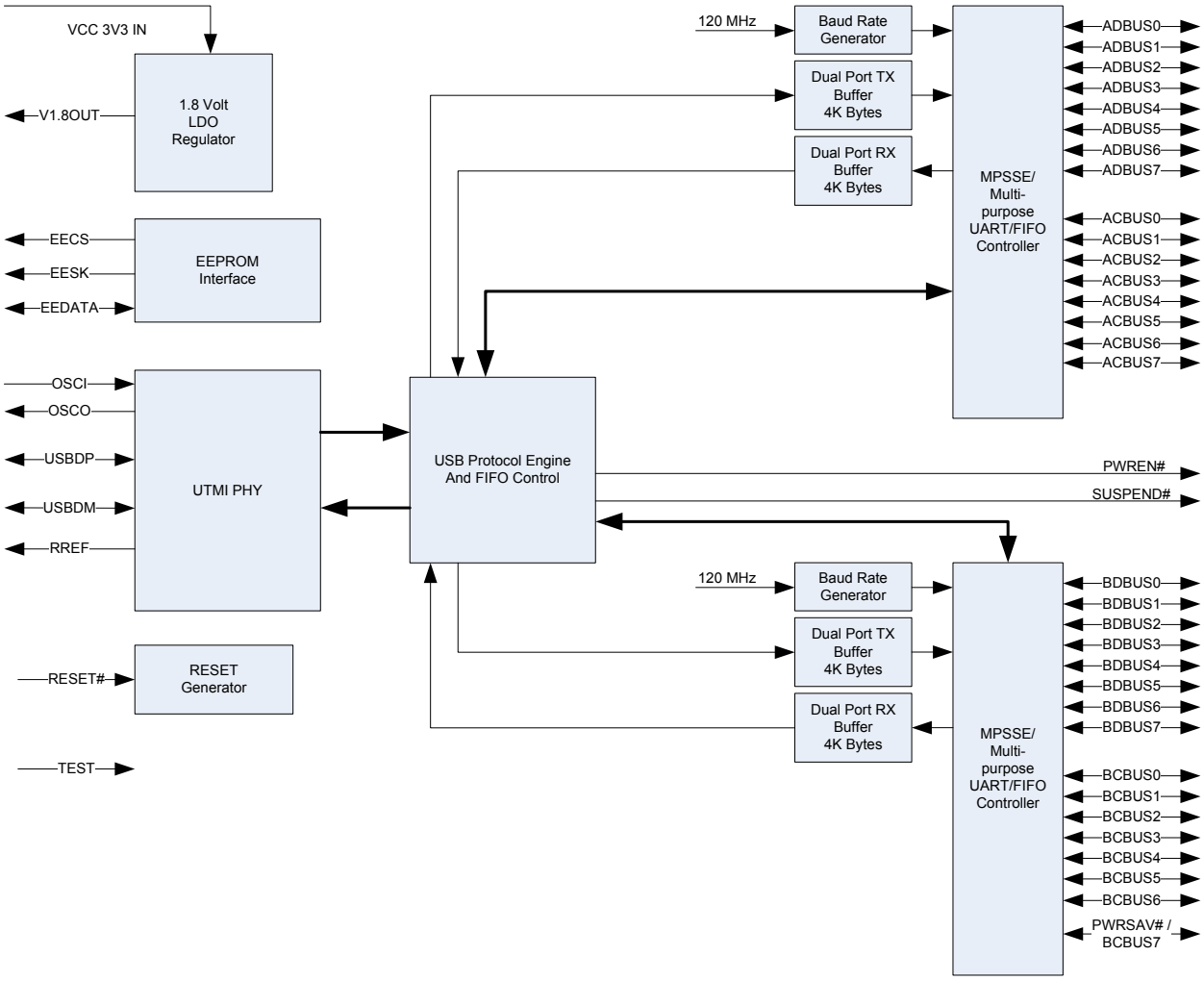

Figure 2.1 FT2232H Block Diagram

For a description of each function please refer to Section 4.

Table of Contents

3 Device Pin Out and Signal Description

The 64-pin LQFP and 64-pin QFN have the same pin numbering for specific functions. This pin numbering is illustrated in the schematic symbol shown in **Figure 3.1**.

3.1 64-Pin LQFP and 64-Pin QFN Package Schematic Symbol

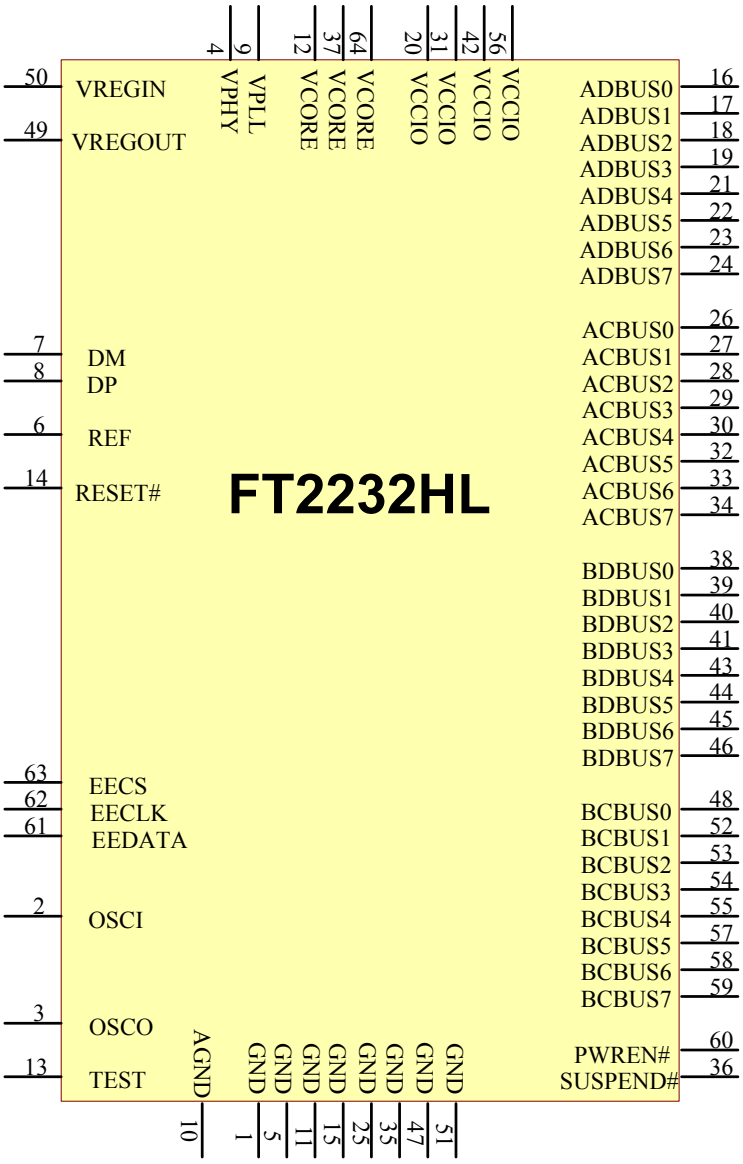

Figure 3.1 FT2232H Schematic Symbol

3.2 FT2232H Pin Descriptions

This section describes the operation of the FT2232H pins. Both the LQFP and the QFN packages have the same function on each pin. The function of many pins is determined by the configuration of the FT2232H. The following table details the function of each pin dependent on the configuration of the interface. Each of the functions are described in the following table (Note: The convention used throughout this document for active low signals is the signal name followed by a #).

Pins marked ** default to tri-stated inputs with an internal 75KΩ (approx) pull up resistor to VCCIO.

FT2232H										
Pin		Pin functions (depends on configuration)								
Pin #	Pin Name	ASYNC Serial (RS232)	245 FIFO SYNC	245 FIFO	ASYNC Bit-bang	SYNC Bit-bang	MPSSE	Fast Serial interface	CPU Style FIFO	Host Bus Emulation
		Channel A								
16	ADBUS0	TXD	D0	D0	D0	D0	TCK/SK	USES CHANNEL B	D0	AD0
17	ADBUS1	RXD	D1	D1	D1	D1	TDI/DO		D1	AD1
18	ADBUS2	RTS#	D2	D2	D2	D2	TDO/DI		D2	AD2
19	ADBUS3	CTS#	D3	D3	D3	D3	TMS/CS		D3	AD3
21	ADBUS4	DTR#	D4	D4	D4	D4	GPIOL0		D4	AD4
22	ADBUS5	DSR#	D5	D5	D5	D5	GPIOL1		D5	AD5
23	ADBUS6	DCD#	D6	D6	D6	D6	GPIOL2		D6	AD6
24	ADBUS7	RI#	D7	D7	D7	D7	GPIOL3		D7	AD7
26	ACBUS0	TXDEN	RXF#	RXF#	**	**	GPIOH0		CS#	A8
27	ACBUS1	**	TXE#	TXE#	WRSTB#	WRSTB#	GPIOH1		A0	A9
28	ACBUS2	**	RD#	RD#	RDSTB#	RDSTB#	GPIOH2		RD#	A10
29	ACBUS3	RXLED#	WR#	WR#	**	**	GPIOH3		WR#	A11
30	ACBUS4	TXLED#	SIWUA	SIWUA	SIWUA	SIWUA	GPIOH4		SIWUA	A12
32	ACBUS5	**	CLKOUT	**	**	**	GPIOH5		**	A13
33	ACBUS6	**	OE#	**	**	**	GPIOH6		**	A14
34	ACBUS7	**	**	**	**	**	GPIOH7		**	A15
		Channel B								
38	BDBUS0	TXD		D0	D0	D0	TCK/SK	FSDI	D0	CS#
39	BDBUS1	RXD		D1	D1	D1	TDI/DO	FSCLK	D1	ALE
40	BDBUS2	RTS#		D2	D2	D2	TDO/DI	FSDO	D2	RD#
41	BDBUS3	CTS#		D3	D3	D3	TMS/CS	FSCTS	D3	WR#
43	BDBUS4	DTR#		D4	D4	D4	GPIOL0		D4	IORDY
44	BDBUS5	DSR#		D5	D5	D5	GPIOL1		D5	CLKOUT
45	BDBUS6	DCD#		D6	D6	D6	GPIOL2		D6	I/O0
46	BDBUS7	RI#		D7	D7	D7	GPIOL3		D7	I/O1
48	BCBUS0	TXDEN		RXF#	**	**	GPIOH0		CS#	**
52	BCBUS1	**		TXE#	WRSTB#	WRSTB#	GPIOH1		A0	**
53	BCBUS2	**		RD#	RDSTB#	RDSTB#	GPIOH2		RD#	**
54	BCBUS3	RXLED#		WR#	**	**	GPIOH3		WR#	**
55	BCBUS4	TXLED#		SIWUB	SIWUB	SIWUB	GPIOH4	SIWUB	SIWUB	**
57	BCBUS5	**		**	**	**	GPIOH5		**	**
58	BCBUS6	**		**	**	**	GPIOH6		**	**
59	BCBUS7	PWRSAV#	PWRSAV#	PWRSAV#	PWRSAV#	PWRSAV#	GPIOH7	PWRSAV#	PWRSAV#	PWRSAV#
60	PWREN#	PWREN#	PWREN#	PWREN#	PWREN#	PWREN#	PWREN#	PWREN#	PWREN#	PWREN#

36	SUSPEND#	SUSPEND#	SUSPEND #	SUSPEND #	SUSPEND #	SUSPEND #	SUSPEND #	SUSPEND #	SUSPEND#	SUSPEND #
Configuration memory interface										
63	EECS									
62	EECLK									
61	EEDATA									

3.3 Common Pins

The operation of the following FT2232H pins are the same regardless of the configured mode:-

Pin No.	Name	Type	Description
12,37,64	VCORE	POWER Input	+1.8V input. Core supply voltage input.
20,31,42,56	VCCIO	POWER Input	+3.3V input. I/O interface power supply input. Failure to connect all VCCIO pins will result in failure of the device.
9	VPLL	POWER Input	+3.3V input. Internal PHY PLL power supply input. It is recommended that this supply is filtered using an LC filter.
4	VPHY	POWER Input	+3.3V Input. Internal USB PHY power supply input. Note that this cannot be connected directly to the USB supply. A +3.3V regulator must be used. It is recommended that this supply is filtered using an LC filter.
50	VREGIN	POWER Input	+3.3V Input. Integrated 1.8V voltage regulator input.
49	VREGOUT	POWER Output	+1.8V Output. Integrated voltage regulator output. Connect to VCORE with 3.3uF filter capacitor.
10	AGND	POWER Input	0V Analog ground.
1,5,11,15, 25,35,47,51	GND	POWER Input	0V Ground input.

Table 3.1 Power and Ground

Pin No.	Name	Type	Description
2	OSCI	INPUT	Oscillator input.
3	OSCO	OUTPUT	Oscillator output.
6	REF	INPUT	Current reference – connect via a 12KΩ resistor @ 1% to GND.
7	DM	INPUT	USB Data Signal Minus.
8	DP	INPUT	USB Data Signal Plus.
13	TEST	INPUT	IC test pin – for normal operation should be connected to GND.
14	RESET#	INPUT	Reset input (active low).
60	PWREN#	OUTPUT	Active low power-enable output. PWREN# = 0: Normal operation. PWREN# =1 : USB SUSPEND mode or device has not been configured. This can be used by external circuitry to power down logic when device is in USB suspend or has not been configured.
36	SUSPEND#	OUTPUT	Active low when USB is in suspend mode.
59	PWRSAV#	INPUT	USB Power Save input. This is an EEPROM configurable option used when the FT2232H is used in a self powered mode and is used to prevent forcing current down the USB lines when the host or hub is powered off. PWRSAV# = 1 : Normal Operation PWRSAV# = 0 : FT2232H forced into SUSPEND mode. PWRSAV# can be connected to GND (via a 10KΩ resistor) and another resistor (e.g. 4K7) connected to the VBUS of the USB connector. When this input goes high, then it indicates to the FT2232H that it is connected to a host PC. When the host or hub is powered down then the FT2232H is held in SUSPEND mode.

Table 3.2 Common Function pins

Pin No.	Name	Type	Description
63	EECS	I/O	EEPROM – Chip Select. Tri-State during device reset.
62	EECLK	OUTPUT	Clock signal to EEPROM. Tri-State during device reset. When not in reset, this outputs the EEPROM clock.
61	EEDATA	I/O	EEPROM – Data I/O Connect directly to Data-In of the EEPROM and to Data-Out of the EEPROM via a 2.2K resistor. Also, pull Data-Out of the EEPROM to VCC via a 10K resistor for correct operation. Tri-State during device reset.

Table 3.3 EEPROM Interface Group

3.4 Configured Pins

The following sections describe the function of the configurable pins referred to in the table given in Section 3.2 which is determined by how the FT2232H is configured.

3.4.1 FT2232H pins used in an RS232 interface

The FT2232H channel A or channel B can be configured as an RS232 interface. When configured in this mode, the pins used and the descriptions of the signals are shown in Table 3.4.

Channel A Pin No.	Channel B Pin No.	Name	Type	RS232 Configuration Description
16	***38***	TXD	OUTPUT	TXD = transmitter output
17	***39***	RXD	INPUT	RXD = receiver input
18	***40***	RTS#	OUTPUT	RTS# = Ready To send handshake output
19	***41***	CTS#	INPUT	CTS# = Clear To Send handshake input
21	***43***	DTR#	OUTPUT	DTR# = Data Transmit Ready modem signaling line
22	***44***	DSR#	INPUT	DSR# = Data Set Ready modem signaling line
23	***45***	DCD#	INPUT	DCD# = Data Carrier Detect modem signaling line
24	***46***	RI#	INPUT	RI# = Ring Indicator Control Input. When the Remote Wake up option is enabled in the EEPROM, taking RI# low can be used to resume the PC USB Host controller from suspend. (Also see note 1, 2, 3 in section 4.12)
26	***48***	TXDEN	OUTPUT	TXDEN = (TTL level). For use with RS485 level converters.
29	***54***	RXLED#	OUTPUT	RXLED = Receive signaling output when data is transferred from FT2232H to USB Host. Pulses low when receiving data (RXD) via USB. This should be connected to an LED.
30	***55***	TXLED#	OUTPUT	TXLED = Transmit signaling output when data is transferred from USB Host to FT2232H. Pulses low when transmitting data (TXD) via USB. This should be connected to an LED.

Table 3.4 Channel A and Channel B RS232 Configured Pin Descriptions

3.4.2 FT2232H pins used in an FT245 Style Synchronous FIFO Interface

The FT2232H only channel A can be configured as a FT245 style synchronous FIFO interface. When configured in this mode, the pins used and the descriptions of the signals are shown in Table 3.5. To enter this mode the external EEPROM must be set to make port A 245 mode. A software command (Set Bit Mode option) is then sent by the application to the FTDI driver to tell the chip to enter single channel synchronous FIFO mode. In this mode the 'B' channel is not available as all resources have been switched onto channel A. In this mode, data is written or read on the rising edge of the CLKOUT.

Channel A Pin No.	Name	Type	FT245 Configuration Description
24,23,22,21, 19,18,17,16	ADBUS[7:0]	I/O	D7 to D0 bidirectional FIFO data. This bus is normally input unless OE# is low.
26	RXF#	OUTPUT	When high, do not read data from the FIFO. When low, there is data available in the FIFO which can be read by driving RD# low. When in synchronous mode, data is transferred on every clock that RXF# and RD# are both low. Note that the OE# pin must be driven low at least 1 clock period before asserting RD# low.
27	TXE#	OUTPUT	When high, do not write data into the FIFO. When low, data can be written into the FIFO by driving WR# low. When in synchronous mode, data is transferred on every clock that TXE# and WR# are both low.
28	RD#	INPUT	Enables the current FIFO data byte to be driven onto D0...D7 when RD# goes low. The next FIFO data byte (if available) is fetched from the receive FIFO buffer each CLKOUT cycle until RD# goes high.
29	WR#	INPUT	Enables the data byte on the D0...D7 pins to be written into the transmit FIFO buffer when WR# is low. The next FIFO data byte is written to the transmit FIFO buffer each CLKOUT cycle until WR# goes high.
32	CLKOUT	OUTPUT	60 MHz Clock driven from the chip. All signals should be synchronized to this clock.
33	OE#	INPUT	Output enable when low to drive data onto D0-7. This should be driven low at least 1 clock period before driving RD# low to allow for data buffer turn-around.
30	SIWU	INPUT	The Send Immediate / WakeUp signal combines two functions on a single pin. If USB is in suspend mode (PWREN# = 1) and remote wakeup is enabled in the EEPROM , strobing this pin low will cause the device to request a resume on the USB Bus. Normally, this can be used to wake up the Host PC. During normal operation (PWREN# = 0), if this pin is strobed low any data in the device TX buffer will be sent out over USB on the next Bulk-IN request from the drivers regardless of the pending packet size. This can be used to optimize USB transfer speed for some applications. Tie this pin to VCCIO if not used. (Also see note 1, 2, 3 in section 4.12)

Table 3.5 Channel A FT245 Style Synchronous FIFO Configured Pin Descriptions

For a functional description of this mode, please refer to section 4.4

3.4.3 FT2232H pins used in an FT245 Style Asynchronous FIFO Interface

The FT2232H channel A or channel B can be configured as a FT245 asynchronous FIFO interface. When configured in this mode, the pins used and the descriptions of the signals are shown in Table 3.6. To enter this mode the external EEPROM must be set to make port A or B or both 245 mode. In this mode, data is written or read on the falling edge of the RD# or WR# signals.

Channel A Pin No.	Channel B Pin No.	Name	Type	FT245 Configuration Description
24,23,22,21, 19,18,17,16	46,45,44,43, 41,40,39,38	Channel A = ADBUS[7:0] Channel B = BDBUS[7:0]	I/O	D7 to D0 bidirectional FIFO data. This bus is normally input unless RD# is low.
26	48	RXF#	OUTPUT	When high, do not read data from the FIFO. When low, there is data available in the FIFO which can be read by driving RD# low. When RD# goes high again RXF# will always go high and only become low again if there is another byte to read. During reset this signal pin is tri-state, but pulled up to VCCIO via an internal 200kΩ resistor.
27	52	TXE#	OUTPUT	When high, do not write data into the FIFO. When low, data can be written into the FIFO by strobing WR# high, then low. During reset this signal pin is tri-state, but pulled up to VCCIO via an internal 200kΩ resistor.
28	53	RD#	INPUT	Enables the current FIFO data byte to be driven onto D0...D7 when RD# goes low. Fetches the next FIFO data byte (if available) from the receive FIFO buffer when RD# goes high.
29	54	WR#	INPUT	Writes the data byte on the D0...D7 pins into the transmit FIFO buffer when WR# goes from high to low.
30	55	SIWU	INPUT	The Send Immediate / WakeUp signal combines two functions on a single pin. If USB is in suspend mode (PWREN# = 1) and remote wakeup is enabled in the EEPROM , strobing this pin low will cause the device to request a resume on the USB Bus. Normally, this can be used to wake up the Host PC. During normal operation (PWREN# = 0), if this pin is strobed low any data in the device TX buffer will be sent out over USB on the next Bulk-IN request from the drivers regardless of the pending packet size. This can be used to optimize USB transfer speed for some applications. Tie this pin to VCCIO if not used. (Also see note 1, 2, 3 in section 4.12)

Table 3.6 Channel A and Channel B FT245 Style Asynchronous FIFO Configured Pin Descriptions

3.4.4 FT2232H pins used in a Synchronous or Asynchronous Bit-Bang Interface

The FT2232H channel A or channel B can be configured as a synchronous or asynchronous bit-bang interface. Bit-bang mode is a special FTDI FT2232H device mode that changes the 8 IO lines on either (or both) channels into an 8 bit bi-directional data bus. There are two types of bit-bang modes: synchronous and asynchronous.

When configured in any bit-bang mode, the pins used and the descriptions of the signals are shown in **Table 3.7**

Channel A Pin No.	Channel B Pin No.	Name	Type	Configuration Description
24,23,22,21 , 19,18,17,16	**46,45,44,43, 41,40,39,38**	**Channel A = ADBUS[7:0]** **Channel B = BDBUS[7:0]**	I/O	D7 to D0 bidirectional Bit-Bang parallel I/O data pins
27	**52**	**WRSTB#**	OUTPUT	Write strobe, active low output indicates when new data has been written to the I/O pins from the Host PC (via the USB interface).
28	**53**	**RDSTB#**	OUTPUT	Read strobe, this output rising edge indicates when data has been read from the parallel I/O pins and sent to the Host PC (via the USB interface).
30	**55**	**SIWU**	INPUT	The Send Immediate / WakeUp signal combines two functions on a single pin. If USB is in suspend mode (PWREN# = 1) and remote wakeup is enabled in the EEPROM , strobing this pin low will cause the device to request a resume on the USB Bus. Normally, this can be used to wake up the Host PC. During normal operation (PWREN# = 0), if this pin is strobed low any data in the device TX buffer will be sent out over USB on the next Bulk-IN request from the drivers regardless of the pending packet size. This can be used to optimize USB transfer speed for some applications. Tie this pin to VCCIO if not used. (Also see note 1, 2, 3 in section 4.12)

Table 3.7 Channel A and Channel B Synchronous or Asynchronous Bit-Bang Configured Pin Descriptions

For a functional description of this mode, please refer to section 4.10 Synchronous and Asynchronous Bit-Bang Interface Mode Description.

3.4.5 FT2232H pins used in an MPSSE

The FT2232H channel A and channel B each have a Multi-Protocol Synchronous Serial Engine (MPSSE). Each MPSSE can be independently configured to a number of industry standard serial interface protocols such as JTAG, I2C or SPI, or it can be used to implement a proprietary bus protocol. For example, it is possible to use one of the FT2232H's channels to connect to an SRAM configurable FPGA such as supplied by Altera or Xilinx. The FPGA device would normally be un-configured (i.e. have no defined function) at power-up. Application software on the PC could use the MPSSE to download configuration data to the FPGA over USB. This data would define the hardware function on power up. The other FT2232H channel would be available for another function. Alternatively each MPSSE can be used to control a number of GPIO pins. When configured in this mode, the pins used and the descriptions of the signals are shown Table 3.6

Channel A Pin No.	Channel B Pin No.	Name	Type	MPSSE Configuration Description
16	38	TCK/SK	OUTPUT	Clock Signal Output. For example: JTAG – TCK, Test interface clock SPI – SK, Serial Clock
17	39	TDI/DO	OUTPUT	Serial Data Output. For example: JTAG – TDI, Test Data Input SPI – DO
18	40	TDO/DI	INPUT	Serial Data Input. For example: JTAG – TDO, Test Data output SPI – DI, Serial Data Input
19	41	TMS/CS	OUTPUT	Output Signal Select. For example: JTAG – TMS, Test Mode Select SPI – CS, Serial Chip Select
21	43	GPIOL0	I/O	General Purpose input/output
22	44	GPIOL1	I/O	General Purpose input/output
23	45	GPIOL2	I/O	General Purpose input/output
24	46	GPIOL3	I/O	General Purpose input/output
26	48	GPIOH0	I/O	General Purpose input/output
27	52	GPIOH1	I/O	General Purpose input/output
28	53	GPIOH2	I/O	General Purpose input/output
29	54	GPIOH3	I/O	General Purpose input/output
30	55	GPIOH4	I/O	General Purpose input/output
32	57	GPIOH5	I/O	General Purpose input/output
33	58	GPIOH6	I/O	General Purpose input/output
34	59	GPIOH7	I/O	General Purpose input/output

Table 3.8 Channel A and Channel B MPSSE Configured Pin Descriptions

For a functional description of this mode, please refer to section 4.6 MPSSE Interface Mode Description.

3.4.6 FT2232H Pins used as a Fast Serial Interface

The FT2232H channel B can be configured for use with high-speed optical bi-directional isolated serial data transfer: Fast Serial Interface. (Not available on channel A). A proprietary FTDI protocol designed to allow galvanic isolated devices to communicate synchronously with the FT2232H using just 4 signal wires (over two dual opto-isolators), and two power lines. The peripheral circuitry controls the data transfer rate in both directions, whilst maintaining full data integrity. Maximum USB full speed data rates can be achieved. Both 'A' and 'B' channels can communicate over the same 4 wire interface if desired.

When configured in this mode, the pins used and the descriptions of the signals are shown in **Table 3.9**.

Channel B Pin No.	Name	Type	Fast Serial Interface Configuration Description
38	FSDI	INPUT	Fast serial data input.
39	FSCLK	INPUT	Fast serial clock input. Clock input to FT2232H chip to clock data in or out.
40	FSDO	OUTPUT	Fast serial data output.
41	FSCTS	OUTPUT	Fast serial Clear To Send signal output. Driven low to indicate that the chip is ready to send data

Table 3.9 Channel B Fast Serial Interface Configured Pin Descriptions

For a functional description of this mode, please refer to section 4.8 Fast Opto-Isolated Serial Interface Mode Description

3.4.7 FT2232H Pins Configured as a CPU-style FIFO Interface

The FT2232H channel A or channel B can be configured in a CPU-style FIFO interface mode which allows a CPU to interface to USB via the FT2232H. This mode is enabled in the external EEPROM.

When configured in this mode, the pins used and the descriptions of the signals are shown in **Table 3.10**

Channel A Pin No.	Channel B Pin No.	Name	Type	Fast Serial Interface Configuration Description
24,23,22,21 **,** ***19,18,17,16***	**46,45,44,43 , 41,40,39,38**	**Channel A = ADBUS[7:0]** **Channel B = BDBUS[7:0]**	I/O	D7 to D0 bidirectional data bus
26	48	CS#	INPUT	Active low chip select input
27	52	A0	INPUT	Address bit A0
28	53	RD#	INPUT	Active Low FIFO Read input
29	54	WR#	INPUT	Active Low FIFO Write input

Table 3.10 Channel A and Channel B CPU-style FIFO Interface Configured Pin Descriptions

For a functional description of this mode, please refer to section 4.9 CPU-style FIFO Interface Mode Description

3.4.8 FT2232H Pins Configured as a Host Bus Emulation Interface

The FT2232H can be used to combine channel A and channel B to be configured as a host bus emulation interface mode which emulates a standard 8048 or 8051 MCU host.

When configured in this mode, the pins used and the descriptions of the signals are shown in **Table 3.11**

Pin No.	Name	Type	Fast Serial Interface Configuration Description
24,23,22,21, 19,18,17,16	ADBUS[7:0]	I/O	Multiplexed bidirectional Address/Data bus AD7 to AD0
34,33,32,30, 29,28,27,26	A[15:8]	OUTPUT	Extended Address A15 to A8
38	CS#	OUTPUT	Active low chip select device during Read or Write.
39	ALE	OUTPUT	Positive pulse to latch the address
40	RD#	OUTPUT	Active low read output.
41	WR#	OUTPUT	Active low write output. (Data is setup before WR# goes low, and is held after WR# goes high)
43	IORDY	INPUT	Extends the time taken to perform a Read or Write operation if driven low. Pull up to VCORE if not being used.
44	CLKOUT	OUTPUT	Master clock. Outputs the clock signal being used by the configured interface.
45	I/O0	I/O	MPSSE mode instructions to set / clear or read the high byte of data can be used with this pin. Please refer to Application Note **AN_108** for operation of these instructions.
46	I/O1	I/O	MPSSE mode instructions to set / clear or read the high byte of data can be used with this pin. In addition this pin has instructions which will make the controller wait until it is high, or wait until it is low. This can be used to connect to an IRQ pin of a peripheral chip. The FT2232H will wait for the interrupt, and then read the device, and pass the answer back to the host PC. I/O1 must be held in input mode if this option is used. Please refer to Application Note **AN_108** for operation of these instructions.

Table 3.11 Channel A and Channel B Host Bus Emulation Interface Configured Pin Descriptions

For a functional description of this mode, please refer to section 4.7 MCU Host Bus Emulation Mode

4 Function Description

The FT2232H USB 2.0 High Speed (480Mb/s) to UART/FIFO is one of FTDI's 5th generation of Ics. It has the capability of being configured in a variety of industry standard serial or parallel interfaces.

The FT2232H has two independent configurable interfaces. Each interface can be configured as UART, FIFO, JTAG, SPI, I2C or bit-bang mode with independent baud rate generators. In addition to these, the FT2232H supports a host bus emulation mode, a CPU-Style FIFO mode and a fast opto-isolated serial interface mode.

4.1 Key Features

USB High Speed to Dual Interface. The FT2232H is a USB 2.0 High Speed (480Mbits/s) to dual independent flexible and configurable parallel/serial interfaces.

Functional Integration. The FT2232H integrates a USB protocol engine which controls the physical Universal Transceiver Macrocell Interface (UTMI) and handles all aspects of the USB 2.0 High Speed interface. The FT222H includes an integrated +1.8V Low Drop-Out (LDO) regulator and 12MHz to 480MHz PLL. It also includes 4kbytes Tx and Rx data buffers per interface. The FT2232H effectively integrates the entire USB protocol on a chip with no firmware required.

MPSSE.Multi-Purpose Synchronous Serial Engines (MPSSE), capable of speeds up to 30 Mbits/s, provides flexible synchronous interface configurations.

Data Transfer rate. The FT2232H supports a data transfer rate up to 12 Mbaud when configured as an RS232/RS422/RS485 UART interface or greater than 25 Mbytes/second over a synchronous parallel FIFO interface. Please note the FT2232H does not support the baud rates of 7 Mbaud 9 Mbaud, 10 Mbaud and 11 Mbaud.

Latency Timer. This is really a feature of the driver and is used to as a timeout to flush short packets of data back to the PC. The default is 16ms, but it can be altered between 0ms and 255ms. At 0ms latency you get a packet transfer on every high speed microframe.

4.2 Functional Block Descriptions

Dual Multi-Purpose UART/FIFO Controllers. The FT2232H has two independent UART/FIFO Controllers. These control the UART data, 245 fifo data, opto isolation (Fast Serial) or control the Bit-Bang mode if selected by SETUP command. Each Multi-Purpose UART/FIFO Controller also contain an MPSSE (Multi Protocol Synchronous Serial Engine) which can be used independently of each other. Using this MPSSE, the Multi-Purpose UART/FIFO Controller can be configured, under software command, to have 1 MPSSE + 1 UART / 245 FIFO (each UART / 245 can be set to Bit Bang mode to gain extra I/O if required) or 2 MPSSE.

USB Protocol Engine and FIFO control. The USB Protocol Engine controls and manages the interface between the UTMI PHY and the FIFOs of the chip. It also handles power management and the USB protocol specification.

Dual Port FIFO TX Buffer (4Kbytes per interface). Data from the Host PC is stored in these buffers to be used by the Multi-purpose UART/FIFO controllers. This is controlled by the USB Protocol Engine and FIFO control block.

Dual Port FIFO RX Buffer (4Kbytes per interface). Data from the Multi-purpose UART/FIFO controllers is stored in these blocks to be sent back to the the Host PC when requested. This is controlled by the USB Protocol Engine and FIFO control block.

RESET Generator – The integrated Reset Generator Cell provides a reliable power-on reset to the device internal circuitry at power up. The RESET# input pin allows an external device to reset the FT2232H. RESET# should be tied to VCCIO (+3.3v) if not being used.

Independent Baud Rate Generators – The Baud Rate Generators provides a x16 or a x10 clock input to the UART's from a 120MHz reference clock and consists of a 14 bit pre-scaler and 4 register bits which

provide fine tuning of the baud rate (used to divide by a number plus a fraction). This determines the Baud Rate of the UART which is programmable from 183 baud to 12 million baud. The FT2232H does not support the baud rates of 7 Mbaud 9 Mbaud, 10 Mbaud and 11 Mbaud.

See FTDI application note AN232B-05 on the FTDI website (www.ftdichip.com) for more details.

+1.8V LDO Regulator. The +1.8V LDO regulator generates the +1.8 volts for the core and the USB transceiver cell. Its input (VREGIN) must be connected to a +3.3V external power source. It is also recommended to add an external filtering capacitor to the VREGIN. There is no direct connection from the +1.8V output (VREGOUT) and the internal functions of the FT2232H. The PCB must be routed to connect VREGOUT to the pins that require the +1.8V including VREGIN.

UTMI PHY. The Universal Transceiver Macrocell Interface (UTMI) physical interface cell. This block handles the Full speed / High Speed SERDES (serialise – deserialise) function for the USB TX/RX data. It also provides the clocks for the rest of the chip. A 12 MHz crystal should be connected to the OSCI and OSCO pins. A 12K Ohm resistor should be connected between REF and GND on the PCB.

The UTMI PHY functions include:

- Supports 480 Mbit/s "High Speed" (HS)/ 12 Mbit/s "Full Speed" (FS), FS Only and "Low Speed" (LS)
- SYNC/EOP generation and checking
- Data and clock recovery from serial stream on the USB.
- Bit-stuffing/unstuffing; bit stuff error detection.
- Manages USB Resume, Wake Up and Suspend functions.
- Single parallel data clock output with on-chip PLL to generate higher speed serial data clocks.

EEPROM Interface. When used without an external EEPROM the FT2232H defaults to a USB to dual asynchronous serial port device. Adding an external 93C46 (93C56 or 93C66) EEPROM allows each of the chip's channels to be independently configured as a serial UART (RS232 mode), parallel FIFO (245) mode or fast serial (opto isolation). The external EEPROM can also be used to customise the USB VID, PID, Serial Number, Product Description Strings and Power Descriptor value of the FT2232H for OEM applications. Other parameters controlled by the EEPROM include Remote Wake Up, Soft Pull Down on Power-Off and I/O pin drive strength.

The EEPROM should be a 16 bit wide configuration such as a Microchip 93LC46B or equivalent capable of a 1Mbit/s clock rate at VCC = +3.00V to 3.6V. The EEPROM is programmable in-circuit over USB using a utility program called MPROG available from FTDI's web site (**www.ftdichip.com**). This allows a blank part to be soldered onto the PCB and programmed as part of the manufacturing and test process.

If no EEPROM is connected (or the EEPROM is blank), the FT2232H will default to dual serial ports. The device uses its built-in default VID (0403) , PID (6010) Product Description and Power Descriptor Value. In this case, the device will not have a serial number as part of the USB descriptor.

4.3 Dual Port FT232 UART Interface Mode Description

The FT2232H can be configured in similar UART modes as the FTDI FT232 devices. The following examples illustrate how to configure the FT2232H with an RS232, RS422 or RS485 interface. The FT2232 can be configured as a mixture of these interfaces.

4.3.1 Dual Port RS232 Configuration

Figure 4.1 illustrates how the FT2232H can be configured with an RS232 UART interface. This can be repeated for channel B to provide a dual RS232, but has been omitted for clarity.

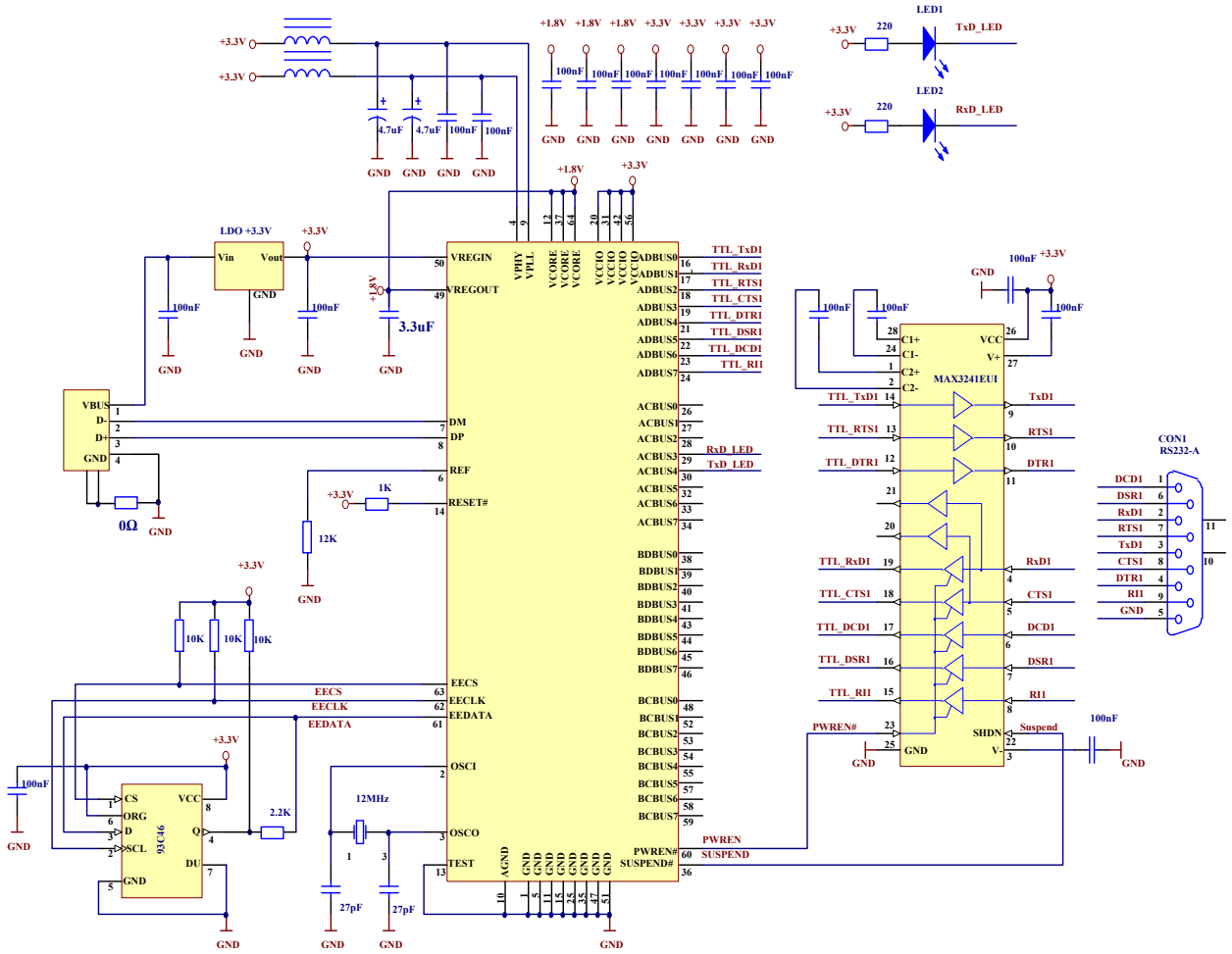

Figure 4.1 RS232 Configuration

4.3.2 Dual Port RS422 Configuration

Figure 4.2 illustrates how the FT2232H can be configured as a dual RS422 interface.

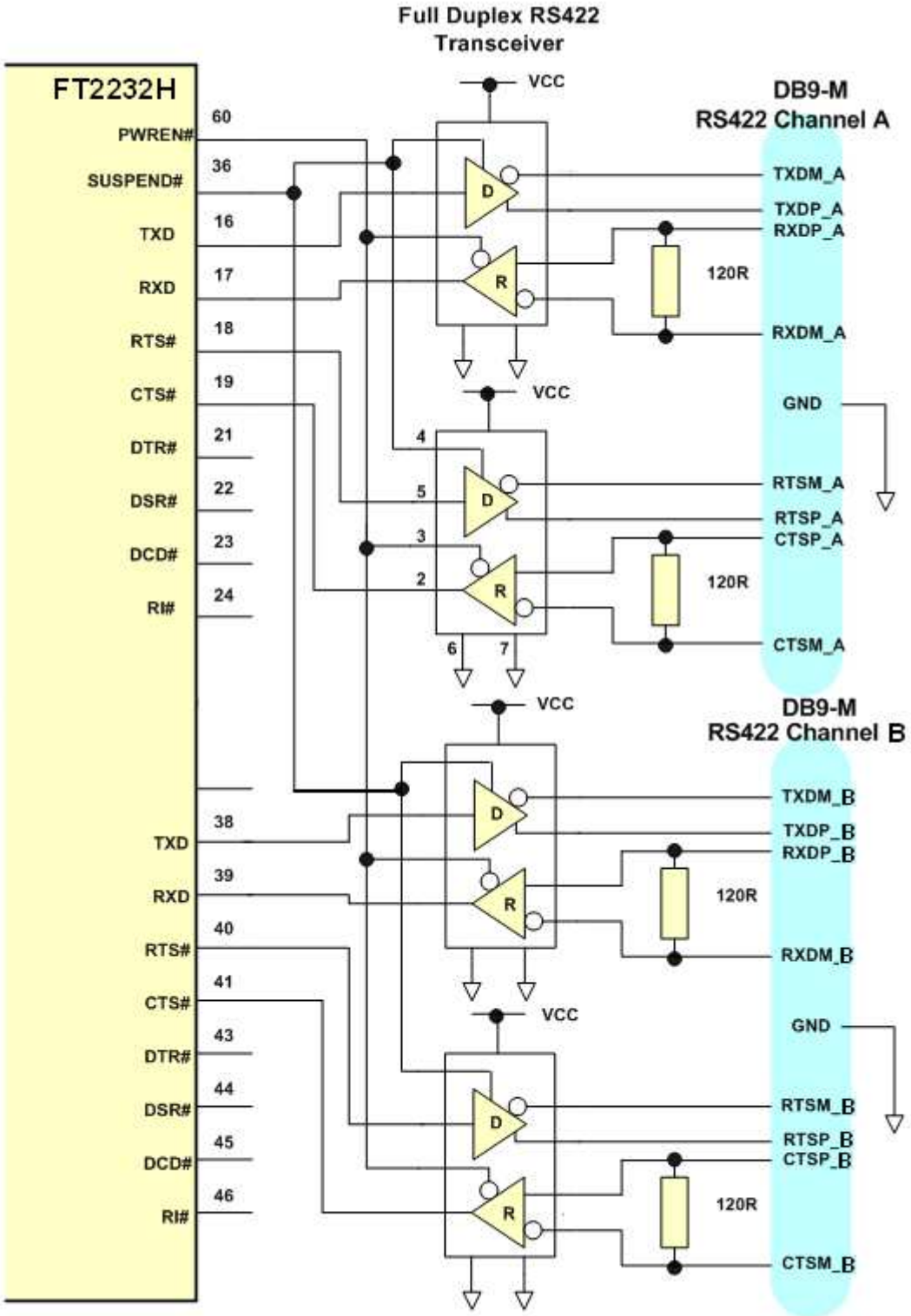

Figure 4.2 Dual RS422 Configuration

In this case both channel A and channel B are configured as UART operating at TTL levels and a level converter device (full duplex RS485 transceiver) is used to convert the TTL level signals from the

FT2232H to RS422 levels. The PWREN# signal is used to power down the level shifters such that they operate in a low quiescent current when the USB interface is in suspend mode.

4.3.3 Dual Port RS485 Configuration

Figure 4.3 illustrates how the FT2232H can be configured as a dual RS485 interface.

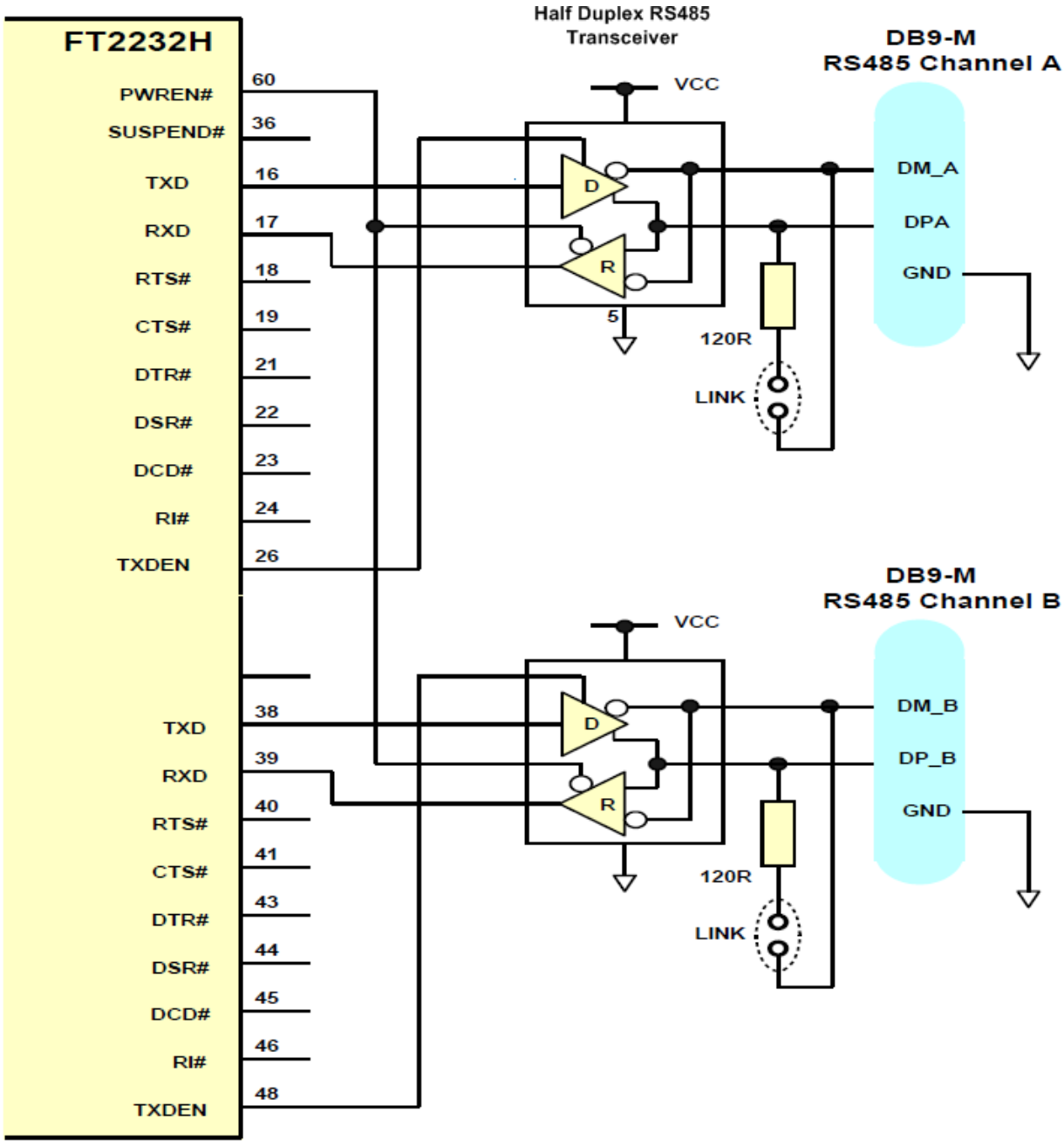

Figure 4.3 Dual RS485 Configuration

In this case both channel A and channel B are configured as RS485 operating at TTL levels and a level converter device (half duplex RS485 transceiver) is used to convert the TTL level signals from the FT232H to RS485 levels. It has separate enables on both the transmitter and receiver. With RS485, the transmitter is only enabled when a character is being transmitted from the UART. The TXDEN pins on the FT2232H are provided for exactly that purpose, and so the transmitter enables are wired to the TXDEN's. The receiver enable is active low, so it is wired to the PWREN# pin to disable the receiver when in USB suspend mode.