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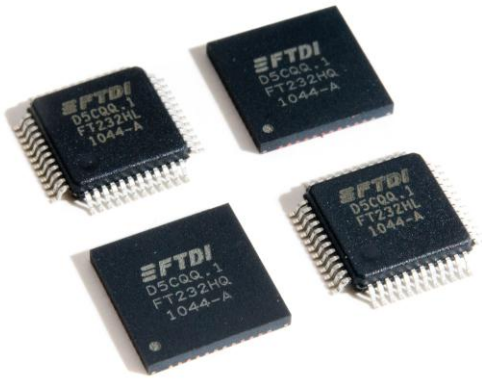
Future Technology Devices International Ltd

FT232H Single Channel Hi-Speed USB to Multipurpose UART/FIFO IC



The FT232H is a single channel USB 2.0 Hi-Speed (480Mb/s) to UART/FIFO IC. It has the capability of being configured in a variety of industry standard serial or parallel interfaces. The FT232H has the following advanced features:

- Single channel USB to serial / parallel ports with a variety of configurations.
- Entire USB protocol handled on the chip. No USB specific firmware programming required.
- USB 2.0 Hi-Speed (480Mbits/Second) and Full Speed (12Mbits/Second) compatible.
- Multi-Protocol Synchronous Serial Engine (MPSSE) to simplify synchronous serial protocol (USB to JTAG, I^2C, SPI (MASTER) or bit-bang) design.
- UART transfer data rate up to 12Mbaud. (RS232 Data Rate limited by external level shifter).
- USB to asynchronous 245 FIFO mode for transfer data rate up to 8 Mbyte/Sec.
- USB to synchronous 245 parallel FIFO mode for transfers upto 40 Mbytes/Sec
- Supports a proprietary half duplex FT1248 interface with a configurable width, bi-directional data bus (1, 2, 4 or 8 bits wide).
- CPU-style FIFO interface mode simplifies CPU interface design.
- Fast serial interface option.
- FTDI's royalty-free Virtual Com Port (VCP) and Direct (D2XX) drivers eliminate the requirement for USB driver development in most cases.
- Adjustable receive buffer timeout.
- Option for transmit and receive LED drive signals.
- Bit-bang Mode interface option with RD# and WR# strobes
- Highly integrated design includes 5V to 3.3/+1.8V LDO regulator for VCORE, integrated POR function
- Asynchronous serial UART interface option with full hardware handshaking and modem interface signals.
- Fully assisted hardware or X-On / X-Off software handshaking.
- UART Interface supports 7/8 bit data, 1/2 stop bits, and Odd/Even/Mark/Space/No Parity.
- Auto transmit enable control for RS485 serial applications using the TXDEN pin.
- Operational mode configuration and USB Description strings configurable in external EEPROM over the USB interface.
- Configurable I/O drives strength (4, 8, 12 or 16mA) and slew rate.
- Low operating and USB suspend current.
- Supports self powered, bus powered and high-power bus powered USB configurations.
- UHCI/OHCI/EHCI host controller compatible.
- USB Bulk data transfer mode (512 byte packets in Hi-Speed mode).
- +1.8V (chip core) and +3.3V I/O interfacing (+5V Tolerant).
- Extended -40°C to 85°C industrial operating temperature range.
- Compact 48-pin Lead Free LQFP or QFN package
- Configurable ACBUS I/O pins.

1 Typical Applications

- Single chip USB to UART (RS232, RS422 or RS485)
- USB to FIFO
- USB to FT1248
- USB to JTAG
- USB to SPI
- USB to I^2C
- USB to Bit-Bang
- USB to Fast Serial Interface
- USB to CPU target interface (as memory)
- USB Instrumentation
- USB Industrial Control
- USB EPOS Control
- USB MP3 Player Interface
- USB FLASH Card Reader / Writers
- Set Top Box - USB interface
- USB Digital Camera Interface
- USB Bar Code Readers

1.1 Driver Support

The FT232H requires USB device drivers (listed below), available free from **http://www.ftdichip.com**, to operate. The VCP version of the driver creates a Virtual COM Port allowing legacy serial port applications to operate over USB e.g. serial emulator application TTY. Another FTDI USB driver, the D2XX driver, can also be used with application software to directly access the FT232H through a DLL.

Royalty free VIRTUAL COM PORT (VCP) DRIVERS for...

- Windows 8 and Windows 8 64-bit
- Windows 7 and Windows 7 64-bit
- Windows Vista and Vista 64-bit
- Windows XP and XP 64-bit
- Windows XP Embedded
- Windows 2000, Server 2003, Server 2008
- Windows CE 4.2, 5.0, 5.2 and 6.0
- Mac OS-X
- Linux (2.6.39 or later)

Royalty free D2XX *Direct* Drivers (USB Drivers + DLL S/W Interface)

- Windows 8 and Windows 8 64-bit
- Windows 7 and Windows 7 64-bit
- Windows Vista and Vista 64-bit
- Windows XP and XP 64-bit
- Windows XP Embedded
- Windows 2000, Server 2003, Server 2008
- Windows CE 4.2, 5.0, 5.2 and 6.0
- Mac OS-X
- Linux (2.6.32 or later)

1.2 Part Numbers

Part Number	Package
FT232HL -xxxx	48 Pin LQFP
FT232HQ-xxxx	48 Pin QFN

Note: Packaging codes for xxxx is:

- Reel: Taped and Reel (LQFP = 1500 pieces per reel, QFN = 3000 pieces per reel)

-Tray: Tray packing, (LQFP = 250 pieces per tray, QFN =260 pieces per tray)

Please refer to section 8 for all package mechanical parameters.

1.3 USB Compliant

The FT232H is fully compliant with the USB 2.0 specification and has been given the USB-IF Test-ID (TID) 40770005.

The timing of the rise/fall time of the USB signals is not only dependant on the USB signal drivers, it is also dependant system and is affected by factors such as PCB layout, external components and any transient protection present on the USB signals. For USB compliance these may require a slight adjustment. This timing can be modified through a programmable setting stored in the same external EEPROM that is used for the USB descriptors. Timing can also be changed by adding appropriate passive components to the USB signals.

1.4 Applicable Documents

The following application and technical documents can be downloaded by clicking on the appropriate links below:

AN_108 – Command Processor For MPSSE and MCU Host Bus Emulation Modes

AN_113 – Interfacing FT2232H Hi-Speed Devices To I2C Bus

AN_114 – Interfacing FT2232H Hi-Speed Devices To SPI Bus

AN_129 – Interfacing FT2232H Hi-Speed Devices to a JTAG TAP

AN_135 – MPSSE Basics

AN_167_FT1248 Parallel Serial Interface Basics

2 FT232H Block Diagram

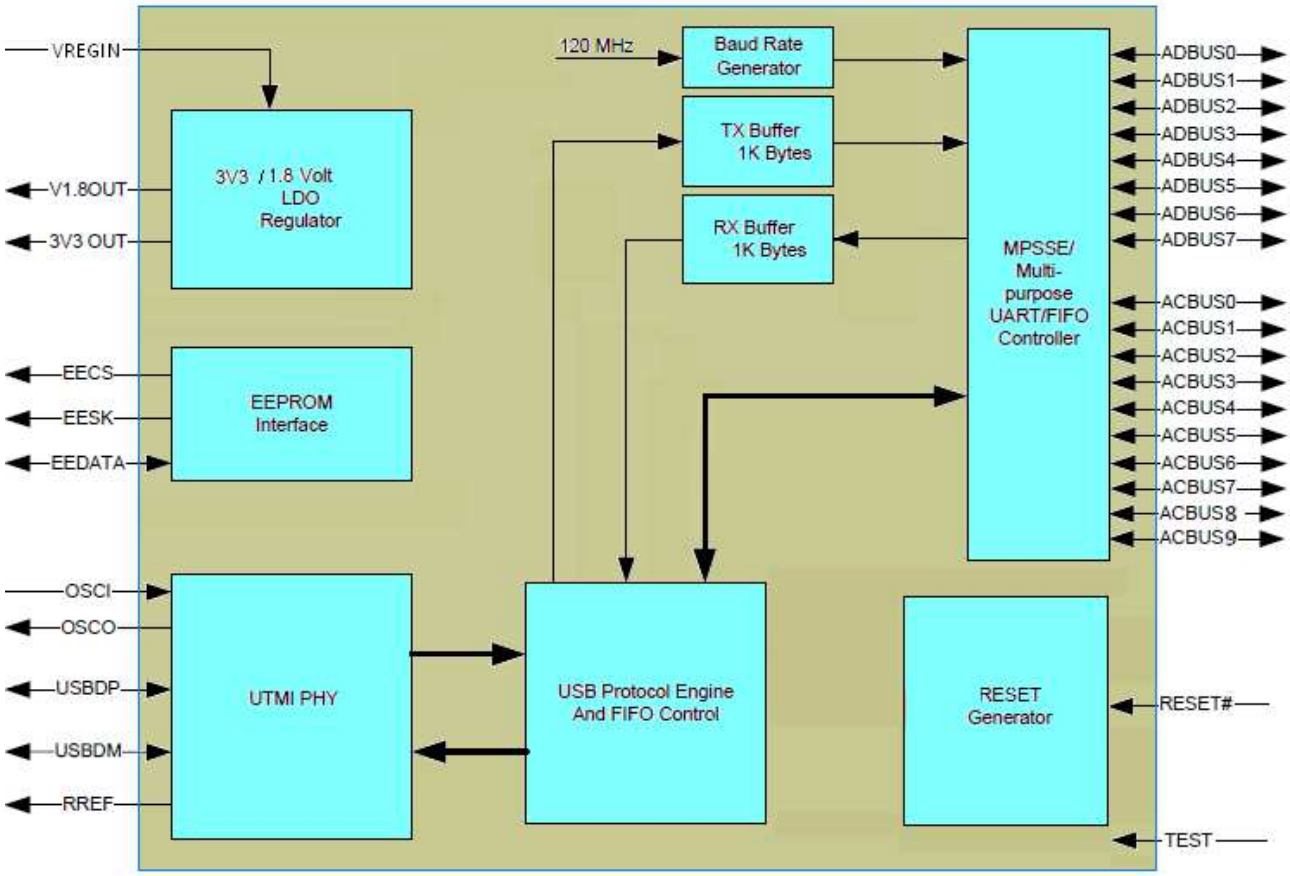


Figure 2.1 FT232H Block Diagram

A full description of each function is available in section 4.

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3 Device Pin Out And Signal Descriptions

The 48-pin LQFP and 48-pin QFN have the same pin numbering for specific functions. This pin numbering is illustrated in the schematic symbol shown in Figure 3.1

3.1 Schematic Symbol

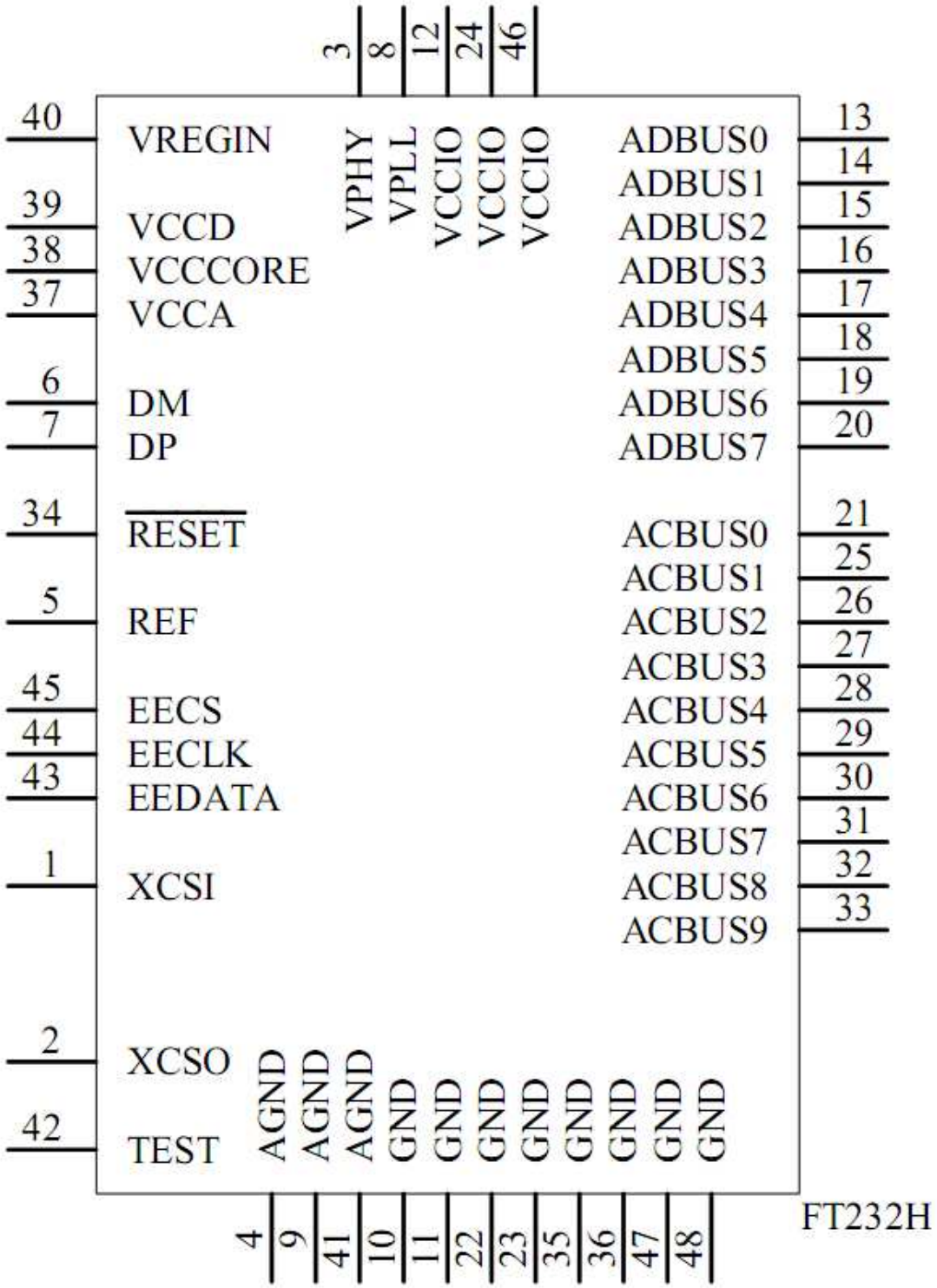

Figure 3.1 FT232H Schematic Symbol

3.2 FT232H Pin Descriptions

This section describes the operation of the FT232H pins. Both the LQFP and the QFN packages have the same function on each pin. The function of many pins is determined by the configuration of the FT232H. The following table details the function of each pin dependent on the configuration of the interface. Each of the functions is described in the following table (Note: The convention used throughout this document for active low signals is the signal name followed by #).

Pins marked * are EEPROM selectable

FT232H										
Pin		**Pin functions (depends on configuration)**								
Pin #	Pin Name	ASYNC Serial (RS232)	SYNC 245 FIFO	STYLE ASYNC 245 FIFO	ASYNC Bit-bang	SYNC Bit-bang	MPSSE	Fast Serial interface	CPU Style FIFO	FT1248
13	ADBUS0	TXD	D0	D0	D0	D0	TCK/SK	FSDI	D0	MIOSI0
14	ADBUS1	RXD	D1	D1	D1	D1	TDI/DO	FSCLK	D1	MIOSI1
15	ADBUS2	RTS#	D2	D2	D2	D2	TDO/DI	FSDO	D2	MIOSI2
16	ADBUS3	CTS#	D3	D3	D3	D3	TMS/CS	FSCTS	D3	MIOSI3
17	ADBUS4	DTR#	D4	D4	D4	D4	GPIOL0	** TriSt-UP	D4	MIOSI4
18	ADBUS5	DSR#	D5	D5	D5	D5	GPIOL1	** TriSt-UP	D5	MIOSI5
19	ADBUS6	DCD#	D6	D6	D6	D6	GPIOL2	** TriSt-UP	D6	MIOSI6
20	ADBUS7	RI#	D7	D7	D7	D7	GPIOL3	** TriSt-UP	D7	MIOSI7
21	ACBUS0	* TXDEN	RXF#	RXF#	ACBUS0	ACBUS0	GPIOH0	** ACBUS0	CS#	SCLK
25	ACBUS1	** ACBUS1	TXE#	TXE#	WRSTB#	WRSTB#	GPIOH1	** ACBUS1	A0	SS_n
26	ACBUS2	** ACBUS2	RD#	RD#	RDSTB#	RDSTB#	GPIOH2	** ACBUS2	RD#	MISO
27	ACBUS3	* RXLED#	WR#	WR#	ACBUS3	ACBUS3	GPIOH3	** ACBUS3	WR#	ACBUS3
28	ACBUS4	* TXLED#	SIWU#	SIWU#	SIWU#	SIWU#	GPIOH4	SIWU#	SIWU#	ACBUS4
29	ACBUS5	** ACBUS5	CLKOUT	ACBUS5	** ACBUS5	** ACBUS5	GPIOH5	** ACBUS5	** ACBUS5	ACBUS5
30	ACBUS6	** ACBUS6	OE#	ACBUS6	ACBUS6	ACBUS6	GPIOH6	** ACBUS6	** ACBUS6	ACBUS6
31	ACBUS7	PWRSAV#	PWRSAV#	PWRSAV#	PWRSAV#	PWRSAV#	*** GPIOH7	PWRSAV#	PWRSAV#	PWRSAV#
32	ACBUS8	** ACBUS8	** ACBUS8	** ACBUS8	** ACBUS8	** ACBUS8	** ACBUS8	** ACBUS8	** ACBUS8	ACBUS8
33	ACBUS9	** ACBUS9	** ACBUS9	** ACBUS9	** ACBUS9	** ACBUS9	** ACBUS9	** ACBUS9	** ACBUS9	ACBUS9

Pins marked ** default to tri-stated inputs with an internal 75KΩ (approx) pull up resistor to VCCIO.

Pin marked *** default to GPIO line with an internal 75KΩ pull down resistor to GND. Using the EEPROM this pin can be enabled USBVCC mode instead of GPIO mode.

3.3 Signal Description

The operation of the following FT232H pins are the same regardless of the configured mode:-

Pin No.	Name	Type	Description
40	** VREGIN	POWER input	+5.0V or 3V3 power supply input.
37	VCCA	POWER output	+1.8V output. Should not be used.
38	VCORE	POWER output	+1.8V output. Should not be used.
39	** VCCD	POWER output or input	+3.3V output or input.
12, 24, 46	VCCIO	POWER input	+3.3V input. I/O interface power supply input
8	VPLL	POWER Input	+3.3V input. Internal PLL power supply input. It is recommended that this supply is filtered using an LC filter. (See figure 6.1)
3	VPHY	POWER Input	+3.3V input. Internal USB PHY power supply input. Note that this cannot be connected directly to the USB supply. A +3.3V regulator must be used. It is recommended that this supply is filtered using an LC filter.(See figure 6.1)
4,9,41	AGND	POWER Input	0V Ground input.
10,11,22,23,35,36,47,48	GND	POWER Input	0V Ground input.

Table 3.1 Power and Ground

** If pin 40 (VREGIN) is +5.0V, pin 39 becomes an output and If pin 40 (VREGIN) is 3V3 pin 39 becomes an input.

Pin No.	Name	Type	Description
1	OSCI	INPUT	Oscillator input.
2	OSCO	OUTPUT	Oscillator output.
5	REF	INPUT	Current reference – connect via a 12KΩ resistor @ 1% to GND.
6	DM	INPUT	USB Data Signal Minus.
7	DP	INPUT	USB Data Signal Plus.
42	TEST	INPUT	IC test pin – for normal operation must be connected to GND.
34	RESET#	INPUT	Reset input (active low).
31	PWRSAV#	INPUT	USB Power Save input. This is an EEPROM configurable option which is set using a 'Suspend on DBus7 Low' bit on FT_PROG . This option is available when the FT232H is on a self powered mode and is used to prevent forcing current down the USB lines when the host or hub is powered off. PWRSAV# = 1 : Normal Operation PWRSAV# = 0 : FT232H forced into SUSPEND mode. PWRSAV# can be connected to VBUS of the USB connector (via a 39KΩ resistor). When this input goes high, then it indicates to the FT232H that it is connected to a host PC. When the host or hub is powered down then the FT232H is held in SUSPEND mode.

Table 3.2 Common Function pins

Pin No.	Name	Type	Description
45	EECS	I/O	EEPROM – Chip Select. Tri-State during device reset.
44	EECLK	OUTPUT	Clock signal to EEPROM. Tri-State during device reset. When not in reset, this outputs the EEPROM clock.
43	EEDATA	I/O	EEPROM – Data I/O. Connect directly to Data-in of the EEPROM and to Data-out of the EEPROM via a 2.2K resistor. Also, pull Data-Out of the EEPROM to VCCD via a 10K resistor for correct operation. Tri-State during device reset.

Table 3.3 EEPROM Interface Group

Pin No.	Name	Type	Description
13	ADBUS0	Output	Configurable Output Pin, the default configuration is Transmit Asynchronous Data Output.
14	ADBUS1	Input	Configurable Input Pin, the default configuration is Receiving Asynchronous Data Input.
15	ADBUS2	Output	Configurable Output Pin, the default configuration is Request to Send Control Output / Handshake Signal.
16	ADBUS3	Input	Configurable Input Pin, the default configuration is Clear To Send Control Input / Handshake Signal.
17	ADBUS4	Output	Configurable Output Pin, the default configuration is Data Terminal Ready Control Output / Handshake Signal.
18	ADBUS5	Input	Configurable Input Pin, the default configuration is Data Set Ready Control Input / Handshake Signal.
19	ADBUS6	Input	Configurable Input Pin, the default configuration is Data Carrier Detect Control Input.
20	ADBUS7	Input	Configurable Input Pin, the default configuration is Ring Indicator Control Input. When remote wake up is enabled in the EEPROM taking RI# low can be used to resume the PC USB host controller from suspend. (Also see note 1, 2, 3 in section 4.12)
21	ACBUS0	I/O	Configurable ACBUS I/O Pin. Function of this pin is configured in the device EEPROM. If the external EEPROM is not fitted the default configuration is TriSt-PU. See ACBUS Signal Options, Table 3.5.
25	ACBUS1	I/O	Configurable ACBUS I/O Pin. Function of this pin is configured in the device EEPROM. If the external EEPROM is not fitted the default configuration is TriSt-PU. See ACBUS Signal Options, Table 3.5.
26	ACBUS2	I/O	Configurable ACBUS I/O Pin. Function of this pin is configured in the device EEPROM. If the external EEPROM is not fitted the default configuration is TriSt-PU. See ACBUS Signal Options, Table 3.5.
27	ACBUS3	I/O	Configurable ACBUS I/O Pin. Function of this pin is configured in the device EEPROM. If the external EEPROM is not fitted the default configuration is TriSt-PU. See ACBUS Signal Options, Table 3.5.
28	ACBUS4	I/O	Configurable ACBUS I/O Pin. Function of this pin is configured in the device EEPROM. If the external EEPROM is not fitted the default configuration is TriSt-PU. See ACBUS Signal Options, Table 3.5.
29	ACBUS5	I/O	Configurable ACBUS I/O Pin. Function of this pin is configured in the device EEPROM. If the external EEPROM is not fitted the default configuration is TriSt-PU. See ACBUS Signal Options, Table 3.5.

30	ACBUS6	I/O	Configurable ACBUS I/O Pin. Function of this pin is configured in the device EEPROM. If the external EEPROM is not fitted the default configuration is TriSt-PU. See ACBUS Signal Options, Table 3.5.
31	ACBUS7	I/O	Configurable ACBUS I/O Pin. Function of this pin is configured in the device EEPROM. If the external EEPROM is not fitted the default configuration is TriSt-PD. See ACBUS Signal Options, Table 3.5.
32	ACBUS8	I/O	Configurable ACBUS I/O Pin. Function of this pin is configured in the device EEPROM. If the external EEPROM is not fitted the default configuration is TriSt-PU. See ACBUS Signal Options, Table 3.5.
33	ACBUS9	I/O	Configurable ACBUS I/O Pin. Function of this pin is configured in the device EEPROM. If the external EEPROM is not fitted the default configuration is TriSt-PU. See ACBUS Signal Options, Table 3.5.

Table 3.4 UART Interface and ACBUS Group (see note 1)

Notes:
1. When used in Input Mode, the input pins are pulled to VCCIO via internal 75kΩ (approx) resistors. These pins can be programmed to gently pull low during USB suspend (PWREN# = "1") by setting an option in the EEPROM.

3.4 ACBUS Signal Option

If the external EEPROM is fitted, the following options can be configured on the CBUS I/O pins using the software utility FT_PROG which can be downloaded from the FTDI utilities page. CBUS signal options are common to both package versions of the FT232H. The default configuration is described in section 7.

ACBUS Signal Option	Available On ACBUS Pin	Description
TXDEN	ACBUS0, ACBUS1, ACBUS2, ACBUS3, ACBUS4, ACBUS5, ACBUS6, ACBUS8, ACBUS9	TXDEN = (TTL level). Used with RS485 level converters to enable the line driver during data transmit. TXDEN is active from one bit time before the start bit is transmitted on TXD until the end of the stop bit.
*PWREN#	ACBUS0, ACBUS1, ACBUS2, ACBUS3, ACBUS4, ACBUS5, ACBUS6, ACBUS8, ACBUS9	Output is low after the device has been configured by USB, then high during USB suspend mode. This output can be used to control power to external logic P-Channel logic level MOSFET switch. Enable the interface pull-down option when using the PWREN# in this way.*
TXLED#	ACBUS0, ACBUS1, ACBUS2, ACBUS3, ACBUS4, ACBUS5, ACBUS6, ACBUS8, ACBUS9	TXLED = Transmit signalling output. Pulses low when transmitting data (TXD) to the external device. This can be connected to an LED.
RXLED#	ACBUS0, ACBUS1, ACBUS2, ACBUS3, ACBUS4, ACBUS5, ACBUS6, ACBUS8, ACBUS9	RXLED = Receive signalling output. Pulses low when receiving data (RXD) from the external device. This can be connected to an LED.
TX&RXLED#	ACBUS0, ACBUS1, ACBUS2, ACBUS3, ACBUS4, ACBUS5, ACBUS6, ACBUS8, ACBUS9	LED drive – pulses low when transmitting or receiving data from or to the external device. See Section 4.11 for more details.
SLEEP#	ACBUS0, ACBUS1, ACBUS2, ACBUS3, ACBUS4, ACBUS5, ACBUS6, ACBUS8, ACBUS9	Goes low during USB suspend mode. Typically used to power down an external TTL to RS232 level converter IC in USB to RS232 converter designs.
**CLK30	ACBUS0, ACBUS5, ACBUS6,ACBUS8, ACBUS9	30MHz Clock output.
**CLK15	ACBUS0, ACBUS5, ACBUS6,ACBUS8, ACBUS9	15MHz Clock output.
**CLK7.5	ACBUS0, ACBUS5, ACBUS6,ACBUS8, ACBUS9	7.5MHz Clock output.
TriSt-PU	ACBUS0, ACBUS1, ACBUS2, ACBUS3, ACBUS4, ACBUS5, ACBUS6, ACBUS8, ACBUS9	Input Pull Up
DRIVE 1	ACBUS0, ACBUS5, ACBUS6,ACBUS8, ACBUS9	Output High
DRIVE 0	ACBUS0, ACBUS1, ACBUS2, ACBUS3, ACBUS4, ACBUS5, ACBUS6, ACBUS8, ACBUS9	Output Low
I/O mode	ACBUS5, ACBUS6,ACBUS8, ACBUS9	ACBUS BitBang

Table 3.5 ACBUS Configuration Control

* Must be used with a 10kΩ resistor pull up.

**When in USB suspend mode the outputs clocks are also suspended.

3.5 Pin Configurations

The following section describes the function of the pins when the device is configured in different modes of operation.

3.5.1 FT232H pins used in an UART interface

The FT232H can be configured as a UART interface. When configured in this mode, the pins used and the descriptions of the signals are shown in Table 3.6

Pin No.	Name	Type	UART Configuration Description
13	TXD	OUTPUT	TXD = transmitter output
14	RXD	INPUT	RXD = receiver input
15	RTS#	OUTPUT	RTS# = Ready To send handshake output
16	CTS#	INPUT	CTS# = Clear To Send handshake input
17	DTR#	OUTPUT	DTR# = Data Transmit Ready modem signalling line
18	DSR#	INPUT	DSR# = Data Set Ready modem signalling line
19	DCD#	INPUT	DCD# = Data Carrier Detect modem signalling line
20	RI#	INPUT	RI# = Ring Indicator Control Input. When the Remote Wake up option is enabled in the EEPROM, taking RI# low can be used to resume the PC USB Host controller from suspend.
21	** TXDEN	OUTPUT	TXDEN = (TTL level). Use to enable RS485 level converter
27	** RXLED	OUTPUT	RXLED = Receive signalling output. Pulses low when receiving data (RXD) from the external device (UART Interface). This should be connected to an LED.
28	** TXLED	OUTPUT	TXLED = Transmit signalling output. Pulses low when transmitting data (TXD) to the external device (UART Interface). This should be connected to an LED.

Table 3.6 UART Configured Pin Descriptions

** ACBUS I/O pins

For a functional description of this mode, please refer to section 4.3

NOTE: UART is the device default mode.

3.5.2 FT232H pins used in an FT245 Synchronous FIFO Interface

The FT232H can be configured as a FT245 synchronous FIFO interface. When configured in this mode, the pins used and the descriptions of the signals are shown in Table 3.7. To set this mode the external EEPROM must be set to 245 modes. A software command (FT_SetBitMode) is then sent by the application to the FTDI D2xx driver to tell the chip to enter 245 synchronous FIFO mode. In this mode, data is written or read on the rising edge of the CLKOUT. Refer to Figure 4.4 for timing details.

Pin No.	Name	Type	FT245 Configuration Description
13,14,15,16, 17,18,19,20	ADBUS[7:0]	I/O	D7 to D0 bidirectional FIFO data. This bus is normally input unless OE# is low.
21	RXF#	OUTPUT	When high, do not read data from the FIFO. When low, there is data available in the FIFO which can be read by driving RD# low. When in synchronous mode, data is transferred on every clock that RXF# and RD# are both low. Note that the OE# pin must be driven low at least 1 clock period before asserting RD# low.
25	TXE#	OUTPUT	When high, do not write data into the FIFO. When low, data can be written into the FIFO by driving WR# low. When in synchronous mode, data is transferred on every clock that TXE# and WR# are both low.
26	RD#	INPUT	Enables the current FIFO data byte to be driven onto D0...D7 when RD# goes low. The next FIFO data byte (if available) is fetched from the receive FIFO buffer each CLKOUT cycle until RD# goes high.
27	WR#	INPUT	Enables the data byte on the D0...D7 pins to be written into the transmit FIFO buffer when WR# is low. The next FIFO data byte is written to the transmit FIFO buffer each CLKOUT cycle until WR# goes high.
28	SIWU#	INPUT	The Send Immediate / WakeUp signal combines two functions on a single pin. If USB is in suspend mode (PWREN# = 1) and remote wakeup is enabled in the EEPROM, strobing this pin low will cause the device to request a resume on the USB Bus. Normally, this can be used to wake up the Host PC. During normal operation (PWREN# = 0), if this pin is strobed low any data in the device RX buffer will be sent out over USB on the next Bulk-IN request from the drivers regardless of the pending packet size. This can be used to optimize USB transfer speed for some applications. Tie this pin to VCCIO if not used.
29	CLKOUT	OUTPUT	60 MHz Clock driven from the chip. All signals should be synchronized to this clock.
30	OE#	INPUT	Output enable when low to drive data onto D0-7. This should be driven low at least 1 clock period before driving RD# low to allow for data buffer turn-around.

Table 3.7 FT245 Synchronous FIFO Configured Pin Descriptions

For a functional description of this mode, please refer to section 4.4

3.5.3 FT232H pins used in an FT245 Style Asynchronous FIFO Interface

The FT232H can be configured as a FT245 style asynchronous FIFO interface. When configured in this mode, the pins used and the descriptions of the signals are shown in Table 3.8. To enter this mode the external EEPROM must be set to 245 asynchronous FIFO mode. In this mode, data is written or read on the falling edge of the RD# or WR# signals.

Pin No.	Name	Type	FT245 Configuration Description
13, 14, 15, 16, 17, 18, 19,20	ADBUS[7:0]	I/O	D7 to D0 bidirectional FIFO data. This bus is normally input unless RD# is low.
21	RXF#	OUTPUT	When high, do not read data from the FIFO. When low, there is data available in the FIFO which can be read by driving RD# low. When RD# goes high again RXF# will always go high and only become low again if there is another byte to read. During reset this signal pin is tri-state, but pulled up to VCCIO via an internal 200kΩ resistor.
25	TXE#	OUTPUT	When high, do not write data into the FIFO. When low, data can be written into the FIFO by strobing WR# high, then low. During reset this signal pin is tri-state, but pulled up to VCCIO via an internal 200kΩ resistor.
26	RD#	INPUT	Enables the current FIFO data byte to be driven onto D0...D7 when RD# goes low. Fetches the next FIFO data byte (if available) from the receive FIFO buffer when RD# goes high.
27	WR#	INPUT	Writes the data byte on the D0...D7 pins into the transmit FIFO buffer when WR# goes from high to low.
28	SIWU#	INPUT	The Send Immediate / WakeUp signal combines two functions on a single pin. If USB is in suspend mode (PWREN# = 1) and remote wakeup is enabled in the EEPROM, strobing this pin low will cause the device to request a resume on the USB Bus. Normally, this can be used to wake up the Host PC. During normal operation (PWREN# = 0), if this pin is strobed low any data in the device RX buffer will be sent out over USB on the next Bulk-IN request from the drivers regardless of the pending packet size. This can be used to optimize USB transfer speed for some applications. Tie this pin to VCCIO if not used.

Table 3.8 FT245 Style Asynchronous FIFO Configured Pin Descriptions

For a functional description of this mode, please refer to section 4.5

3.5.4 FT232H can be configured as a Synchronous or Asynchronous Bit-Bang Interface.

Bit-bang mode is an FTDI FT232H device mode that changes the 8 IO lines into an 8 bit bi-directional data bus. This mode is enabled by sending a software command (FT_SetBitMode) to the FTDI driver. When configured in any bit-bang mode, the pins used and the descriptions of the signals are shown in Table 3.9

Pin No.	Name	Type	Configuration Description
13,14,15,16,17, 18,19,20	ADBUS[7:0]	I/O	D7 to D0 bidirectional Bit-Bang parallel I/O data pins
25	WRSTB#	OUTPUT	Write strobe, active low output indicates when new data has been written to the I/O pins from the Host PC (via the USB interface).
26	RDSTB#	OUTPUT	Read strobe, this output rising edge indicates when data has been read from the parallel I/O pins and sent to the Host PC (via the USB interface).
28	SIWU#	INPUT	The Send Immediate / WakeUp signal combines two functions on a single pin. If USB is in suspend mode (PWREN# = 1) and remote wakeup is enabled in the EEPROM, strobing this pin low will cause the device to request a resume on the USB Bus. Normally, this can be used to wake up the Host PC. During normal operation (PWREN# = 0), if this pin is strobed low any data in the device RX buffer will be sent out over USB on the next Bulk-IN request from the drivers regardless of the pending packet size. This can be used to optimize USB transfer speed for some applications. Tie this pin to VCCIO if not used.

Table 3.9 Synchronous or Asynchronous Bit-Bang Configured Pin Descriptions

For functional description of this mode, please refer to section 4.6

3.5.5 FT232H pins used in an MPSSE

The FT232H has a Multi-Protocol Synchronous Serial Engine (MPSSE). This mode is enabled by sending a software command (FT_SetBitMode) to the FTDI D2xx driver. The MPSSE can be configured to a number of industry standard serial interface protocols such as JTAG, I^2C or SPI (MASTER), or it can be used to implement a proprietary bus protocol. For example, it is possible to connect FT232H's to an SRAM configurable FPGA such as supplied by Altera or Xilinx. The FPGA device would normally not be configured (i.e. have no defined function) at power-up. Application software on the PC could use the MPSSE (and D2XX driver) to download configuration data to the FPGA over USB. This data would define the hardware function on power up. The MPSSE can be used to control a number of GPIO pins. When configured in this mode, the pins used and the descriptions of the signals are shown in Table 3.10

Pin No.	Name	Type	MPSSE Configuration Description
13	TCK/SK	OUTPUT	Clock Signal Output. For example: JTAG – TCK, Test interface clock SPI (MASTER) – SK, Serial Clock
14	TDI/DO	OUTPUT	Serial Data Output. For example: JTAG – TDI, Test Data Input SPI (MASTER) – DO
15	TDO/DI	INPUT	Serial Data Input. For example: JTAG – TDO, Test Data output SPI (MASTER) – DI, Serial Data Input
16	TMS/CS	OUTPUT	Output Signal Select. For example: JTAG – TMS, Test Mode Select SPI (MASTER) – CS, Serial Chip Select
17	GPIOL0	I/O	General Purpose input/output
18	GPIOL1	I/O	General Purpose input/output
19	GPIOL2	I/O	General Purpose input/output
20	GPIOL3	I/O	General Purpose input/output
21	GPIOH0	I/O	General Purpose input/output
25	GPIOH1	I/O	General Purpose input/output
26	GPIOH2	I/O	General Purpose input/output
27	GPIOH3	I/O	General Purpose input/output
28	GPIOH4	I/O	General Purpose input/output
29	GPIOH5	I/O	General Purpose input/output
30	GPIOH6	I/O	General Purpose input/output
31	GPIOH7	I/O	General Purpose input/output

Table 3.10 MPSSE Configured Pin Descriptions

For functional description of this mode, please refer to section 4.8

3.5.6 FT232H Pins used as a Fast Serial Interface

The FT232H can be configured for use with high-speed bi-directional isolated serial data. A proprietary FTDI protocol designed to allow galvanic isolated devices to communicate synchronously with the FT232H using just 4 signal wires (over two dual opto-isolators), and two power lines. The peripheral circuitry controls the data transfer rate in both directions, whilst maintaining full data integrity. 12 Mbps (USB full speed) data rates can be achieved when using the proper high speed opto-isolators (see App Note AN-131).

When configured in this mode, the pins used and the descriptions of the signals are shown in Table 3.11.

Pin No.	Name	Type	Fast Serial Interface Configuration Description
13	FSDI	INPUT	Fast serial data input.
14	FSCLK	INPUT	Fast serial clock input. Clock input to FT232H chip to clock data in or out.
15	FSDO	OUTPUT	Fast serial data output.
16	FSCTS	OUTPUT	Fast serial Clear To Send signal output. Driven low to indicate that the chip is ready to send data
28	SIWU#	INPUT	The Send Immediate / WakeUp signal combines two functions on a single pin. If USB is in suspend mode (PWREN# = 1) and remote wakeup is enabled in the EEPROM , strobing this pin low will cause the device to request a resume on the USB Bus. Normally, this can be used to wake up the Host PC. During normal operation (PWREN# = 0), if this pin is strobed low any data in the device RX buffer will be sent out over USB on the next Bulk-IN request from the drivers regardless of the pending packet size. This can be used to optimize USB transfer speed for some applications. Tie this pin to VCCIO if not used.

Table 3.11 Fast Serial Interface Configured Pin Descriptions

For a functional description of this mode, please refer to section 4.9

3.5.7 FT232H Pins Configured as a CPU-style FIFO Interface

The FT232H can be configured in a CPU-style FIFO interface mode which allows a CPU to interface to USB via the FT232H. This mode is enabled in the external EEPROM.

When configured in this mode, the pins used and the descriptions of the signals are shown in Table 3.12

Pin No.	Name	Type	Fast Serial Interface Configuration Description
13, 14, 15, 16, 17, 18, 19, 20	ADBUS[7:0]	I/O	D7 to D0 bidirectional data bus
21	CS#	INPUT	Active low chip select input
25	A0	INPUT	Address bit A0
26	RD#	INPUT	Active Low FIFO Read input
27	WR#	INPUT	Active Low FIFO Write input
28	SIWU#	INPUT	Tie this pin to VCCIO if not used – otherwise, for normal operation The Send Immediate / WakeUp signal combines two functions on a single pin. If USB is in suspend mode (PWREN# = 1) and remote wakeup is enabled in the EEPROM, strobing this pin low will cause the device to request a resume on the USB Bus. Normally, this can be used to wake up the Host PC. During normal operation (PWREN# = 0), if this pin is strobed low any data in the device RX buffer will be sent out over USB on the next Bulk-IN request from the drivers regardless of the pending packet size. This can be used to optimize USB transfer speed for some applications.

Table 3.12 CPU-style FIFO Interface Configured Pin Descriptions

For a functional description of this mode, please refer to section 4.10

3.5.8 FT232H Pins Configured as a FT1248 Interface

The FT232H can be configured as a proprietary FT1248 interface. This mode is enabled in the external EEPROM. When configured in this mode, the pins used and the descriptions of the signals are shown in Table 3.13.

Pin No.	Name	Type	UART Configuration Description
13	MIOSIO0	INPUT /OUTPUT	Bi-directional synchronous command and data bus, bit 0 used to transmit and receive data from/to the master
14	MIOSIO1	INPUT /OUTPUT	Bi-directional synchronous command and data bus, bit 1 used to transmit and receive data from/to the master
15	MIOSIO2	INPUT /OUTPUT	Bi-directional synchronous command and data bus, bit 2 used to transmit and receive data from/to the master
16	MIOSIO3	INPUT /OUTPUT	Bi-directional synchronous command and data bus, bit 3 used to transmit and receive data from/to the master
17	MIOSIO4	INPUT /OUTPUT	Bi-directional synchronous command and data bus, bit 4 used to transmit and receive data from/to the master
18	MIOSIO5	INPUT /OUTPUT	Bi-directional synchronous command and data bus, bit 5 used to transmit and receive data from/to the master
19	MIOSIO6	INPUT /OUTPUT	Bi-directional synchronous command and data bus, bit 6 used to transmit and receive data from/to the master
20	MIOSIO7	INPUT /OUTPUT	Bi-directional synchronous command and data bus, bit 7 used to transmit and receive data from/to the master
21	SCLK	INPUT	Serial clock used to drive the slave device data
27	SS_n	INPUT	Active low slave select 0 from master to slave
28	MISO	OUTPUT	Slave output used to transmit the status of the transmit and receive buffers are empty and full respectively

Table 3.13 FT1248 Configured Pin Descriptions

For functional description of this mode, please refer to section 4.

4 Function Description

The FT232H USB 2.0 Hi-Speed (480Mb/s) to UART/FIFO is an FTDI's 6th generation of ICs. It can be configured in a variety of industry standard serial or parallel interfaces, such as UART, FIFO, JTAG, SPI (MASTER) or I^2C modes. In addition to these, the FT232H introduces the FT1248 interface and supports a CPU-Style FIFO mode, bit-bang and a fast serial interface mode.

4.1 Key Features

USB Hi-Speed to UART/FIFO Interface. The FT232H provides USB 2.0 Hi-Speed (480Mbits/s) to flexible and configurable UART/FIFO Interfaces.

Functional Integration. The FT232H integrates a USB protocol engine which controls the physical Universal Transceiver Macrocell Interface (UTMI) and handles all aspects of the USB 2.0 Hi-Speed interface. The FT232H includes an integrated +1.8V/3.3V Low Drop-Out (LDO) regulator. It also includes 1Kbytes Tx and Rx data buffers. The FT232H integrates the entire USB protocol on a chip with no firmware required.

MPSSE. Multi- Protocol Synchronous Serial Engines (MPSSE), capable of speeds up to 30 Mbits/s, provides flexible synchronous interface configurations.

FT1248 interface. The FT232H supports a new proprietary half-duplex FT1248 interface with a variable bi-directional data bus interface that can be configured as 1, 2, 4, or 8-bits wide and this enables the flexibility to expand the size of the data bus to 8 pins. For details regarding 2-bit, 4-bit and 8-bit modes, please refer to application note AN_167_FT1248_Serial_Parallel Interface Basics available from the FTDI website.

Data Transfer rate. The FT232H supports a data transfer rate up to 12 Mbaud when configured as an RS232/RS422/RS485 UART interface upto 40 Mbytes/second over a synchronous 245 parallel FIFO interface or up to 8 Mbyte/Sec over a asynchronous 245 FIFO interface. Please note the FT232H does not support the baud rates of 7 Mbaud 9 Mbaud, 10 Mbaud and 11 Mbaud.

Latency Timer. A feature of the driver used as a timeout to transmit short packets of data back to the PC. The default is 16ms, but it can be altered between 0ms and 255ms.

Bus (ACBUS) functionality, signal inversion and drive strength selection. There are 11 configurable ACBUS I/O pins. These configurable options are:

1. **TXDEN** – transmit enable for RS485 designs.
2. **PWREN#** - Power control for high power, bus powered designs.
3. **TXLED#** - for pulsing an LED upon transmission of data.
4. **RXLED#** - for pulsing an LED upon receiving data.
5. **TX&RXLED#** - which will pulse an LED upon transmission OR reception of data**.**
6. **SLEEP#** - indicates that the device going into USB suspend mode.
7. **CLK30 / CLK15 / CLK7.5 –** 30MHz, 15MHz and 7.5MHz clock output signal options.
8. **TriSt-PU** – Input pulled up, not used
9. **DRIVE 1** – Output driving high
10. **DRIVE 0** – Output driving low
11. **I/O mode** – ACBUS BitBang

The ACBUS pins can also be individually configured as GPIO pins, similar to asynchronous bit bang mode. It is possible to use this mode while the UART interface is being used, thus providing up to 4 general purpose I/O pins which are available during normal operation.

The ACBUS lines can be configured with any one of these input/output options by setting bits in the external EEPROM see section 3.4.

4.2 Functional Block Descriptions

Multi-Purpose UART/FIFO Controllers. The FT232H has one independent UART/FIFO Controller. This controls the UART data, 245 FIFO data, Fast Serial (opto isolation) or Bit-Bang mode which can be selected by SETUP (FT_SetBitMode) command. Each Multi-Purpose UART/FIFO Controller also contains an MPSSE (Multi Protocol Synchronous Serial Engine). Using this MPSSE, the Multi-Purpose UART/FIFO Controller can be configured under software command, to have one of the MPSSE (SPI (MASTER), I^2C, JTAG).

USB Protocol Engine and FIFO control. The USB Protocol Engine controls and manages the interface between the UTMI PHY and the FIFOs of the chip. It also handles power management and the USB protocol specification.

Port FIFO TX Buffer (1Kbytes). Data from the Host PC is stored in these buffers to be used by the Multi-purpose UART/FIFO controllers. This is controlled by the USB Protocol Engine and FIFO control block.

Port FIFO RX Buffer (1Kbytes). Data from the Multi-purpose UART/FIFO controllers is stored in these blocks to be sent back to the Host PC when requested. This is controlled by the USB Protocol Engine and FIFO control block.

RESET Generator – The integrated Reset Generator Cell provides a reliable power-on reset to the device internal circuitry at power up. The RESET# input pin allows an external device to reset the FT232H. RESET# should be tied to VCCIO (+3.3V) if not being used.

Baud Rate Generators – The Baud Rate Generators provides a x16 or a x10 clock input to the UART's from a 120MHz reference clock and consists of a 14 bit pre-scaler and 4 register bits which provide fine tuning of the baud rate (used to divide by a number plus a fraction). This determines the Baud Rate of the UART which is programmable from 183 baud to 12 Mbaud. See FTDI application note AN_120 on the FTDI website for more details.

EEPROM Interface. If the external EEPROM is fitted, the FT232H can be configured as an asynchronous serial UART (default mode), parallel FIFO (245) mode, FT1248, fast serial (opto isolation) or CPU-Style FIFO. The EEPROM should be a 16 bit wide configuration such as a 93LC56B or equivalent capable of a 1Mbit/s clock rate at VCCIO = +2.97V to 3.63V. The EEPROM is programmable in-circuit over USB using a utility program called FT_Prog available from FTDI web site. Please note that the 93LC46B is not compatible with the FT232H device.

+1.8/3.3V LDO Regulator. The +3.3/+1.8V LDO regulator generates +1.8 volts for the core and the USB transceiver cell and +3.3V for the IO and the internal PLL and USB PHY power supply.

UTMI PHY. The Universal Transceiver Macrocell Interface (UTMI) physical interface cell. This block handles the Full speed / Hi-Speed SERDES (serialise – deserialise) function for the USB TX/RX data. It also provides the clocks for the rest of the chip. A 12 MHz crystal must be connected to the OSCI and OSCO pins or 12 MHz Oscillator must be connected to the OSCI, and the OSCO is left unconnected. A 12K Ohm resistor should be connected between REF and GND on the PCB.

The UTMI PHY functions include:

- Supports 480 Mbit/s "Hi-Speed" (HS)/ 12 Mbit/s "Full Speed" (FS).
- SYNC/EOP generation and checking
- Data and clock recovery from serial stream on the USB.
- Bit-stuffing/unstuffing; bit stuff error detection.
- Manages USB Resume, Wake Up and Suspend functions.
- Single parallel data clock output with on-chip PLL to generate higher speed serial data clocks.

4.3 FT232 UART Interface Mode Description

The FT232H can be configured as a UART with external line drivers, similar to operation with the FTDI FT232R devices. The following examples illustrate how to configure the FT232H with an RS232, RS422 or RS485 interface.

4.3.1 RS232 Configuration

Figure 4.1 illustrates how the FT232H can be configured with an RS232 UART interface.

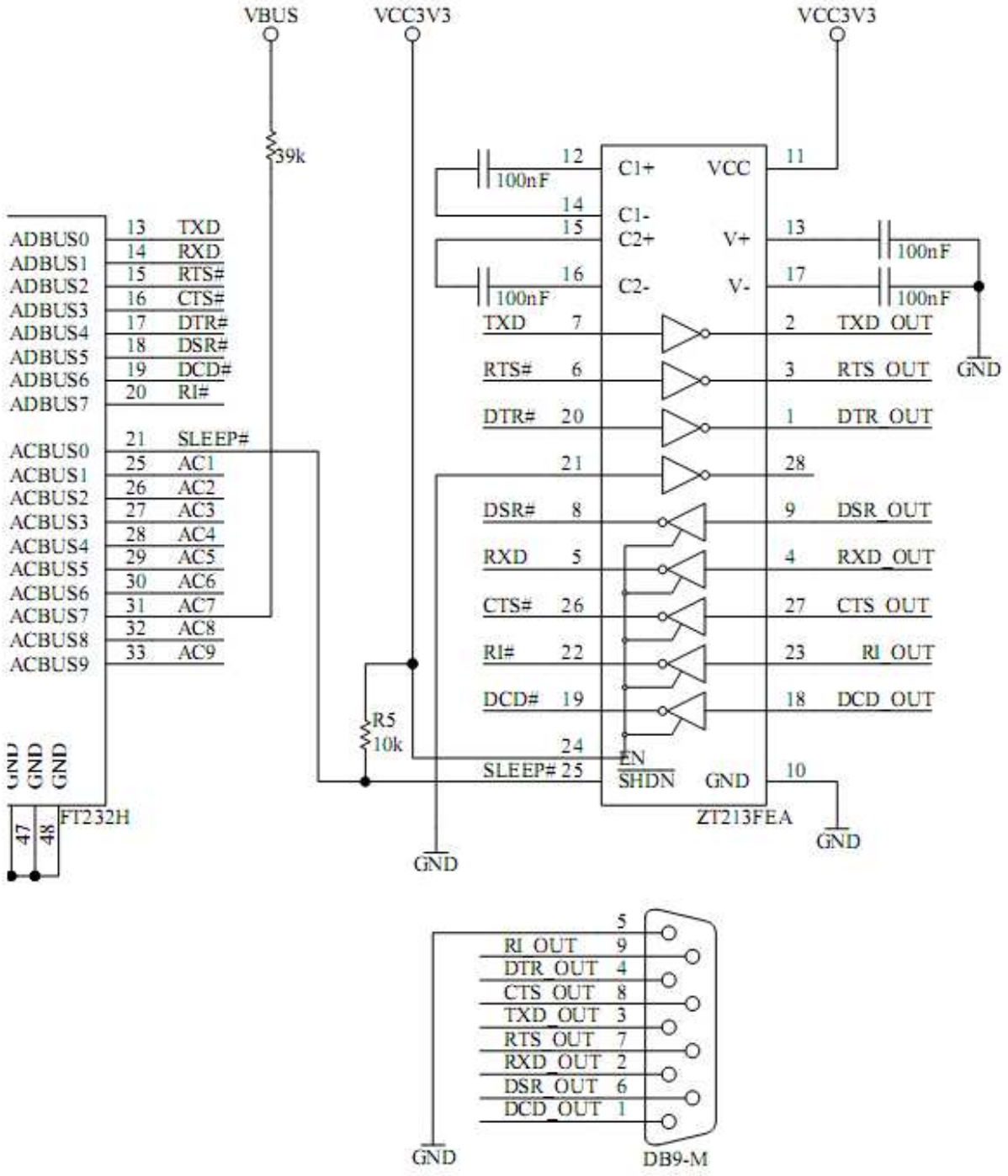

Figure 4.1 RS232 Configuration

4.3.2 RS422 Configuration

Figure 4.2 illustrates how the FT232H can be configured as a RS422 interface.

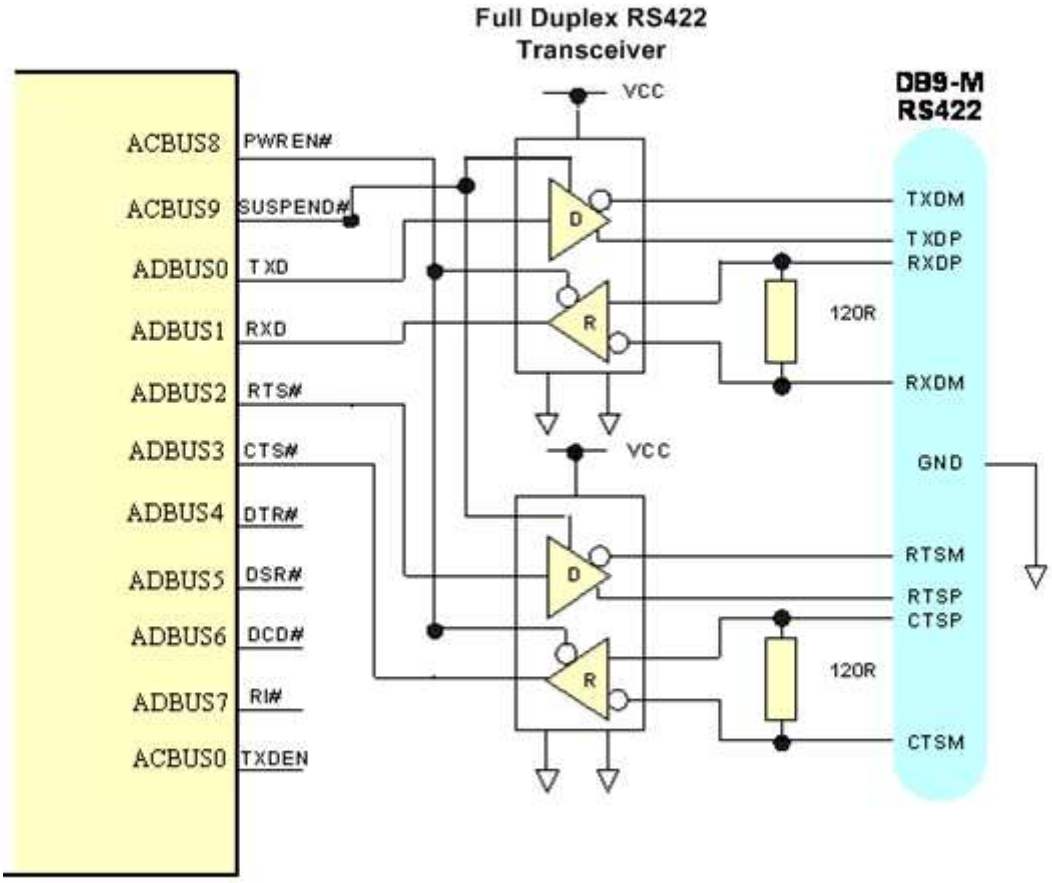

Figure 4.2 Dual RS422 Configuration

In this case the FT232H is configured as UART operating at TTL levels and a level converter device (full duplex RS485 transceiver) is used to convert the TTL level signals from the FT232H to RS422 levels. The PWREN# signal is used to power down the level shifters such that they operate in a low quiescent current when the USB interface is in suspend mode.