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FT25H16
DATASHEET

CONTENTS

1. FEATURES

- 16M -bit Serial Flash
  - 2048K-byte
  - 256 bytes per programmable page

- Standard, Dual, Quad SPI
  - Standard SPI: SCLK, CS#, SI, SO, WP#, HOLD#
  - Dual SPI: SCLK, CS#, IO0, IO1, WP#, HOLD#
  - Quad SPI: SCLK, CS#, IO0, IO1, IO2, IO3

- High Speed Clock Frequency
  - 120MHz for fast read with 30PF load
  - Dual I/O Data transfer up to 240Mbits/s
  - Quad I/O Data transfer up to 480Mbits/s

- Program/Erase Speed
  - Page Program time: 0.4ms typical
  - Sector Erase time: 120ms typical
  - Block Erase time: 0.2/0.4s typical
  - Chip Erase time: 10s typical

- Flexible Architecture
  - Sector of 4K-byte
  - Block of 32/64k-byte

- Low Power Consumption
  - 20mA maximum active current
  - 5uA maximum power down current

- Software/Hardware Write Protection
  - Write protect all/portion of memory via software
  - Enable/Disable protection with WP# Pin
  - Top or Bottom, Sector or Block selection

- Advanced security Features
  - 4*256-Byte Security Registers With OTP Lock

- Single Power Supply Voltage: Full voltage range:2.7~3.6V

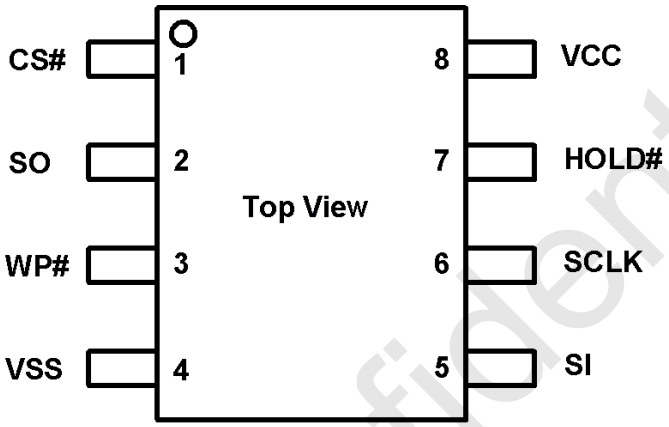
- Minimum 100,000 Program/Erase Cycle

- Hardware Features
  - 8-pin SOP8 (150mil)
  - 8-pin SOP8 (208mil)
  - 8-pin DIP8 (300mil)
  - 8-pin VSOP8 (200mil)
  - 8-pin TSSOP8 (173mil)

2. GENERAL DESCRIPTION

The FT25H16 (16M-bit) Serial flash supports the standard Serial Peripheral Interface (SPI), and supports the Dual/Quad SPI: Serial Clock, Chip Select, Serial Data I/O0 (SI), I/O1 (SO), I/O2 (WP#), and I/O3 (HOLD#). The Dual I/O data is transferred with speed of 240Mbits/s and the Quad I/O & Quad output data is transferred with speed of 480Mbits/s.

CONNECTION DIAGRAM

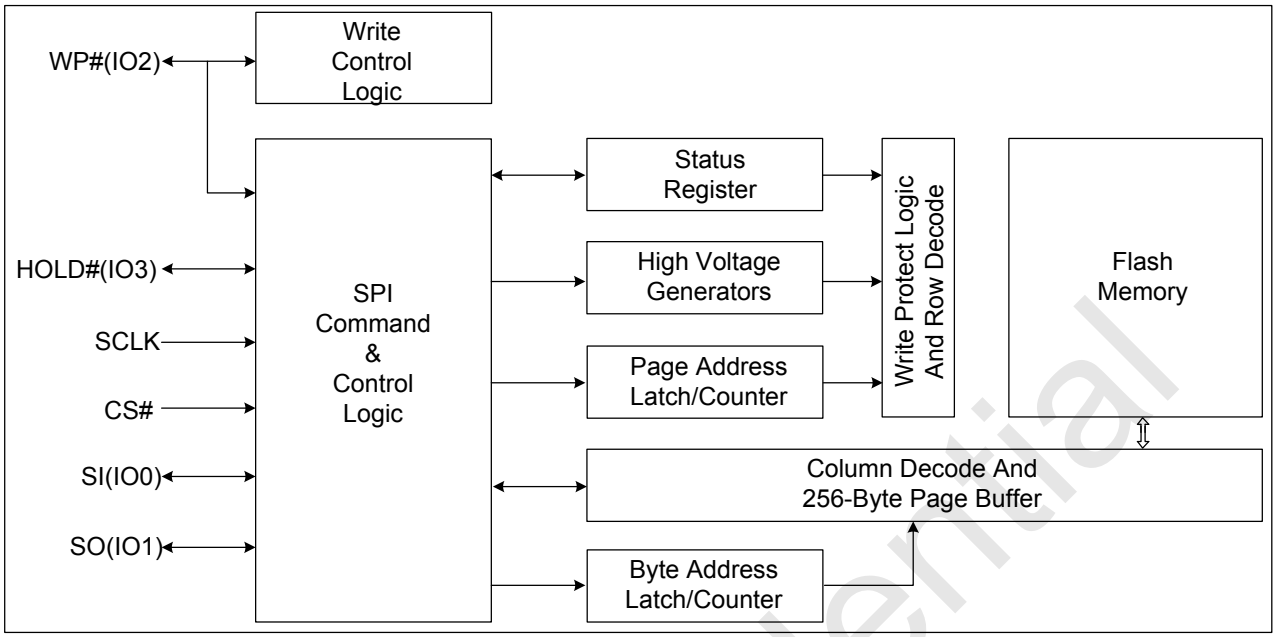


8 – LEAD SOP

PIN DESCRIPTION

Pin Name	I/O	Description
CS#	**I**	Chip Select Input
SO (IO1)	**I/O**	Data Output (Data Input Output 1)
WP# (IO2)	**I/O**	Write Protect Input (Data Input Output 2)
VSS		Ground
SI (IO0)	**I/O**	Data Input (Data Input Output 0)
SCLK	**I**	Serial Clock Input
HOLD# (IO3)	**I/O**	Hold Input (Data Input Output 3)
VCC		Power Supply

BLOCK DIAGRAM



3. MEMORY ORGANIZATION

FT25H16

Each Device has	Each block has	Each sector has	Each page has	
2M	64/32K	4K	256	bytes
8K	256/128	16	-	pages
512	16/8	-	-	sectors
32/64	-	-	-	blocks

UNIFORM BLOCK SECTOR ARCHITECTURE
FT25H16 64K Bytes Block Sector Architecture

Block	Sector	Address range	
31	511	1FF000H	1FFFFFH
	……	……	……
	496	1F0000H	1F0FFFH
30	495	1EF000H	1EFFFFH
	……	……	……
	480	1E0000H	1E0FFFH
……	……	……	……
	……	……	……
	……	……	……
……	……	……	……
	……	……	……
	……	……	……
2	47	02F000H	02FFFFH
	……	……	……
	32	020000H	020FFFH
1	31	01F000H	01FFFFH
	……	……	……
	16	010000H	010FFFH
0	15	00F000H	00FFFFH
	……	……	……
	0	000000H	000FFFH

4. DEVICE OPERATION

SPI Mode

Standard SPI

The FT25H16 features a serial peripheral interface on 4 signals bus: Serial Clock (SCLK), Chip Select (CS#), Serial Data Input (SI) and Serial Data Output (SO). Both SPI bus mode 0 and 3 are supported. Input data is latched on the rising edge of SCLK and data shifts out on the falling edge of SCLK.

Dual SPI

The FT25H16 supports Dual SPI operation when using the “Dual Output Fast Read” and “Dual I/O Fast Read” (3BH and BBH) commands. These commands allow data to be transferred to or from the device at two times the rate of the standard SPI. When using the Dual SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1.

Quad SPI

The FT25H16 supports Quad SPI operation when using the “Quad Output Fast Read”,” Quad I/O Fast Read”, “Quad I/O Word Fast Read” (6BH, EBH, E7H) commands. These commands allow data to be transferred to or from the device at four times the rate of the standard SPI. When using the Quad SPI command the SI and SO pins become bidirectional I/O pins: IO0 and IO1, and WP# and HOLD# pins become IO2 and IO3. Quad SPI commands require the non-volatile Quad Enable bit (QE) in Status Register to be set.

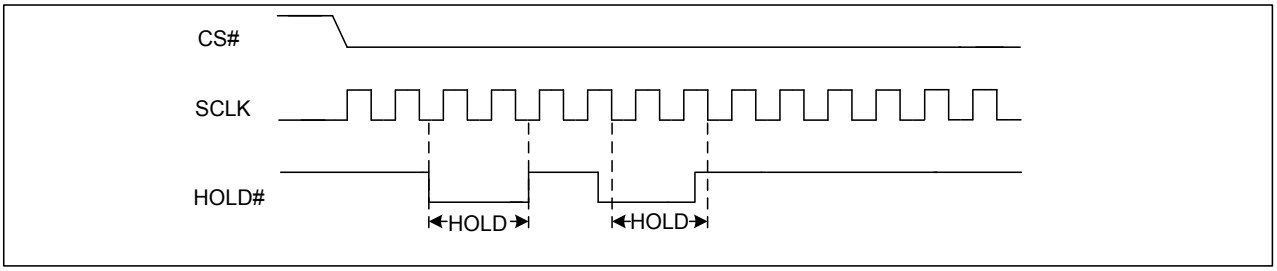
Hold

The HOLD# signal goes low to stop any serial communications with the device, but doesn’t stop the operation of write status register, programming, or erasing in progress.

The operation of HOLD, need CS# keep low, and starts on falling edge of the HOLD# signal, with SCLK signal being low (if SCLK is not being low, HOLD operation will not start until SCLK being low). The HOLD condition ends on rising edge of HOLD# signal with SCLK being low (If SCLK is not being low, HOLD operation will not end until SCLK being low).

The SO is high impedance, both SI and SCLK don’t care during the HOLD operation, if CS# drives high during HOLD operation, it will reset the internal logic of the device. To re-start communication with chip, the HOLD# must be at high and then CS# must be at low.

Figure1. Hold Condition



5. DATA PROTECTION

The FT25H16 provide the following data protection methods:

- Write Enable (WREN) command: The WREN command is set the Write Enable Latch bit (WEL). The WEL bit will return to reset by the following situation:
  - Power-Up
  - Write Disable (WRDI)
  - Write Status Register (WRSR)
  - Page Program (PP)
  - Sector Erase (SE) / Block Erase (BE) / Chip Erase (CE)
- Software Protection Mode: The Block Protect (BP4, BP3, BP2, BP1, BP0) bits define the section of the memory array that can be read but not change.
- Hardware Protection Mode: WP# going low to protected the BP0~BP4 bits and SRP bit.
- Deep Power-Down Mode: In Deep Power-Down Mode, all commands are ignored except the Release from Deep Power-Down Mode command.

Table1.0 FT25H16 Protected area size (CMP=1)

Status Register Content					Memory Content			
BP4	**BP3**	**BP2**	**BP1**	**BP0**	**Blocks**	**Addresses**	**Density**	**Portion**
X	X	0	0	0	0 to 31	000000H-1FFFFFH	2M	ALL
0	0	0	0	1	0 to 30	000000H-1EFFFFH	1984KB	Lower 31/32
0	0	0	1	0	0 to 29	000000H-1DFFFFH	1920KB	Lower 15/16
0	0	0	1	1	0 to 27	000000H-1BFFFFH	1792KB	Lower 7/8
0	0	1	0	0	0 to 23	000000H-17FFFFH	1536KB	Lower 3/4
0	0	1	0	1	0 to 15	000000H-0FFFFFH	1M	Lower 1/2
0	1	0	0	1	1 to 31	010000H-1FFFFFH	1984KB	Upper 31/32
0	1	0	1	0	2 to 31	000000H-01FFFFH	1920KB	Upper 15/16
0	1	0	1	1	4 to 31	000000H-03FFFFH	1792KB	Upper 7/8
0	1	1	0	0	8 to 31	000000H-07FFFFH	1536KB	Upper 3/4
0	1	1	0	1	16 to 31	000000H-0FFFFFH	1M	Upper 1/2
X	X	1	1	X	NONE	000000H-1FFFFFH	NONE	NONE
1	0	0	0	1	31	1FF000H-1FFFFFH	4KB	Top Block
1	0	0	1	0	31	1FE000H-1FFFFFH	8KB	Top Block
1	0	0	1	1	31	1FC000H-1FFFFFH	16KB	Top Block
1	0	1	0	X	31	1F8000H-1FFFFFH	32KB	Top Block
1	1	0	0	1	0	000000H-000FFFH	4KB	Bottom Block
1	1	0	1	0	0	000000H-001FFFH	8KB	Bottom Block
1	1	0	1	1	0	000000H-003FFFH	16KB	Bottom Block
1	1	1	0	X	0	000000H-007FFFH	32KB	Bottom Block

Table1.1 FT25H16 Protected area size (CMP=1)

Status Register Content					Memory Content			
BP4	**BP3**	**BP2**	**BP1**	**BP0**	**Blocks**	**Addresses**	**Density**	**Portion**
X	X	0	0	0	0 to 31	000000H-1FFFFFH	2M	ALL
0	0	0	0	1	0 to 30	000000H-1EFFFFH	1984KB	Lower 31/32
0	0	0	1	0	0 to 29	000000H-1DFFFFH	1920KB	Lower 15/16
0	0	0	1	1	0 to 27	000000H-1BFFFFH	1792KB	Lower 7/8
0	0	1	0	0	0 to 23	000000H-17FFFFH	1536KB	Lower 3/4
0	0	1	0	1	0 to15	000000H-0FFFFFH	1M	Lower 1/2
0	1	0	0	1	1 to 31	010000H-1FFFFFH	1984KB	Upper 31/32
0	1	0	1	0	2 to 31	020000H-1FFFFFH	1920KB	Upper 15/16
0	1	0	1	1	4 to 31	040000H-1FFFFFH	1792KB	Upper 7/8
0	1	1	0	0	8 to 31	080000H-1FFFFFH	1536KB	Upper 3/4
0	1	1	0	1	16 to 31	100000H-1FFFFFH	1M	Upper 1/2
X	X	1	1	X	NONE	NONE	NONE	NONE
1	0	0	0	1	0 to 31	000000H-1FEFFFH	2044KB	Lower 511/512
1	0	0	1	0	0 to 31	000000H-1FDFFFH	2040KB	Lower 255/256
1	0	0	1	1	0 to 31	000000H-1FBFFFH	2032KB	Lower 127/128
1	0	1	0	X	0 to 31	000000H-1F7FFFH	2016KB	Lower 63/64
1	1	0	0	1	0 to 31	001000H-1FFFFFH	2044KB	Upper 511/512
1	1	0	1	0	0 to 31	002000H-1FFFFFH	2040KB	Upper 255/256
1	1	0	1	1	0 to 31	004000H-1FFFFFH	2032KB	Upper 127/128
1	1	1	0	X	0 to 31	008000H-1FFFFFH	2016KB	Upper 63/64

6. STATUS REGISTER

S15	S14	S13	S12	S11	S10	S9	S8
SUS	CMP	Reserved	Reserved	Reserved	LB	QE	Reserved

S7	S6	S5	S4	S3	S2	S1	S0
SRP	BP4	BP3	BP2	BP1	BP0	WEL	WIP

The status and control bits of the Status Register are as follows:

WIP bit.

The Write In Progress (WIP) bit indicates whether the memory is busy in program/erase/write status register progress. When WIP bit sets to 1, means the device is busy in program/erase/write status register progress, when WIP bit sets 0, means the device is not in program/erase/write status register progress.

WEL bit.

The Write Enable Latch (WEL) bit indicates the status of the internal Write Enable Latch. When set to 1 the internal Write Enable Latch is set, when set to 0 the internal Write Enable Latch is reset and no Write Status Register, Program or Erase command is accepted.

BP4, BP3, BP2, BP1, BP0 bits.

The Block Protect (BP4, BP3, BP2, BP1, BP0) bits are non-volatile. They define the size of the area to be software protected against Program and Erase commands. These bits are written with the Write Status Register (WRSR) command. When the Block Protect (BP4, BP3, BP2, BP1, BP0) bits are set to 1, the relevant memory area (as defined in Table1).becomes protected against Page Program (PP), Sector Erase (SE) and Block Erase (BE) commands. The Block Protect (BP4, BP3, BP2, BP1, BP0) bits can be written provided that the Hardware Protected mode has not been set. The Chip Erase (CE) command is executed, if the Block Protect (BP2, BP1, BP0) bits and CMP are all 0 or all 1.

SRP bit.

The Status Register Protect (SRP) bit is non-volatile Read/Write bits in the status register. The SRP bit controls the method of write protection: software protection, hardware protection, power supply lock-down or one time programmable protection.

SRP	WP#	Status Register	Description
0	X	Software Protected	The Status Register can be written to after a Write Enable command, WEL=1.(Default)
1	0	Hardware Protected	WP#=0,the Status Register locked and can not be written to.
1	1	Hardware Unprotected	WP#=1,the Status Register is unlocked and can be written to after a Write Enable command, WEL=1.

QE bit.

The Quad Enable (QE) bit is a non-volatile Read/Write bit in the Status Register that allows Quad operation. When the QE bit is set to 0 (Default) the WP# pin and HOLD# pin are enable. When the QE pin is set to 1, the Quad IO2 and IO3 pins are enabled. (The QE bit should never be set to 1 during standard SPI or Dual SPI operation if the WP# or HOLD# pins are tied directly to the power supply or ground)

LB bit.

The LB bit is a non-volatile One Time Program (OTP) bit in Status Register (S10) that provide the write protect control

and status to the Security Registers. The default state of LB is 0, the security registers are unlocked. LB can be set to 1 individually using the Write Register instruction. LB is One Time Programmable, once it's set to 1, the Security Registers will become read-only permanently.

CMP bit.

The CMP bit is a non-volatile Read/Write bit in the Status Register (S14). It is used in conjunction the BP4-BP0 bits to provide more flexibility for the array protection. Please see the Status registers Memory Protection table for details. The default setting is CMP=0.

SUS bit.

The SUS bit is a read only bit in the status register (S15) that is set to 1 after executing an Erase/Program Suspend (75H) command. The SUS bit is cleared to 0 by Erase/Program Resume (7AH) command as well as a power-down, power-up cycle.

7. COMMANDS DESCRIPTION

All commands, addresses and data are shifted in and out of the device, beginning with the most significant bit on the first rising edge of SCLK after CS# is driven low. Then, the one-byte command code must be shifted in to the device, most significant bit first on SI, each bit being latched on the rising edges of SCLK.

See Table2, every command sequence starts with a one-byte command code. Depending on the command, this might be followed by address bytes, or by data bytes, or by both or none. CS# must be driven high after the last bit of the command sequence has been shifted in. For the command of Read, Fast Read, Read Status Register or Release from Deep Power-Down, and Read Device ID, the shifted-in command sequence is followed by a data-out sequence. CS# can be driven high after any bit of the data-out sequence is being shifted out.

For the command of Page Program, Sector Erase, Block Erase, Chip Erase, Write Status Register, Write Enable, Write Disable or Deep Power-Down command, CS# must be driven high exactly at a byte boundary, otherwise the command is rejected, and is not executed. That is CS# must driven high when the number of clock pulses after CS# being driven low is an exact multiple of eight. For Page Program, if at any time the input byte is not a full byte, nothing will happen and WEL will not be reset.

Table2. Commands

Command Name	Byte1	Byte2	Byte3	Byte4	Byte5	Byte6	n-Bytes
Write Enable	06H						
Write Disable	04H						
Read Status Register	05H	(S7-S0)					(continuous)
Read Status Register-1	35H	(S15-S8)					(continuous)
Write Status Register	01H	(S7-S0)	(S15-S8)				(continuous)
Read Data	03H	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	(continuous)
Fast Read	0BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	(continuous)
Dual Output Fast Read	3BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(1)	(continuous)
Dual I/O Fast Read	BBH	A23-A8(2)	A7-A0 M7-M0(2)	(D7-D0)(1)			(continuous)
Quad Output Fast Read	6BH	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)(3)	(continuous)
Quad I/O Fast Read	EBH	A23-A0 M7-M0(4)	Dummy(5)	(D7-D0)(3)			(continuous)
Quad I/O Word Fast Read	E7H	A23-A0 M7-M0(4)	Dummy(6)	(D7-D0)(3)			(continuous)
Continuous Read Reset	FFH						
Page Program	02H	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	
Quad Page Program	32H	A23-A16	A15-A8	A7-A0	(D7-D0)(3)		
Sector Erase	20H	A23-A16	A15-A8	A7-A0			
Block Erase(32KB)	52H	A23-A16	A15-A8	A7-A0			
Block Erase(64KB)	D8H	A23-A16	A15-A8	A7-A0			
Chip Erase	C7/60H						

Program/Erase Suspend	75H						
Program/Erase Resume	7AH						
Deep Power-Down	B9H						
Release From Deep Power-Down, And Read Device ID	ABH	dummy	dummy	dummy	(DID7-DID0)		(continuous)
Release From Deep Power-Down	ABH						
Manufacturer/Device ID	90H	dummy	dummy	00H	(MID7-MID0)	(DID7-DID0)	(continuous)
High Speed Mode	A3H	dummy	dummy	dummy			
Read Identification	9FH	(MID7-MID 0)	(JDID15-J DID8)	(JDID7-JDI D0)			(continuous)
Erase Security Register(8)	44H	A23-A16	A15-A8	A7-A0			
Program Security Register(8)	42H	A23-A16	A15-A8	A7-A0	(D7-D0)	(Next byte)	
Read Security Register(8)	48H	A23-A16	A15-A8	A7-A0	dummy	(D7-D0)	

NOTE:

1. Dual Output data

IO0 = (D6, D4, D2, D0)

IO1 = (D7, D5, D3, D1)

2. Dual Input Address

IO0 = A22, A20, A18, A16, A14, A12, A10, A8,A6, A4, A2, A0, M6, M4, M2, M0

IO1 = A23, A21, A19, A17, A15, A13, A11, A9,A7, A5, A3, A1, M7, M5, M3, M1

3. Quad Output Data

IO0 = (D4, D0, …..)

IO1 = (D5, D1, …..)

IO2 = (D6, D2, …..)

IO3 = (D7, D3, …..)

4. Quad Input Address

IO0 = A20, A16, A12, A8, A4, A0, M4, M0

IO1 = A21, A17, A13, A9, A5, A1, M5, M1

IO2 = A22, A18, A14, A10, A6, A2, M6, M2

IO3 = A23, A19, A15, A11, A7, A3, M7, M3

5. Quad I/O Fast Read Data

IO0 = (x, x, x, x, D4, D0,…)

IO1 = (x, x, x, x, D5, D1,…)

IO2 = (x, x, x, x, D6, D2,…)

IO3 = (x, x, x, x, D7, D3,…)

6. Quad I/O Word Fast Read Data

IO0 = (x, x, D4, D0,…)

IO1 = (x, x, D5, D1,…)

IO2 = (x, x, D6, D2,…)

IO3 = (x, x, D7, D3,…)

7. Quad I/O Word Fast Read Data: the lowest address bit must be 0.

8. Security Registers Address:

Security Register0: A23-A16=00H, A15-A8=00H, A7-A0= Byte Address;

Security Register1: A23-A16=00H, A15-A8=01H, A7-A0= Byte Address;

Security Register2: A23-A16=00H, A15-A8=02H, A7-A0= Byte Address;

Security Register3: A23-A16=00H, A15-A8=03H, A7-A0= Byte Address.

Table of ID Definitions:

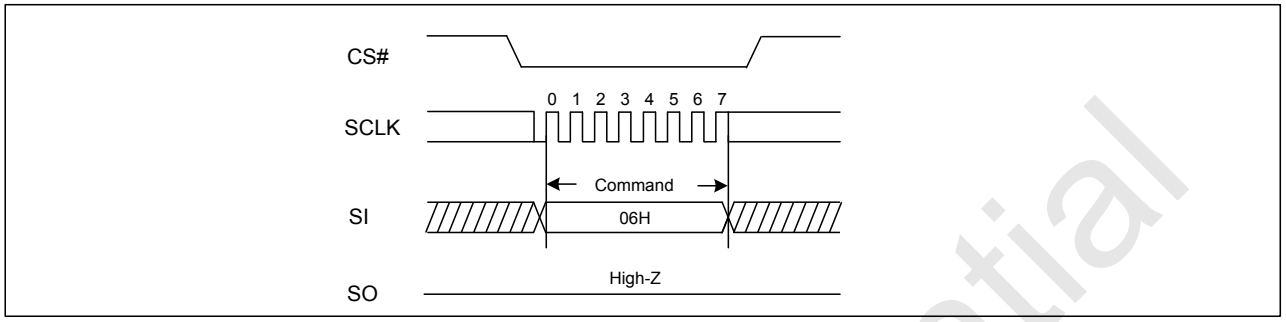
FT25H16

Operation Code	M7-M0	ID15-ID8	ID7-ID0
9FH	0E	40	15
90H	0E		14
ABH			14

7.1. Write Enable (WREN) (06H)

The Write Enable (WREN) command is for setting the Write Enable Latch (WEL) bit. The Write Enable Latch (WEL) bit must be set prior to every Page Program (PP), Sector Erase (SE), Block Erase (BE), Chip Erase (CE) and Write Status Register (WRSR) command. The Write Enable (WREN) command sequence: CS# goes low→Sending the Write Enable command→CS# goes high.

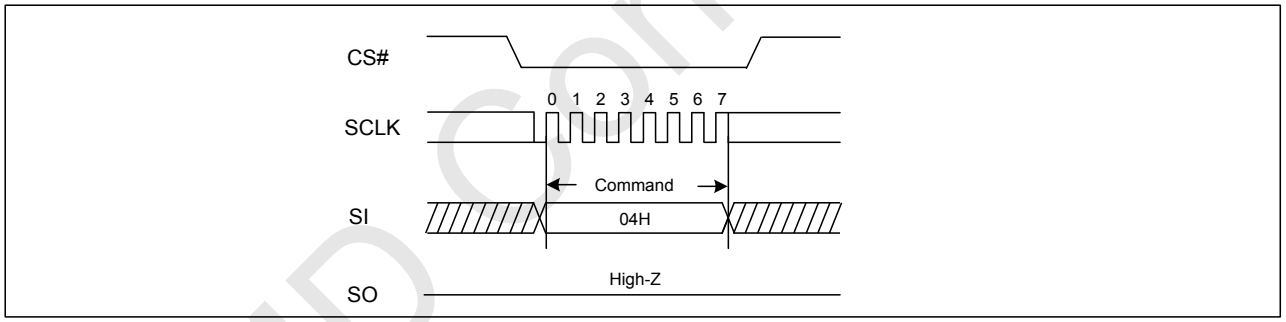
Figure2. Write Enable Sequence Diagram



7.2. Write Disable (WRDI) (04H)

The Write Disable command is for resetting the Write Enable Latch (WEL) bit. The Write Disable command sequence: CS# goes low→Sending the Write Disable command→CS# goes high. The WEL bit is reset by following condition: Power-up and upon completion of the Write Status Register, Page Program, Sector Erase, Block Erase and Chip Erase commands.

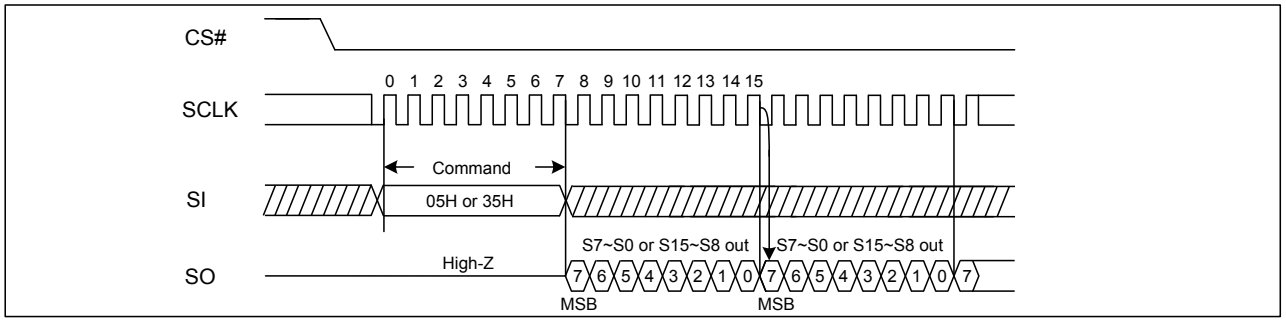
Figure3. Write Disable Sequence Diagram



7.3. Read Status Register (RDSR) (05H or 35H)

The Read Status Register (RDSR) command is for reading the Status Register. The Status Register may be read at any time, even while a Program, Erase or Write Status Register cycle is in progress. When one of these cycles is in progress, it is recommended to check the Write In Progress (WIP) bit before sending a new command to the device. It is also possible to read the Status Register continuously. For command code “05H”, the SO will output Status Register bits S7~S0. The command code “35H”, the SO will output Status Register bits S15~S8.

Figure4. Read Status Register Sequence Diagram



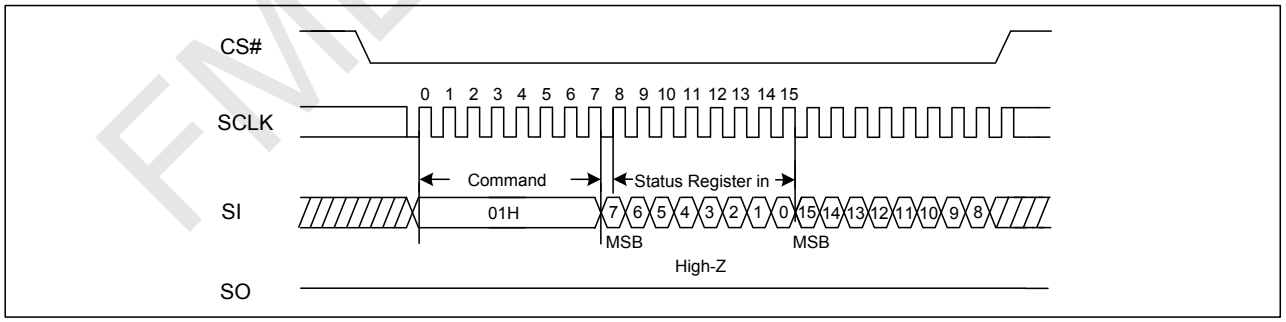
7.4. Write Status Register (WRSR) (01H)

The Write Status Register (WRSR) command allows new values to be written to the Status Register. Before it can be accepted, a Write Enable (WREN) command must previously have been executed. After the Write Enable (WREN) command has been decoded and executed, the device sets the Write Enable Latch (WEL).

The Write Status Register (WRSR) command has no effect on S15, S1 and S0 of the Status Register. CS# must be driven high after the eighth or sixteen bit of the data byte has been latched in. If not, the Write Status Register (WRSR) command is not executed. If CS# is driven high after eighth bit of the data byte, the CMP and QE bit will be cleared to 0. As soon as CS# is driven high, the self-timed Write Status Register cycle (whose duration is t_W) is initiated. While the Write Status Register cycle is in progress, the Status Register may still be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Write Status Register cycle, and is 0 when it is completed. When the cycle is completed, the Write Enable Latch (WEL) is reset.

The Write Status Register (WRSR) command allows the user to change the values of the Block Protect (BP4, BP3, BP2, BP1, BP0) bits, to define the size of the area that is to be treated as read-only, as defined in Table1. The Write Status Register (WRSR) command also allows the user to set or reset the Status Register Protect (SRP) bit in accordance with the Write Protect (WP#) signal. The Status Register Protect (SRP) bit and Write Protect (WP#) signal allow the device to be put in the Hardware Protected Mode. The Write Status Register (WRSR) command is not executed once the Hardware Protected Mode is entered.

Figure5. Write Status Register Sequence Diagram

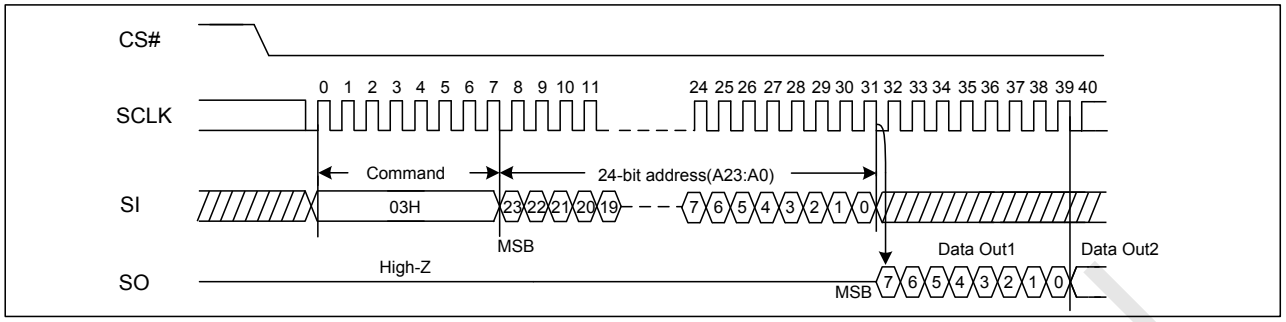


7.5. Read Data Bytes (READ) (03H)

The Read Data Bytes (READ) command is followed by a 3-byte address (A23-A0), each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency f_R, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The whole memory can, therefore, be read with a single Read Data Bytes (READ)

command. Any Read Data Bytes (READ) command, while an Erase, Program or Write cycle is in progress, is rejected without having any effects on the cycle that is in progress.

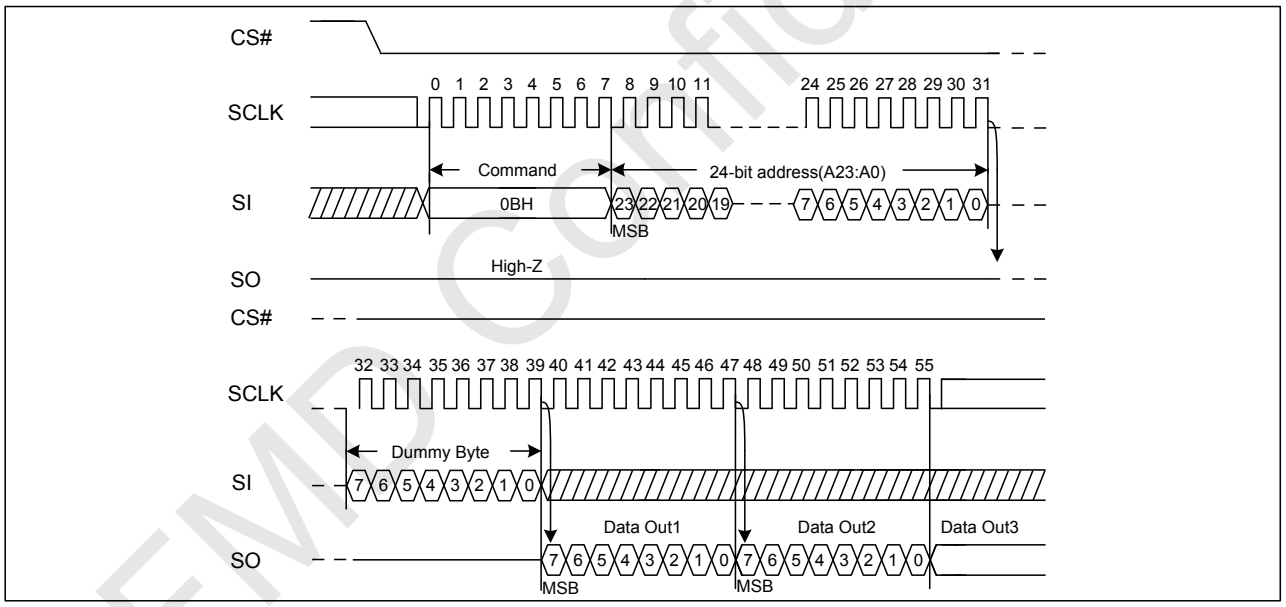
Figure6. Read Data Bytes Sequence Diagram



7.6. Read Data Bytes At Higher Speed (Fast Read) (0BH)

The Read Data Bytes at Higher Speed (Fast Read) command is for quickly reading data out. It is followed by a 3-byte address (A23-A0) and a dummy byte, each bit being latched-in during the rising edge of SCLK. Then the memory content, at that address, is shifted out on SO, each bit being shifted out, at a Max frequency f_C, during the falling edge of SCLK. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

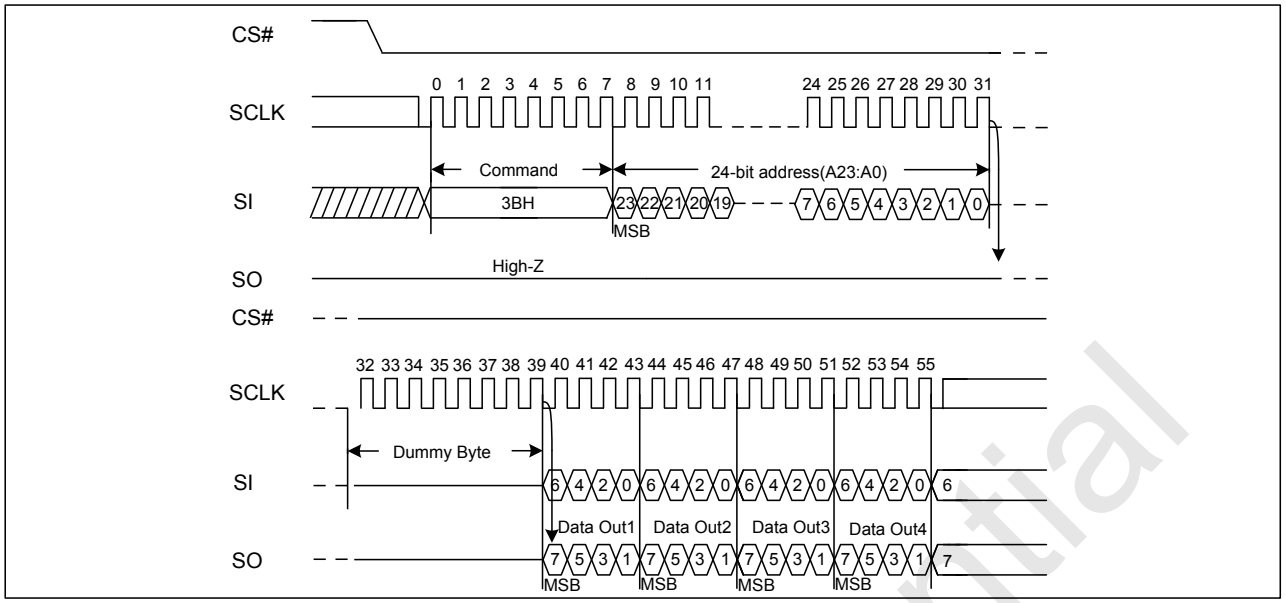
Figure7. Read Data Bytes at Higher Speed Sequence Diagram



7.7. Dual Output Fast Read (3BH)

The Dual Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in followed Figure8. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

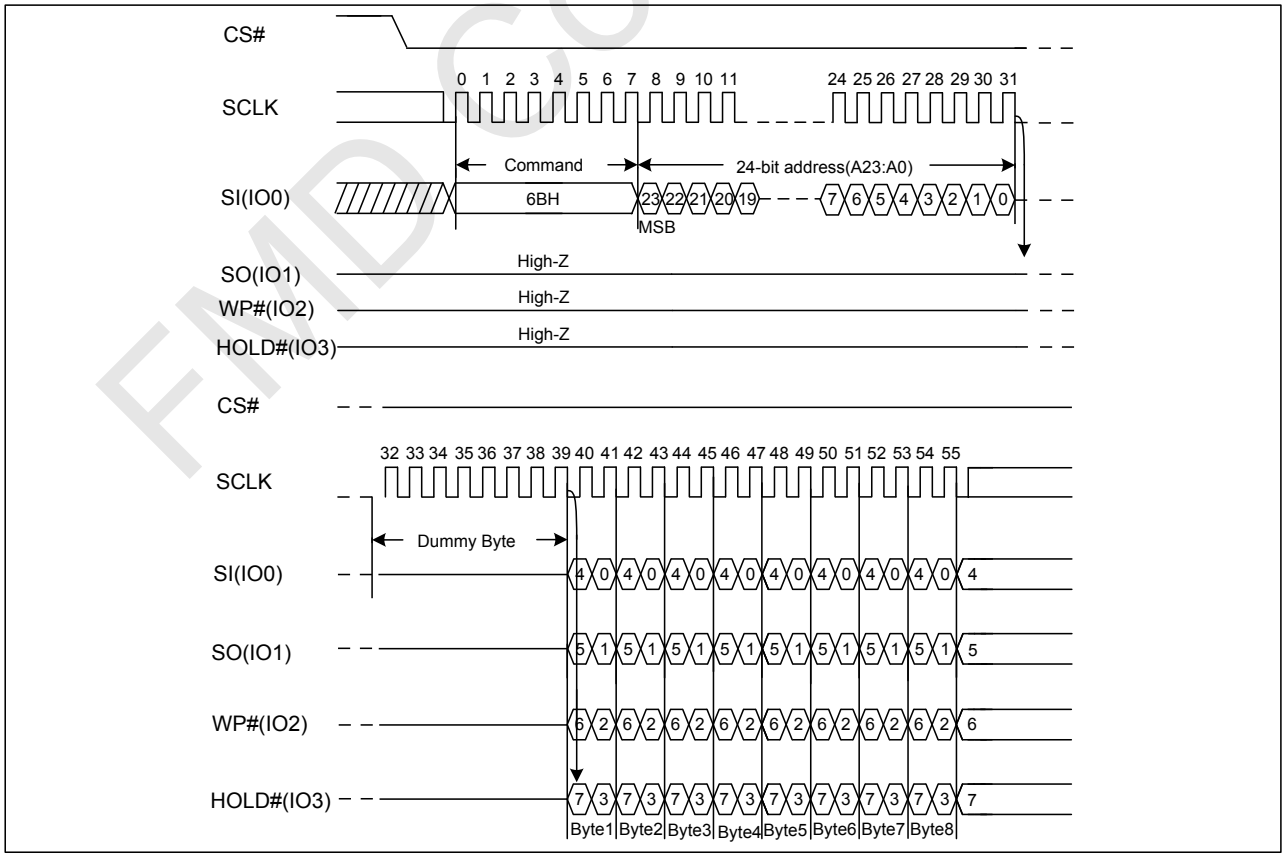
Figure8. Dual Output Fast Read Sequence Diagram



7.8. Quad Output Fast Read (6BH)

The Quad Output Fast Read command is followed by 3-byte address (A23-A0) and a dummy byte, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO3, IO2, IO1 and IO0. The command sequence is shown in followed Figure9. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out.

Figure9. Quad Output Fast Read Sequence Diagram



7.9. Dual I/O Fast Read (BBH)

The Dual I/O Fast Read command is similar to the Dual Output Fast Read command but with the capability to input the 3-byte address (A23-0) and a “Continuous Read Mode” byte 2-bit per clock by SI and SO, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 2-bit per clock cycle from SI and SO. The command sequence is shown in followed Figure10. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. To ensure optimum performance the High Speed mode (HSM) command (A3H) must be executed once, prior to the Dual I/O Fast Read command.

Dual I/O Fast Read with “Continuous Read Mode”

The Dual I/O Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7- 0) after the input 3-byte address (A23-A0). If the “Continuous Read Mode” bits (M5- 4) =(1, 0), then the next Dual I/O Fast Read command (after CS# is raised and then lowered) does not require the BBH command code. The command sequence is shown in followed Figure11. If the “Continuous Read Mode” bits (M5- 4) do not equal (1, 0), the next command requires the first BBH command code, thus returning to normal operation. A “Continuous Read Mode” Reset command can be used to reset (M5- 4) before issuing normal command.

Figure10. Dual I/O Fast Read Sequence Diagram (M5-4≠(1, 0))

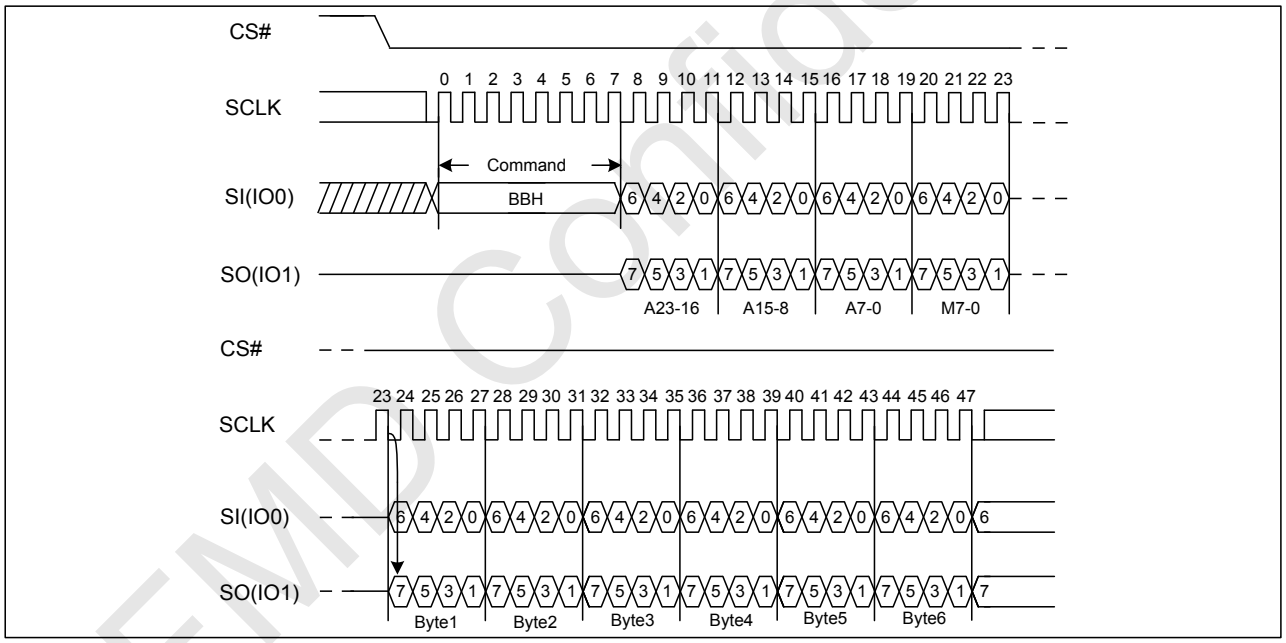
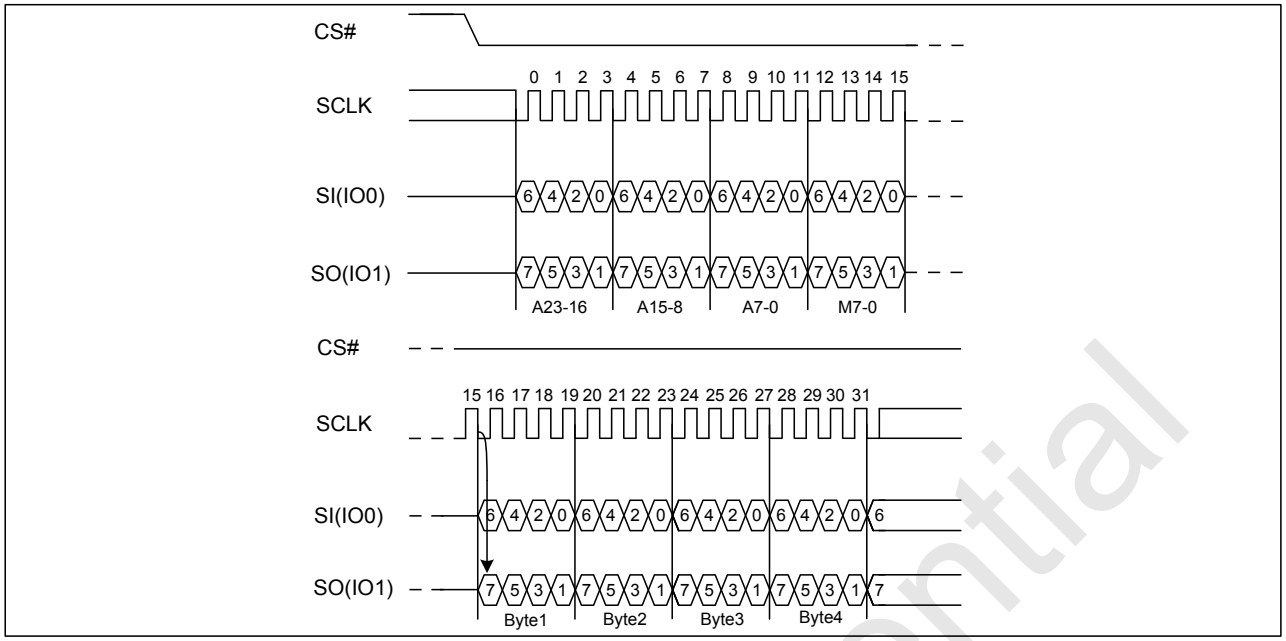


Figure11. Dual I/O Fast Read Sequence Diagram (M5-4= (1, 0))



7.10. Quad I/O Fast Read (EBH)

The Quad I/O Fast Read command is similar to the Dual I/O Fast Read command but with the capability to input the 3-byte address (A23-0) and a “Continuous Read Mode” byte and 4-dummy clock 4-bit per clock by IO0, IO1, IO3, IO4, each bit being latched in during the rising edge of SCLK, then the memory contents are shifted out 4-bit per clock cycle from IO0, IO1, IO2, IO3. The command sequence is shown in followed Figure12. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Fast read command. To ensure optimum performance the High Speed mode (HSM) command (A3H) must be executed once, prior to the Quad I/O Fast Read command.

Quad I/O Fast Read with “Continuous Read Mode”

The Quad I/O Fast Read command can further reduce command overhead through setting the “Continuous Read Mode” bits (M7-0) after the input 3-byte address (A23-A0). If the “Continuous Read Mode” bits (M5- 4) =(1, 0), then the next Quad I/O Fast Read command (after CS# is raised and then lowered) does not require the EBH command code. The command sequence is shown in followed Figure13. If the “Continuous Read Mode” (M5- 4) do not equal (1, 0), the next command requires the first EBH command code, thus returning to normal operation. A “Continuous Read Mode” Reset command can be used to reset (M5- 4) before issuing normal command.

Figure12. Quad I/O Fast Read Sequence Diagram (M5-4≠(1, 0))

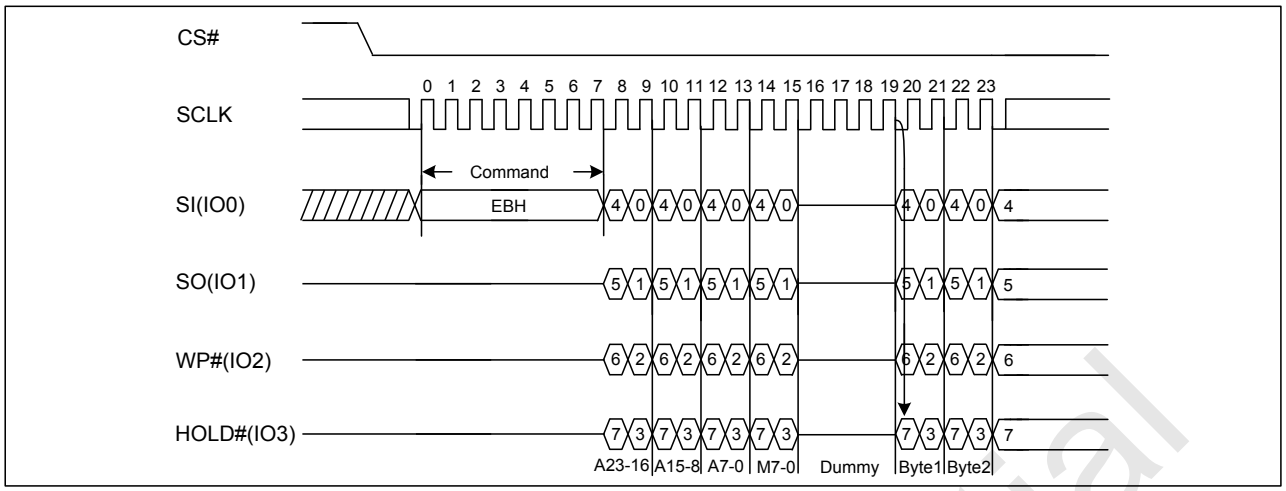
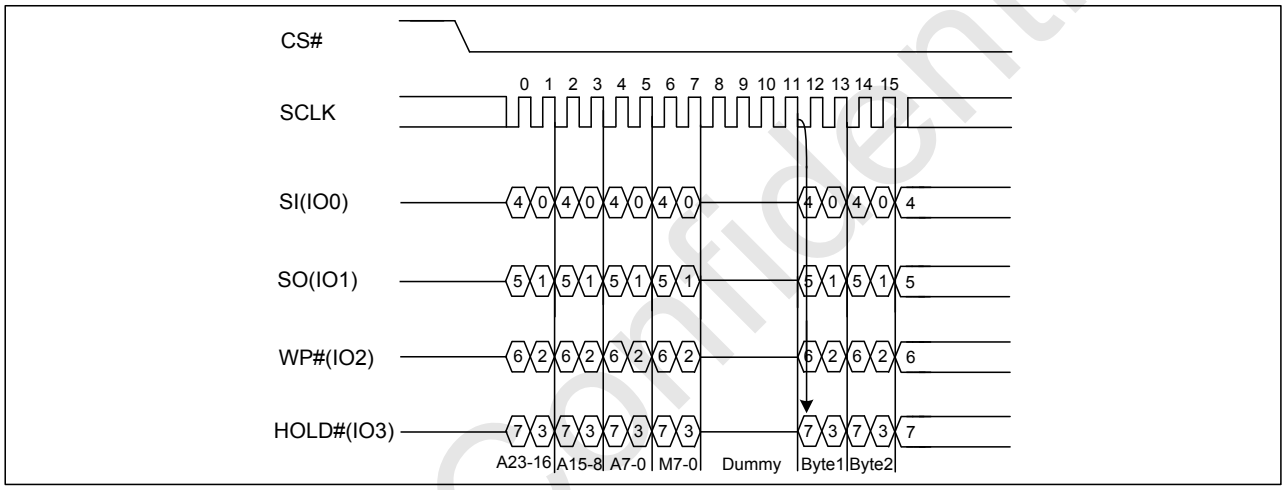


Figure13. Quad I/O Fast Read Sequence Diagram (M5-4= (1, 0))



7.11. Quad I/O Word Fast Read (E7H)

The Quad I/O Word Fast Read command is similar to the Quad I/O Fast Read command except that the lowest address bit (A0) must equal 0 and only 2-dummy clock. The command sequence is shown in followed Figure14. The first byte addressed can be at any location. The address is automatically incremented to the next higher address after each byte of data is shifted out. The Quad Enable bit (QE) of Status Register (S9) must be set to enable for the Quad I/O Word Fast read command. To ensure optimum performance the High Speed mode (HSM) command (A3H) must be executed once, prior to the Quad I/O Word Fast Read command.

Quad I/O Word Fast Read with "Continuous Read Mode"

The Quad I/O Word Fast Read command can further reduce command overhead through setting the "Continuous Read Mode" bits (M7-0) after the input 3-byte address (A23-A0). If the "Continuous Read Mode" bits (M5- 4) =(1, 0), then the next Quad I/O Word Fast Read command (after CS# is raised and then lowered) does not require the E7H command code. The command sequence is shown in followed Figure15. If the "Continuous Read Mode" bits (M5- 4) do not equal (1, 0), the next command requires the first E7H command code, thus returning to normal operation. A "Continuous Read Mode" Reset command can be used to reset (M7-0) before issuing normal command.

Figure14. Quad I/O Word Fast Read Sequence Diagram (M5-4≠(1, 0))

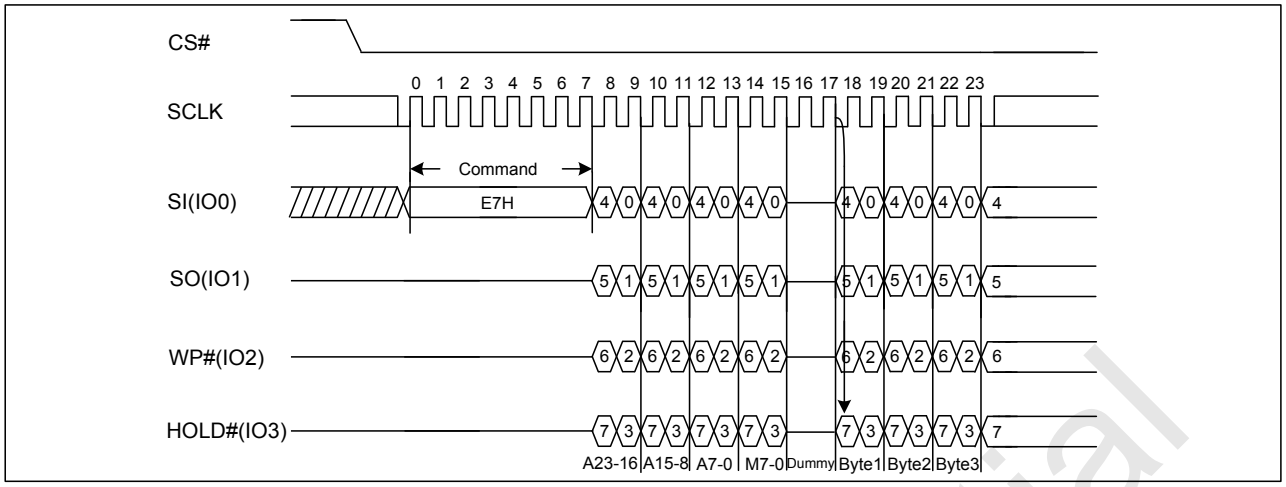
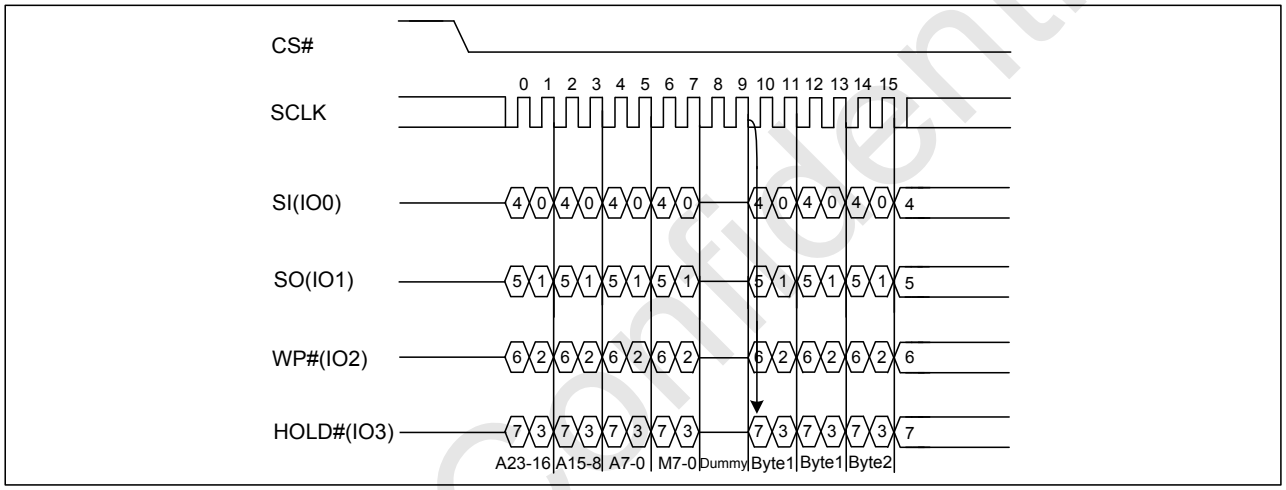


Figure15. Quad I/O Word Fast Read Sequence Diagram (M5-4= (1, 0))



7. 12. Page Program (PP) (02H)

The Page Program (PP) command is for programming the memory. A Write Enable (WREN) command must previously have been executed to set the Write Enable Latch (WEL) bit before sending the Page Program command.

The Page Program (PP) command is entered by driving CS# Low, followed by the command code, three address bytes and at least one data byte on SI. If the 8 least significant address bits (A7-A0) are not all zero, all transmitted data that goes beyond the end of the current page are programmed from the start address of the same page (from the address whose 8 least significant bits (A7-A0) are all zero). CS# must be driven low for the entire duration of the sequence. The Page Program command sequence: CS# goes low→sending Page Program command→3-byte address on SI→at least 1 byte data on SI→ CS# goes high. The command sequence is shown in Figure16. If more than 256 bytes are sent to the device, previously latched data are discarded and the last 256 data bytes are guaranteed to be programmed correctly within the same page. If less than 256 data bytes are sent to device, they are correctly programmed at the requested addresses without having any effects on the other bytes of the same page. CS# must be driven high after the eighth bit of the last data byte has been latched in; otherwise the Page Program (PP) command is not executed.

As soon as CS# is driven high, the self-timed Page Program cycle (whose duration is t_{PP}) is initiated. While the Page Program cycle is in progress, the Status Register may be read to check the value of the Write In Progress (WIP) bit. The Write In Progress (WIP) bit is 1 during the self-timed Page Program cycle, and is 0