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Future Technology Devices International Ltd.

FT313H

(USB2.0 HS Embedded Host Controller)

The FT313H is a Hi-Speed Universal Serial Bus (USB) Host Controller compatible with Universal Serial Bus Specification Rev 2.0 and supports data transfer speeds of up to 480M bit/s. The FT313H has the following advanced features:

- Single chip USB2.0 Hi-Speed compatible.
- Compatible to Enhanced Host Controller Interface Specification Rev 1.0.
- The USB1.1 host is integrated into the USB2.0 EHCI compatible host controller.
- Single USB host port.
- Supports data transfer at high-speed (480M bit/s), full-speed (12M bit/s), and low-speed (1.5M bit/s).
- Supports the Isochronous, Interrupt, Control, and Bulk transfers.
- Supports the split transaction for high-speed Hub and the preamble transaction for full-speed Hub.
- Supports multiple processor interfaces with 8-bit or 16-bit bus: SRAM, NOR Flash, and General multiplex.
- Single configurable interrupt (INT) line for host controller.
- Integrated 24kB high speed RAM memory.
- Supports DMA operation.
- Integrated Phase-Locked Loop (PLL) supports external 12MHz, 19.2MHz, and 24MHz crystal, and direct external clock source input.
- Low power consumption for portable application.
- Supports bus interface I/O voltage from 1.62V to 3.63V.
- Supports hybrid power mode; VCC(3V3) is not present, VCC(I/O) is powered.
- Internal voltage regulator supplies 1.2v to the digital core.
- Supports Battery Charging Specification Rev 1.2.
- The downstream port can be configured as SDP, CDP or DCP.
- Supports VBUS power switching and over current control.
- -40°C to 85°C extended operating temperature range.
- Available in compact Pb-free 64 Pin QFN, LQFP and TQFP packages (all RoHS compliant).

1 Typical Applications

- TV/TV box
- Printer
- Instrumentation
- Media player
- Tablet
- Set-top box

1.1 Part Numbers

Part Number	Package
FT313HQ-x	64 Pin QFN
FT313HL-x	64 Pin LQFP
FT313HP-x	64 Pin TQFP

Table 1-1 FT313H Numbers

Note: Packaging codes for x is:

-R: Taped and Reel, (QFN is 3000pcs, LQFP is 1000 pcs, TQFP is 2500pcs per reel)

-T: Tray packing, (QFN is 2600pcs, LQFP is 1600 pcs, TQFP is 2500pcs per tray)

For example: FT313HQ-R is 3000 QFN pcs in taped and reel packaging

1.2 USB Compliant

At the time of writing this datasheet, the FT313H was still to complete USB compliance testing.

2 FT313H Block Diagram

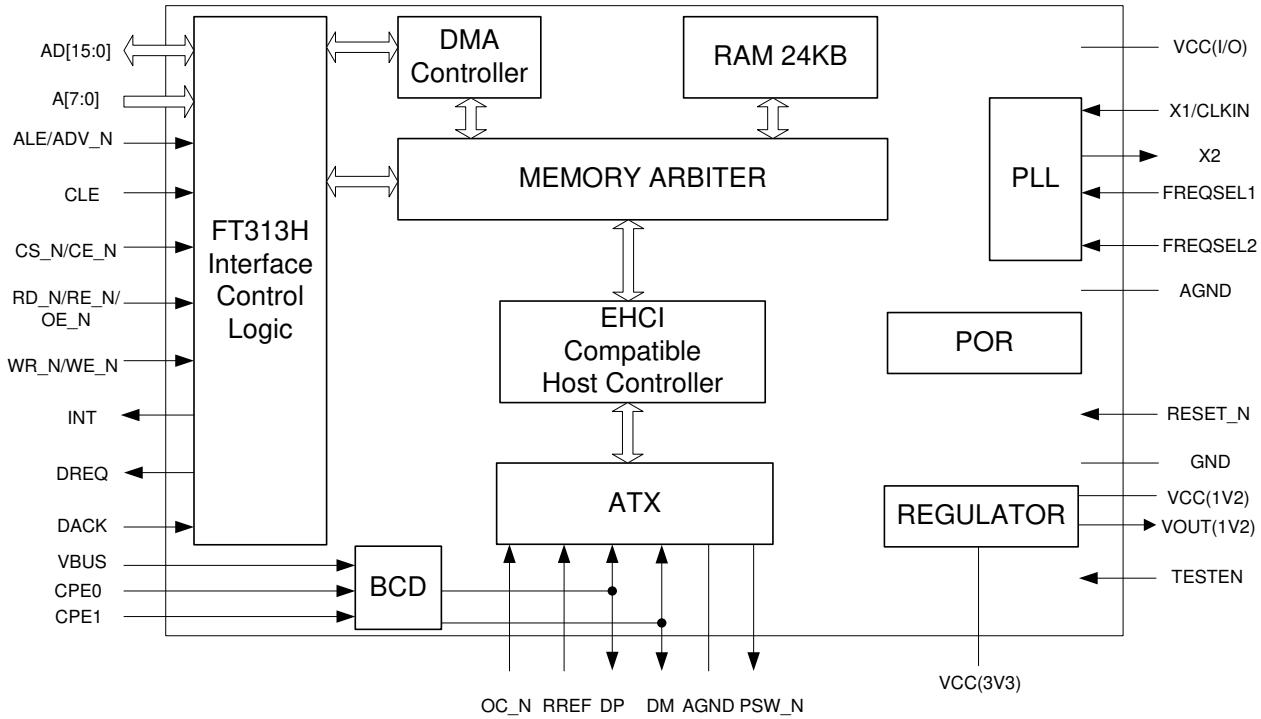

Figure 2-1 FT313H Block Diagram

For a description of each function please refer to Section 4.

Table of Contents

3 Device Pin Out and Signal Description

3.1 Pin Out – 64pin QFN

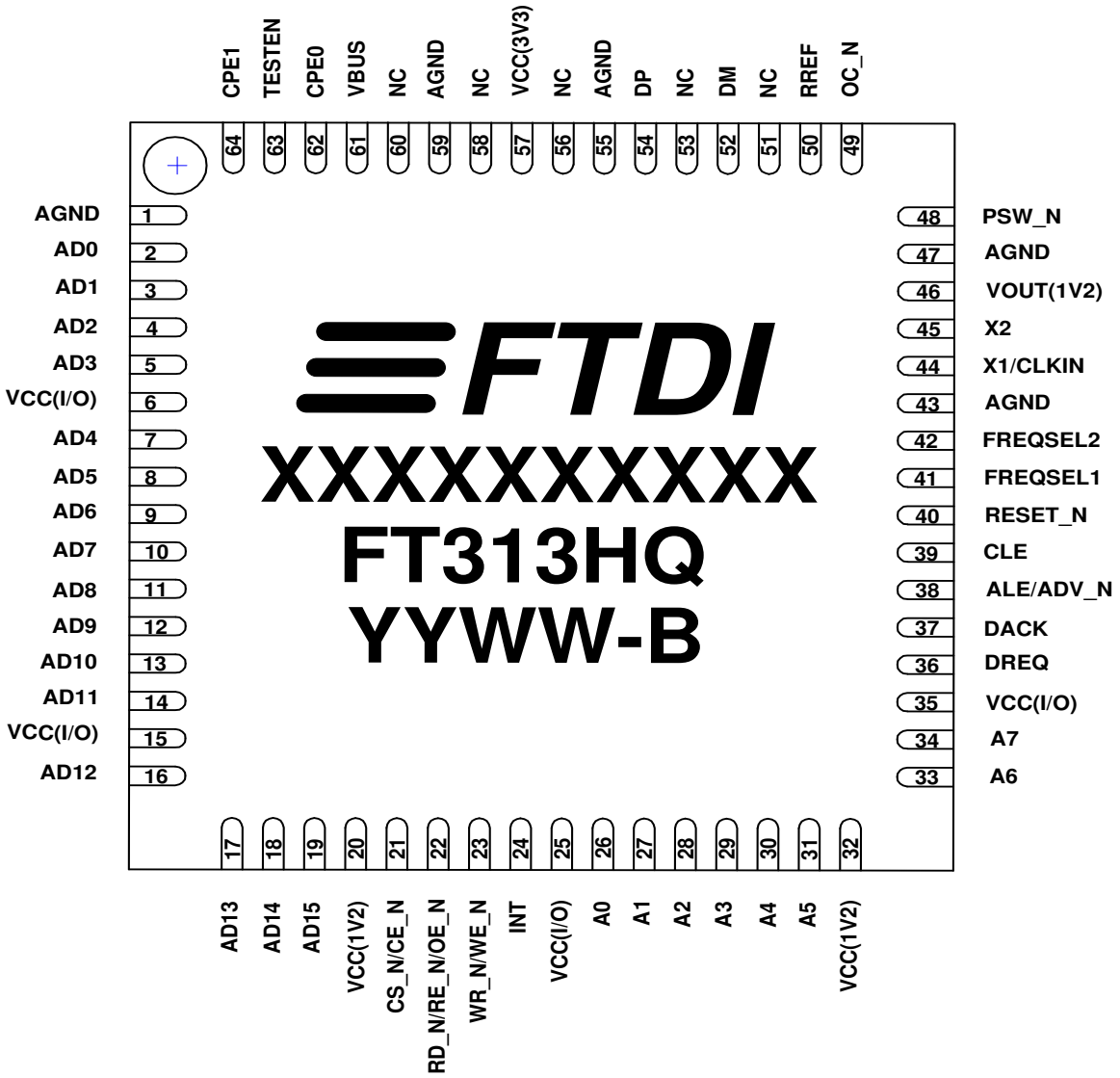

Figure 3-1 Pin Configuration QFN64 (top-down view)

3.2 Pin Out – 64pin LQFP

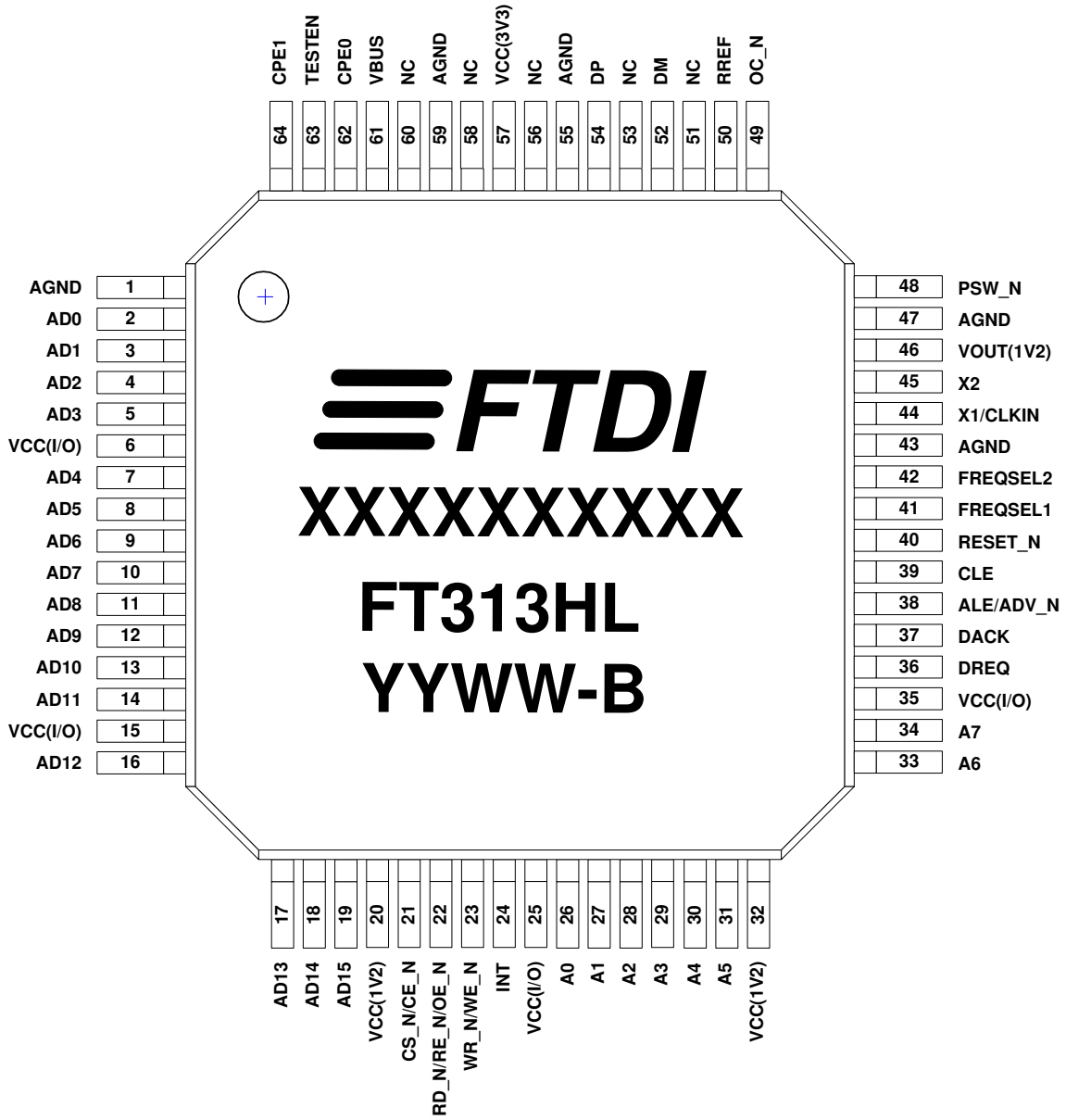

Figure 3-2 Pin Configuration LQFP64 (top-down view)

3.3 Pin Out – 64pin TQFP

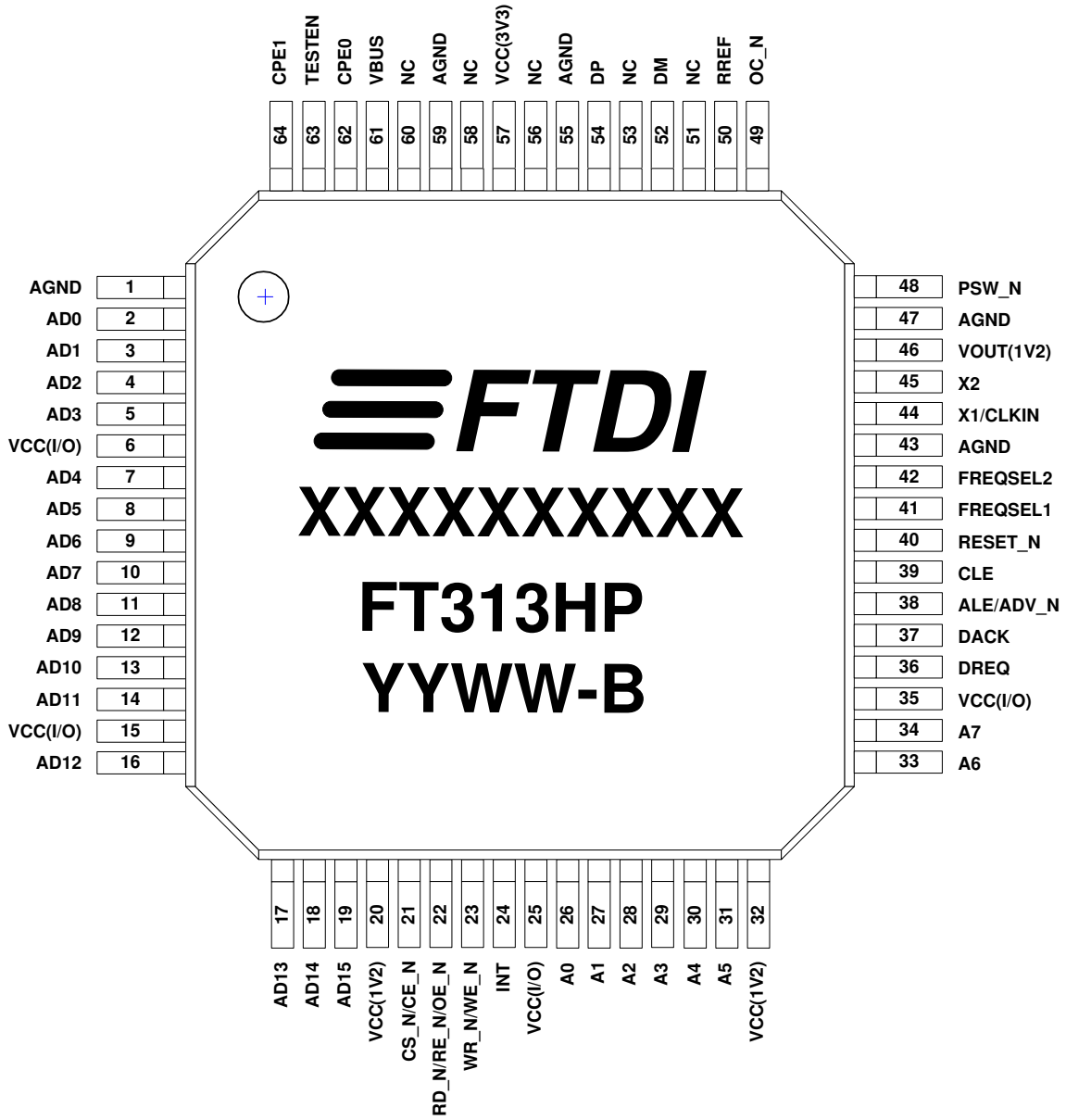

Figure 3-3 Pin Configuration TQFP64 (top-down view)

3.4 Pin Description

Pin No.	Name	Type	Description
1	AGND	P	Analog Ground
2	AD0	I/O	Bit 0 of the address and data bus Bidirectional pad; push-pull, three-state output. 3.3V tolerant
3	AD1	I/O	Bit 1 of the address and data bus Bidirectional pad; push-pull, three-state output. 3.3V tolerant
4	AD2	I/O	Bit 2 of the address and data bus Bidirectional pad; push-pull, three-state output. 3.3V tolerant
5	AD3	I/O	Bit 3 of the address and data bus Bidirectional pad; push-pull, three-state output. 3.3V tolerant
6	VCC(I/O)	P	I/O supply voltage; connect a 0.1uF decoupling capacitor 1.8V, 2.5V or 3.3V
7	AD4	I/O	Bit 4 of the address and data bus Bidirectional pad; push-pull, three-state output. 3.3V tolerant
8	AD5	I/O	Bit 5 of the address and data bus Bidirectional pad; push-pull, three-state output. 3.3V tolerant
9	AD6	I/O	Bit 6 of the address and data bus Bidirectional pad; push-pull, three-state output. 3.3V tolerant
10	AD7	I/O	Bit 7 of the address and data bus Bidirectional pad; push-pull, three-state output. 3.3V tolerant
11	AD8	I/O	Bit 8 of the address and data bus Bidirectional pad; push-pull, three-state output. 3.3V tolerant
12	AD9	I/O	Bit 9 of the address and data bus Bidirectional pad; push-pull, three-state output. 3.3V tolerant
13	AD10	I/O	Bit 10 of the address and data bus Bidirectional pad; push-pull, three-state output. 3.3V tolerant
14	AD11	I/O	Bit 11 of the address and data bus Bidirectional pad; push-pull, three-state output. 3.3V tolerant
15	VCC(I/O)	P	I/O supply voltage; connect a 0.1uF decoupling capacitor

Pin No.	Name	Type	Description
			1.8V, 2.5V or 3.3V
16	AD12	I/O	Bit 12 of the address and data bus Bidirectional pad; push-pull, three-state output. 3.3V tolerant
17	AD13	I/O	Bit 13 of the address and data bus Bidirectional pad; push-pull, three-state output. 3.3V tolerant
18	AD14	I/O	Bit 14 of the address and data bus Bidirectional pad; push-pull, three-state output. 3.3V tolerant
19	AD15	I/O	Bit 15 of the address and data bus Bidirectional pad; push-pull, three-state output. 3.3V tolerant
20	VCC(1V2)	P	Core power 1.2V input; for normal operation, this pin must be connected to pin 46. Connect a 0.1uF decoupling capacitor
21	CS_N/CE_N	I	Chip select; Input ; 3.3V tolerant
22	RD_N /RE_N/OE_N	I	Read enable, or read latch; when not in use, connect to VCC(I/O) Input; 3.3V tolerant
23	WR_N /WE_N	I	Write enable; when not in use, connect to VCC(I/O) Input; 3.3V tolerant
24	INT	O	Interrupt output Push-pull output; 3.3V tolerant
25	VCC(I/O)	P	I/O supply voltage; connect a 0.1uF decoupling capacitor 1.8V, 2.5V or 3.3V
26	A0	I	Bit 0 of the address bus; when not in use, connect to GND Input; 3.3V tolerant
27	A1	I	Bit 1 of the address bus; when not in use, connect to GND Input; 3.3V tolerant
28	A2	I	Bit 2 of the address bus; when not in use, connect to GND Input; 3.3V tolerant
29	A3	I	Bit 3 of the address bus; when not in use, connect to GND Input; 3.3V tolerant

Pin No.	Name	Type	Description
30	A4	I	Bit 4 of the address bus; when not in use, connect to GND Input; 3.3V tolerant
31	A5	I	Bit 5 of the address bus; when not in use, connect to GND Input; 3.3V tolerant
32	VCC (1V2)	P	Core power 1.2V input; for normal operation, this pin must be connected to pin 46. Connect a 0.1uF decoupling capacitor.
33	A6	I	Bit 6 of the address bus; when not in use, connect to GND Input; 3.3V tolerant
34	A7	I	Bit 7 of the address bus; when not in use, connect to GND Input; 3.3V tolerant
35	VCC(I/O)	P	I/O supply voltage; connect a 0.1uF decoupling capacitor 1.8V, 2.5V or 3.3V
36	DREQ	O	DMA request; Push-pull output; 3.3V tolerant
37	DACK	I	DMA acknowledge; Internal pull-down. Input; 3.3V tolerant
38	ALE/ADV_N	I	Address latch enable Input; 3.3V tolerant
39	CLE	I	Command latch enable Input; 3.3V tolerant
40	RESET_N	I	Chip reset; Internal pull-up. Input; 3.3V tolerant
41	FREQSEL1	I	Input clock frequency selection pin1 Input; 3.3V tolerant
42	FREQSEL2	I	Input clock frequency selection pin2 Input; 3.3V tolerant
43	AGND	P	Analog Ground
44	X1/CLKIN	AI	Crystal oscillator or clock input; 3.3V peak input allowed
45	X2	AO	Crystal oscillator output; leave open if an external clock is applied on pin X1/CLKIN
46	VOUT(1V2)	AO	Internal 1.2V regulator output; connect 4.7uF and

Pin No.	Name	Type	Description
			0.1uF decoupling capacitors to this pin.
47	AGND	P	Analog Ground
48	PSW_N	OD	Port power switch; when not in use, connect to VCC(3V3) through a 10kΩ resistor Open drain output; 5V tolerant
49	OC_N	I	Over current input; when not in use, connect to VCC(3V3) through a 10KΩ resistor Input; 5V tolerant
50	RREF	AI	Port reference resistor connection Connect 12 kΩ±1% resistor between RREF and GND
51	NC		No connect
52	DM	AI/O	Port DM; connect to the D- pin of the USB connector
53	NC		No connect
54	DP	AI/O	Port DP; connect to the D+ pin of the USB connector
55	AGND	P	Analog Ground
56	NC		No connect
57	VCC(3V3)	P	Supply 3.3V voltage; Connect 10uF and 0.1uF decoupling capacitors
58	NC		No connect
59	AGND	P	Analog Ground
60	NC		No connect
61	VBUS	OD	VBUS discharge. 5V tolerant
62	CPE0	I	Bit 0 to select charging port emulation type
63	TESTEN	I	Enable test mode. Internal pull-down. For normal operation leave floating.
64	CPE1	I	Bit 1 to select charging port emulation type

Table 3-1 FT313H pin description

Notes:

P : Power or ground
I : Input
O : Output
OD : Open drain output
I/O : Bi-direction Input and Output
AI : Analog Input
AO : Analog Output
AI/O : Analog Input / Output

4 Function Description

The FT313H is a USB2.0 compatible EHCI single port host controller which is mainly composed of the following:

- Microcontroller bus interface
- SRAM bus interface mode
- NOR bus interface mode
- General multiplex bus interface mode
- Interface mode lock
- DMA controller
- EHCI host controller
- System clock
- Power management
- BCD mode

The functions for each block are briefly described in the following subsections.

4.1 Microcontroller Bus Interface

The FT313H has a fast advance general purpose interface to communicate with most types of microcontrollers and microprocessors. This microcontroller interface is configured using pins ALE/ADV_N and CLE to accommodate most types of interfaces. The bus interface supports 8-bit and 16-bit, which can be configured using bit DATA_BUS_WIDTH. Three bus interface types are selected using inputs ALE/ADV_N and CLE during power up, the RD_N /RE_N/OE_N and CS_N/CE_N pins, or the RESET_N pin. Table 4.1 provides detail of bus configuration for each mode. Table 4.2 shows pinout information of each bus interface.

Bus Mode	ALE/ADV_N	CLE	DATA_BUS_WIDTH	Signal Description
SRAM 8-bit	HIGH	HIGH	1	• A[7:0]: 8-bit address bus • AD[7:0]: 8-bit data bus • Write (WR_N), read (RD_N), chip select (CS_N): control signals for normal SRAM mode • DACK: DMA acknowledge input • DREQ: DMA request output
SRAM 16-bit	HIGH	HIGH	0	• A[7:0]: 8-bit address bus • AD[15:0]: 16-bit data bus • Write (WR_N), read (RD_N), chip select (CS_N): control signals for normal SRAM mode • DACK: DMA acknowledge input • DREQ: DMA request output
NOR 8-bit	HIGH	LOW	1	• AD[7:0]: 8-bit data bus • ADV_N, write enable, output enable, chip select: control signals
NOR 16-bit	HIGH	LOW	0	• AD[15:0]: 16-bit data bus • ADV_N, write enable, output enable, chip select: control signals
General Multiplex 8-bit	LOW	HIGH	1	• AD[7:0]: 8-bit data bus • ALE, write(WR_N), read(RD_N), chip

Bus Mode	ALE/ADV_N	CLE	DATA_BUS_WIDTH	Signal Description
				select: control signals • DACK: DMA acknowledge input • DREQ: DMA request output
General Multiplex 16-bit	LOW	HIGH	0	• AD[15:0]: 16-bit data bus • ALE, write(WR_N), read(RD_N), chip select: control signals • DACK: DMA acknowledge input • DREQ: DMA request output

Table 4-1 Bus Configuration modes

SRAM mode	NOR mode	General Multiplex mode	Type	Description
AD[15:0]	AD[15:0]	AD[15:0]	I/O	Data or address bus
A[7:0]	-	-	I	Address bus
-	ADV_N	ALE	I	Address or command valid
CS_N	CS_N	CS_N	I	Chip select
RD_N/RE_N	OE_N	RD_N/RE_N	I	Read control
WR_N/WE_N	WE_N	WR_N/WE_N	I	Write control
INT	INT	INT	O	Interrupt request
DREQ	-	DREQ	O	DMA request
DACK	-	DACK	I	DMA acknowledge

Table 4-2 Pin information of the bus interface

4.2 SRAM bus interface mode

The bus interface will be in SRAM 16-bit mode if pins ALE/ADV_N and CLE are HIGH, when:

- The CS_N/CE_N pin goes LOW, and the RD_N /RE_N/OE_N pin goes LOW.

Then, if the DATA_BUS_WIDTH bit is set, the bus interface will be in SRAM 8-bit mode.

In SRAM mode, A[7:0] is the 8-bit address bus and AD[15:0] is the separate 16-bit data bus. The FT313H pins RD_N /RE_N/OE_N and WR_N/WE_N are the read and write strobes. The SRAM bus interface supports both 8-bit and 16-bit bus width that can be configured by setting or clearing bit DATA_BUS_WIDTH. The DMA transfer is also applicable to this interface.

4.3 NOR bus interface mode

The bus interface will be in NOR 16-bit mode, if pin ALE/ADV_N is HIGH and pin CLE is LOW, when:

- The CS_N/CE_N pin goes LOW, and the RD_N /RE_N/OE_N pin goes LOW.

Then, if the DATA_BUS_WIDTH bit is set, the bus interface will be in NOR 8-bit mode.

The NOR Flash interface access consists of two phases: address and data.

The address is valid when CS_N/CE_N and ADV_N are LOW, and the address is latched at the rising edge of ADV_N. For a read operation, WE_N must be HIGH. OE_N is the data output control. When active, the addressed register or the buffer data is driven to the I/O bus. The read operation is completed when CS_N/CE_N is de-asserted. For a write operation, OE_N must be HIGH. The WE_N assertion can start when ADV_N is de-asserted. WE_N is the data input strobe signal. When de-asserted, data will be written to the addressed register or the buffer. The write operation is completed when CS_N/CE_N is de-asserted.

4.4 General multiplex bus interface mode

The bus interface will be in general multiplex 16-bit mode, if pin ALE/ADV_N is LOW and pin CLE is HIGH, when:

- The CS_N/CE_N pin goes LOW, and the RD_N /RE_N/OE_N pin goes LOW.

Then, if the DATA_BUS_WIDTH bit is set, the bus interface will be in general multiplex 8-bit mode. The general multiplex bus interface supports most advance application processors.

The general multiplex interface access consists of two phases: address and data.

The address is valid when ALE/ADV_N goes HIGH, and the address is latched at the falling edge of ALE/ADV_N. For a read operation, WR_N/WE_N must be HIGH. RD_N /RE_N/OE_N is the data output control. When active, the addressed register or the buffer data is driven to the I/O bus. The read operation is completed when CS_N/CE_N is de-asserted. For a write operation, RD_N /RE_N/OE_N must be HIGH. The WR_N/WE_N assertion can start when ALE/ADV_N is de-asserted. WR_N/WE_N is the data input strobe signal. When de-asserted, data will be written to the addressed register or the buffer. The write operation is completed when CS_N/CE_N is de-asserted. The DMA transfer is also applicable to this interface.

4.5 Interface mode lock

The bus interface can be locked in any of the modes, SRAM, NOR, or general multiplex, using bit 3 of the HW Mode Control register. To lock the interface in a particular mode:

1. Read bits 7 and 6 of the SW Reset register.
2. Set bit 3 of the HW Mode Control register to logic 1.
3. Read bits 7 and 6 of the SW Reset register to ensure that the interface is locked in the desired mode.

Note: the default is 16-bit SRAM mode.

4.6 DMA controller

The DMA controller of the FT313H is used to transfer data between the system memory and local buffers. It shares data bus AD[15:0] and control signals WR_N/WE_N, RD_N /RE_N/OE_N, and CS_N/CE_N. The logic is dependent on the bus interface mode setting.

DREQ signal is from the FT313H to indicate the start of DMA transfer. DACK signal is used to differentiate if data transferred is for the DMA or PIO access. When DACK is asserted, it indicates that it is still in DMA mode. When DACK is de-asserted, it indicates that PIO is to be accessed. ALE/ADV_N and CLE are ignored in a DMA access cycle. Correct data will be captured only on the rising edge of WR_N/WE_N and RD_N /RE_N/OE_N.

The DMA controller of the FT313H has only one DMA channel. Therefore, only one DMA read or DMA write may take place at a time. Assign the DMA transfer length in the Data Session Length register for each DMA transfer. If the transfer length is larger than the burst counter, the DREQ signal will de-assert at the end of each burst transfer. DREQ will re-assert at the beginning of the each burst.

When DMA is transferring data from/to local buffer, if it wants to access local buffer content by PIO mode, can use auxiliary memory access registers AUX_MEMADDR and AUX_DATAPORT to read/write data from/to local buffer with single cycle.

For a 16-bit DMA transfer, the minimum burst length is 2 bytes. This means that the burst length is only one DMA cycle. Therefore, DREQ and DACK will assert and de-assert at each DMA cycle.

The FT313H will be asserted DMA EOT interrupt to indicate that the DMA transfer has either successfully completed or terminated.

4.7 EHCI host controller

The FT313H is a one-port EHCI-compatible host controller which supports all the USB 2.0 compliant Low-speed, Full-speed, and High-speed devices and split/preamble transactions for the HS/FS hub.

The EHCI host controller supports two categories of the transfer types, the periodic and asynchronous transfer types. The periodic transfer type includes the isochronous and interrupt transfers, while the asynchronous transfer type includes the control and bulk transfers.

The EHCI host controller has schedule interface that provides to the separate schedules for each category of the transfer type. The periodic schedule is based on a time-oriented frame list that represents a slide window of time of the host controller work items. All the ISO and INT transfers are serviced via the periodic schedule. The asynchronous schedule is a simple circular list of the schedule work items that provides a round robin service opportunity for all the asynchronous transfers.

The EHCI host controller contains the Isochronous Transfer Descriptor (iTD), Queue Head (qH) and Queue Element Transfer Descriptor (qTD), and Split Transaction Isochronous Transfer Descriptor (siTD) data structure interface to support the isochronous/interrupt/control/bulk transfers and split transaction.

The EHCI host controller internal buffer memory is 24KB. START_ADDR_MEM register is allocated from 0x0000 to 0x5FFF.

4.8 System clock

4.8.1 Phase Locked Loop (PLL) clock multiplier

The internal PLL supports 12MHz, 19.2MHz, or 24MHz input, which can be crystal or a clock already existing in system. The frequency selection can be done using the FREQSEL1 and FREQSEL2 pins. Table 4.3 provides clock frequency selection.

FREQSEL1	FREQSEL2	Clock Frequency
0	0	12MHz
1	0	19.2MHz
0	1	24MHz

Table 4-3 Clock frequency select

4.9 Power management

4.9.1 Power up and reset sequence

When VCC(I/O) and VCC(3V3) are on, an internal regulator will power on with VCC(3V3) on. An internal POR pulse will be generated during the regulator power on, so that internal circuits are in reset state until the regulator power is stable.

4.9.2 Power supply

Power supplies are defined in Table 4.4.

Symbol	Typical	Description
VCC(I/O)	1.8V, or 2.5V, or 3.3V	Supply for digital I/O pad
VCC(3V3)	3.3V	Supply for chip

Table 4-4 Power supply

4.9.3 ATX reference voltage

The ATX circuit provides a stable internal voltage reference (+1.2V) to bias the analog circuitry. This circuit requires an accurate external reference resistor. Connect 12kΩ±1% resistor between pins RREF and GND.

4.9.4 Power modes

Power management configuration defined in Table 4.5.

For each bit description, see CONFIG register.

OSC_EN	PLL_EN	HC_CLK_EN	Description
1	1	1	Operation mode
0	0	0	Suspend mode

Table 4-5 power management configuration

4.9.4.1 Operation mode

All power supplies are present. Host controller is active.

4.9.4.2 Suspend mode

All power supplies are present. Host controller goes to USB suspend.

The steps for the host suspend are as follows:

1. Clear the RS bit of the USBCMD register to stop the host controller from executing schedule.
2. Set the PO_SUSP bit of the PORTSC register to force the host controller to go into suspend.
3. Disable OSC_EN, PLL_EN and HC_CLK_EN bits of the CONFIG register to save power.
4. Clear the U_SUSP_U bit of the EOTTIME register to put the chip into suspend mode.

4.9.4.3 Wake up

The regulator will be in normal operating mode and the clock/oscillator/PLL will be enabled when either of these conditions is triggered:

1. Dummy read access with a LOW pulse on pins CS_N/CE_N and RD_N /RE_N/OE_N.
2. USB device connects or disconnects.
3. Remote wake up from external USB device.
4. Over current condition is triggered on OC_N if enabled by register.

After wake up automatically set corresponding bit of the CONFIG register, must set the U_SUSP_U bit of the EOTTIME register to wake up the chip.

4.10 BCD mode

The FT313H is an EHCI-compatible host controller with BCD block function, which follows the Battery Charging Specification Revision 1.2(BC1.2) by USB-IF. The block function that emulates USB host port as either Charging Downstream Port (CDP) or Dedicated Charging Port (DCP) which provides higher current source than Standard Downstream Port (SDP).

The BCD logic block will decode the mode of operation and choose by following setting:

1. BCD function is default enable by CONFIG register bit[5] setting.
2. BCD mode selection is default controlled by external pins configuration. Set CONFIG register bit[15] to take over BCD mode setting by software.
3. Same configuration by CONFIG register bit[14:13] to set BCD mode if software takes over control.

CPE1	CPE0	Mode	BCD_EN	Description
0	0	SDP	1	Standard downstream port, VBUS current limit ≤ 500mA
0	1	DCP	1	Dedicated charging port, USB host no functional on this port, VBUS current limit ≤ 1.5A
1	1	CDP	1	Charging downstream port alternative configuration, VBUS current limit ≤ 1.5A
X	X	X	0	BCD function disable

Table 4-6 BCD mode configuration

5 Host controller specific registers

5.1 Overview of registers

Table 5.1 shows the definitions of the FT313H host controller specific registers.

Address	Register	Reset value	Description
EHCI operational register			
00h	HCCAPLENGTH	0100 0010h	Capability register
04h	HCSPARAMS	0000 0001h	Structural parameter register
08h	HCCPARAMS	0000 0006h	Capability parameter register
10h	USBCMD	0008 0B00h	USB command register
14h	USBSTS	0000 1000h	USB status register
18h	USBINTR	0000 0000h	USB interrupt enable register
1Ch	FRINDEX	0000 0000h	Frame index register
24h	PERIODICLISTADDR	0000 0000h	Periodic frame list base address register
28h	ASYNCLISTADDR	0000 0000h	Current asynchronous list address register
30h	POSTSC	0000 0000h	Port status and control register
Configuration register			
34h	EOFTIME	0000 0041h	EOF time and asynchronous schedule sleep timer register
80h	CHIPID	0313 0001h	Chip ID register
84h	HWMODE	0000 0000h	HW mode control register
88h	EDGEINTC	0000 001Fh	Edge interrupt control register
8Ch	SWRESET	0000 0000h	SW reset register
90h	MEMADDR	0000h	Memory address register
92h	DATAPORT	0000h	Data port register
94h	DATASESSION	0000h	Data session length register
96h	CONFIG	1FA0h	Configuration register
98h	AUX_MEMADDR	0000h	Auxiliary memory address register
9Ah	AUX_DATAPORT	0000h	Auxiliary data port register
9Ch	SLEEPTIMER	0400h	Sleep timer register
Interrupt register			
A0h	HCINTSTS	0000h	Host controller interrupt status register

Address	Register	Reset value	Description
A4h	HCINTEN	0000h	Host controller interrupt enable register
USB testing register			
50h	TESTMODE	0000 0000h	Test mode register
70h	TESTPMSET1	0000 0000h	Test parameter setting 1 register
74h	TESTPMSET2	0000 0000h	Test parameter setting 2 register

Table 5-1 Overview of host controller specific registers

5.2 EHCI operational registers

5.2.1 HCCAPLENGTH register (address = 00h)

This register is used as an offset to add to register base to find the beginning of the operational register space. The high two bytes contain a BCD encoding of the EHCI revision number supported by this host controller. The most signification byte of this register represents a major revision and the least signification byte is the minor revision.

Bit	Name	Type	Default value	Description
[31:16]	HCIVERSION	RO	16'h0100	**Host Controller Interface Version Number** This register is a 2-byte register containing a BCD encoding of the EHCI revision number supported by the host controller.
[15:8]	Reserved	RO	8'h0	-
[7:0]	CAPLENGTH	RO	8'h10	**Capability Register Length** This register is used as an offset added to register base to find out the beginning of the Operational Register Space.

Table 5-2 Capability register

5.2.2 HCSPARAMS register (address = 04h)

This is a set of fields that are structural parameter: number of downstream ports, etc.

Bit	Name	Type	Default value	Description
[31:4]	Reserved	RO	28'h0	-
[3:0]	N_PORTS	RO	4'h1	**Number of Ports** This field specifies the number of the physical downstream ports implemented on the host controller.

Table 5-3 Structural parameter register

5.2.3 HCCPARAMS register (address = 08h)

This is multiple mode control (time base bit functionality) and addressing capability.

Bit	Name	Type	Default value	Description
[31:3]	Reserved	RO	29'h0	-
2	ASPC	RO	1'b1	**Asynchronous Schedule Park Capability** The host controller supports the park feature for high-speed queue heads in the Asynchronous Schedule. This feature can be disabled or enabled and set to a specific level by using the *Asynchronous Schedule Park Mode Enable* and *Asynchronous Schedule Park Mode Count* fields in the USBCMD register.
1	PFLF	RO	1'b1	**Programmable Frame List Flag** When this bit is set to 1b, the system software can specify and use a smaller frame list and configure the host controller via *Frame List Size* field of the USBCMD register. This requirement ensures that the frame list is always physically contiguous.
0	Reserved	RO	1'b0	-

Table 5-4 Capability parameter register

5.2.4 USBCMD register (address = 10h)

The command register indicates the command to be executed by the serial bus host controller. Writing to the register causes a command to be executed.

Bit	Name	Type	Default value	Description
[31:24]	Reserved	RO	8'h0	-
[23:16]	INT_THRC	R/W	8'h08	**Interrupt Threshold Control** This field is used by the system software to select the maximum rate at which the host controller will issue the interrupts. The only valid values are described as below: Value Max Interrupt Interval for the high-speed 00h Reserved 01h No limited interval 02h 2 micro-frames 04h 4 micro-frames 08h 8 micro-frames (Default, equals to 1 ms) 10h 16 micro-frames (2 ms) 20h 32 micro-frames (4 ms) 40h 64 micro-frames (8 ms)

Bit	Name	Type	Default value	Description
				Note1: This is further gated by MIN_WIDTH bits of EDGEINTC register if edge trigger interrupt is used. Note2: In the full-speed mode, these registers are reserved.
[15:12]	Reserved	RO	4'b0	-
11	ASYN_PK_EN	R/W	1'b1	**Asynchronous Schedule Park Mode Enable** Software uses this register to enable or disable the Park mode. When this register is set to '1', the Park mode is enabled.
10	Reserved	RO	1'b0	-
[9:8]	ASYN_PK_CNT	R/W	2'b11	**Asynchronous Schedule Park Mode Count** This field contains a count for the number of successive transactions that the host controller is allowed to execute from a high-speed queue head on the asynchronous schedule.
7	Reserved	RO	1'b0	-
6	INT_OAAD	R/W	1'b0	**Interrupt on Asynchronous Advance Doorbell** This bit is used as a doorbell by software to ring the host controller to issue an interrupt at the next advance of the asynchronous schedule.
5	ASCH_EN	R/W	1'b0	**Asynchronous Schedule Enable** This bit controls whether the host controller skips the processing of asynchronous schedule. 0: Do not process the asynchronous schedule 1: Use the ASYNCLISTADDR register to access the asynchronous schedule
4	PSCH_EN	R/W	1'b0	**Periodic Schedule Enable** This bit controls whether the host controller skips the processing of the periodic schedule. 0: Do not process the periodic schedule 1: Use the PERIODICKISTBASE register to access the periodic schedule
[3:2]	FRL_SIZE	R/W	2'b00	**Frame List Size** This field specifies the size of the frame list. 00: 1024 elements (4096 bytes; default value) 01: 512 elements (2048 bytes) 10: 256 elements (1024 bytes) 11: Reserved
1	HC_RESET	R/W	1'b0	**Host Controller Reset** This control bit is used by the software to reset the host controller.

Bit	Name	Type	Default value	Description
0	RS	R/W	1'b0	**Run/Stop** When this bit is set to 1b, the host controller proceeds with the execution of schedule. 0: Stop 1: Run

Table 5-5 USB command register

5.2.5 USBSTS register (address = 14h)

This register indicates pending interrupts and various states of the Host Controller. The status resulting from a transaction on the serial bus is not indicated in this register. Software sets a bit to 0 in this register by writing a 1 to it.

Bit	Name	Type	Default value	Description
[31:16]	Reserved	RO	16'h0	-
15	ASCH_STS	RO	1'b0	**Asynchronous Schedule Status** This bit reports the actual status of the asynchronous schedule.
14	PSCH_STS	RO	1'b0	**Periodic Schedule Status** This bit reports the actual status of the periodic schedule.
13	Reclamation	RO	1'b0	**Reclamation** This is a read-only status bit, and used to detect an empty of the asynchronous schedule.
12	HCHalted	RO	1'b1	**Host Controller Halted** This bit is a zero whenever the Run/Stop bit is set to '1.' The host controller sets this bit to '1' after it has stopped the executing as a result of the Run/Stop bit being set to 0b.
[11:6]	Reserved	RO	6'b0	-
5	INT_OAA	R/WC	1'b0	**Interrupt on Asynchronous Advance** This status bit indicates the assertion of *interrupt on Async Advance Doorbell*.
4	H_SYSERR	R/WC	1'b0	**Host System Error** The Host Controller sets this bit to '1' when a serious error occurred during a host system access involving the host controller module.
3	FRL_ROL	R/WC	1'b0	**Frame List Rollover** The host controller sets this bit to '1' when the *Frame List Index* rolls over from its maximum value to zero.
2	PO_CHG_DET	R/WC	1'b0	**Port Change Detect** The host controller sets this bit to '1' when any port has a change bit transition from '0' to '1.' In addition, this bit is loaded with the OR of all of

Bit	Name	Type	Default value	Description
				the PORTSC change bits.
1	USBERR_INT	R/WC	1'b0	**USB Error Interrupt** The host controller sets this bit to '1' when the completion of a USB transaction results in an error condition.
0	USB_INT	R/WC	1'b0	**USB Interrupt** The host controller sets this bit to '1' upon the completion of a USB transaction.

Table 5-6 USB status register

5.2.6 USBINTR register (address = 18h)

This register enables and disables reporting of the corresponding interrupt to the software. When a bit is set and the corresponding interrupt is active, an interrupt is generated to the host. Interrupt sources that are disabled in this register still appear in the USBSTS to allow the software to poll for events.

Bit	Name	Type	Default value	Description
[31:6]	Reserved	RO	26'h0	-
5	INT_OAA_EN	R/W	1'b0	**Interrupt on Async Advance Enable** When this bit is set to '1,' and the *Interrupt on Async Advance* bit in the USBSTS register is set to '1' also, the host controller will issue an interrupt at the next interrupt threshold.
4	H_SYSERR_EN	R/W	1'b0	**Host System Error Enable** When this bit is set to '1,' and the *Host System Error Status* bit in the USBSTS register is set to '1' also, the host controller will issue an interrupt.
3	FRL_ROL_EN	R/W	1'b0	**Frame List Rollover Enable** When this bit is set to '1,' and the *Frame List Rollover* bit in the USBSTS register is set to '1' also, the host controller will issue an interrupt.
2	PO_CHG_DET_EN	R/W	1'b0	**Port Change Interrupt Enable** When this bit is set to '1,' and the *Port Change Detect* bit in the USBSTS register is set to '1' also, the host controller will issue an interrupt.
1	USBERR_INT_EN	R/W	1'b0	**USB Error Interrupt Enable** When this bit is set to '1,' and the USBERRINT bit in the USBSTS register is set to '1' also, the host controller will issue an interrupt at the next interrupt threshold.
0	USB_INT_EN	R/W	1'b0	**USB Interrupt Enable** When this bit is set to '1,' and the USBINT bit in the USBSTS register is a set to '1' also, the host controller will issue an interrupt at the next interrupt threshold. If set interrupt threshold to 01h, means that when interrupt event occurred, the INT signal will be toggled at once.

Table 5-7 USB interrupt enable register