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Future Technology Devices International Ltd.

FT4222H

(USB2.0 to QuadSPI/I²C Bridge IC)

FT4222H is a USB2.0 to Quad-SPI/I²C interface Device Controller with the following advanced features:

- Single chip USB2.0 Hi-speed to SPI/I²C bridge with a variety of configurations
- Entire USB protocol handled on the chip.
- On-chip OTP memory for USB Vendor ID (VID), Product ID (PID), device serial number, product description string and various other vender specific data.
- Configurable industry standard SPI Master/Slave interface controller
- Support configurable data width with single, dual, quad data width transfer mode in SPI master
- SCK can support up to 30MHz in SPI master
- Up to 53.8Mbps data transfer rate in SPI master with quad mode transfer
- Support single bit data transfer with full-duplex transfer in SPI Slave
- Support up to 4 channels slave selection control pins in SPI master application
- Configurable I²C Master/Slave interface controller conforming to I²C v2.1 and v3.0 specification.
- Support 4 speed modes as defined in the I²C-bus Specification, standard mode (SM) up to 100Kbit/s, fast mode (FM) up to 400Kbit/s, Fast mode plus (FM+) up to 1Mbit/s, and High Speed mode (HS) up to 3.4 Mbit/s
- Configurable GPIOs can be easily controlled by software applications via USB bus
- USB Battery Charger Detection.
- Device supplied pre-programmed with unique USB serial number.
- USB Power Configurations; supports bus-powered, self-powered and bus-powered with power switching.
- +5V USB VBUS detection engine
- Integrated 5V-3.3V-1.8V regulators.
- True 3.3V CMOS drive output and TTL input. (operates down to 1V8 with external pull-ups)
- Configurable I/O pin output drive strength; 4 mA(min) and 16 mA(max)
- Integrated power-on-reset circuit.
- USB2.0 Low operating and suspend current; 68mA (active-typ) and 375µA (suspend-typ).
- UHCI / OHCI / EHCI / XHCI host controller compatible.
- FTDI's royalty-free Direct (D2XX) drivers for Windows eliminate the requirement for USB driver development in most cases.
- Extended operating temperature range; -40ºC to 85ºC.
- Available in compact Pb-free 32 Pin VQFN packages (RoHS compliant).

1 Typical Applications

- USB to single mode SPI master controller
- USB to dual mode SPI master controller
- USB to quad mode SPI master controller
- USB to single SPI slave controller
- USB to I^2C master interface controller
- USB to I^2C slave interface controller
- Utilising USB to add system modularity
- Incorporate USB interface to enable PC transfers for development system communication
- USB Industrial Control
- USB Data Acquisition
- Accessory connectivity solutions for mobiles and tablets
- USB dongle implementations for Software/ Hardware Encryption and Wireless Modules
- Detect USB dedicated charging ports, to allow for high current battery charging in portable devices.

1.1 Driver Support

Royalty free D2XX *Direct* Drivers (USB Drivers + DLL S/W Interface)

- Windows 10 32, 64-bit
- Windows 8.1 32, 64-bit
- Windows 8 32, 64-bit
- Windows 7 32, 64-bit
- Server 2008 R2
- Server 2012 R2
- Linux
- Android

For driver installation, please refer to http://www.ftdichip.com/Documents/InstallGuides.htm

1.2 Ordering Information

Part Number	Package	Remark
FT4222HQ-C-x	32 Pin VQFN	Rev C

Note: Packing codes for x is:

- R: Taped and Reel, 5,000pcs per reel

- T: Tray packing, 490pcs per tray

For example: FT4222HQ-C-T is 490pcs tray packing (rev C)

1.3 USB Compliant

The FT4222H is fully compliant with the USB 2.0 specification and has been given the USB-IF Test-ID (TID) 40001599.

2 FT4222H Block Diagram

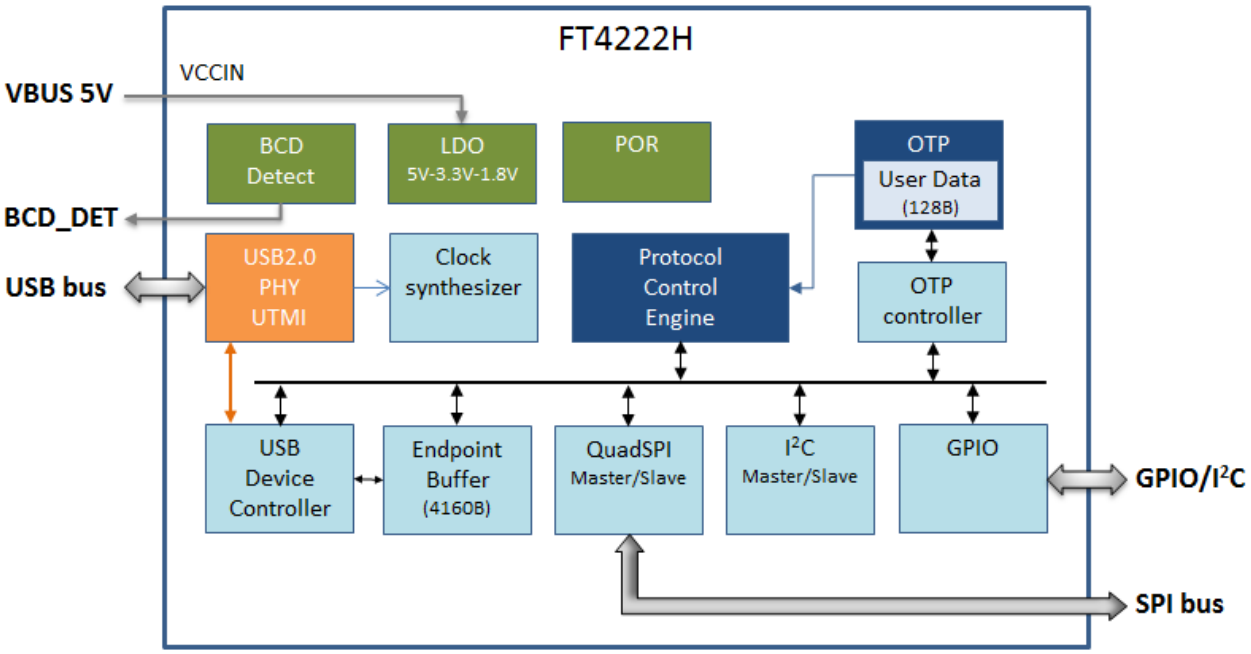

Figure 2.1 FT4222H Block Diagram

For a description of each function please refer to Section 4.

Table of Contents

3 Device Pin Out and Signal Description

3.1 VQFN-32 Package Pin Out

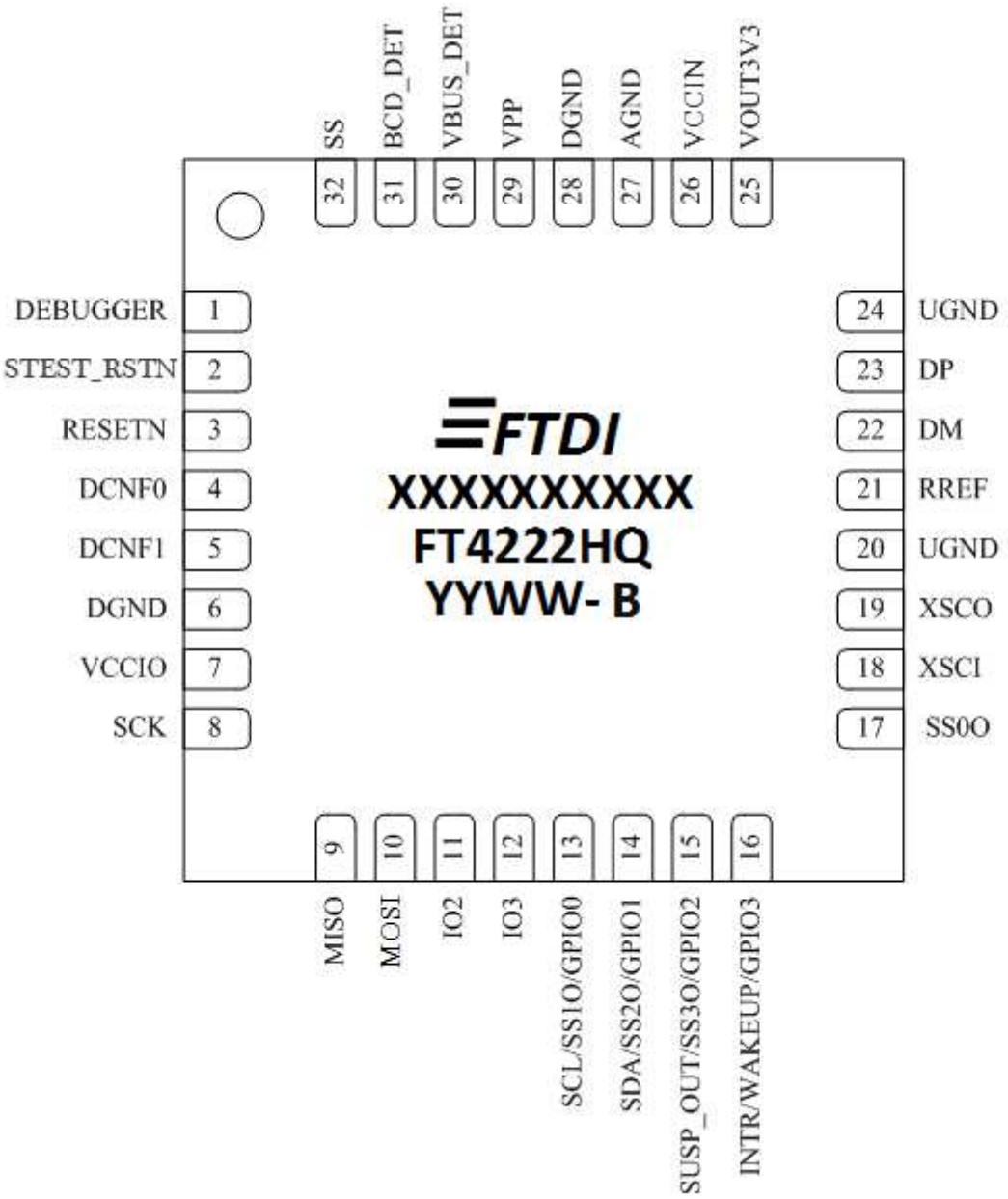

Figure 3.1 Pin Configuration VQFN-32 (top-down view)

3.2 Pin Description

FT4222H Pin No.	Pin Name	Type	Description
1	DEBUGGER	I/O	Debugging pin. Should be reserved and tied to high
2	STEST_RSTN	I	Chip reset input for test mode. Active low. Should be reserved and tied to high.
3	RESETN	I	Chip reset input for non-test mode operation. Active low.
4	DCNF0	I	Chip mode configuration selection bit 0. Refer to Section 5.1
5	DCNF1	I	Chip mode configuration selection bit 1. Refer to Section 5.1
6	DGND	P	Digital Ground
7	VCCIO	** P	+3.3V/2.5V/1.8V supply voltage. This is the supply voltage for all the I/O ports. This pin shall be connected to pin 25 when I/O ports are working at 3.3V
8	SCK	I/O	SPI interface clock. Serial clock output for SPI master; serial clock input for SPI slave mode
9	MISO	I/O	In SPI master single mode, it is master serial data input. In SPI master dual/quad mode, it is SPI data bus bit 1. In SPI slave mode, it is slave serial data output.
10	MOSI	I/O	In SPI master single mode, it is master serial data output. In SPI master dual/quad mode, it is SPI data bus bit 0. In SPI slave mode, it is slave serial data input.
11	IO2	I/O	Quad SPI data bus bit 2
12	IO3	I/O	Quad SPI data bus bit 3
13	GPIO0/SS1O/SCL	I/O	GPIO 0 (default) can be configured as slave selection 1, output pin for SPI master mode or serial clock for I^2C mode
14	GPIO1/SS2O/SDA	I/O	GPIO 1 (default) can be configured as slave selection 2, output pin for SPI master mode or serial data for I^2C mode
15	GPIO2/SS3O/SUSP_OUT	I/O	GPIO 2 (default) can be configured as slave selection 3, output pin for SPI master mode or USB suspend output indicator
16	GPIO3/WAKEUP/INTR	I/O	GPIO 3 (default) and can be configured as USB remote wakeup input pin or interrupt input
17	SS0O	O	Slave selection 0, output pin for SPI master mode.
18	XSCI	AI	Crystal oscillator input, 12MHz only. Related application circuit can be referred to in Section7.4
19	XSCO	AO	Crystal oscillator output, 12MHz only. Related application

FT4222H Pin No.	Pin Name	Type	Description
			circuit can be referred to in Section7.4
20	UGND	P	USB Analog Ground
21	RREF	AI	USB peripheral reference voltage input. Connect 12Kohm +/- 1% resistor to GND.
22	DM	AI/O	USB peripheral bidirectional DM line.
23	DP	AI/O	USB peripheral bidirectional DP line.
24	UGND	P	USB Analog Ground
25	VOUT3V3	** P	+3.3V voltage Out May be used to power VCCIO. When VCCIN is supplied with 3.3V, this pin is a power input pin. Connect to pin 26.
26	VCCIN	** P	+5.0V(or 3.3V) supply voltage In Power source-in to embedded regulator.
27	AGND	P	Analog Ground
28	DGND	P	Digital Ground
29	VPP	P	+6.5V supply voltage In Power source for Programming embedded OTP. It should be kept floating or 0V when not in programming mode
30	VBUS_DET	I	VBUS detection input. It is a +5.0V tolerant pin
31	BCD_DET	O	Battery charger detection indicator output when the device is connected to a dedicated battery charger port. Polarity can be defined
32	SS	I	SPI slave selection indicator from SPI master. This pin is active in SPI slave mode. It must be tied to high when SPI master mode enabled.

Table 3.1 FT4222H Pin Description

**If VCCIN is supplied with 3.3V power input, then VOUT3V3 and VCCIO must also be driven with this 3.3V power source

4 Function Description

The FT4222H is a Hi-Speed USB2.0-to-Quad SPI/ I^2C device controller in a compact 32-pin VQFN package. The FT4222H requires an external Crystal (12 MHz) for the internal PLL to operate. It supports multi-voltage IO, 3.3V, 2.5V or 1.8V. It also provides 128 bytes one-time-programmable (OTP) memory space for storing vendor specific information.

The FT4222H contains SPI/ I^2C configurable interfaces. The SPI interface can be configured in master mode with single, dual, or quad bits data width transfer or in slave mode with single bit data width transfer. The I^2C interface can be configured in master or slave mode.

4.1 Key Features

Functional Integration. The FT4222H is a USB 2.0 Hi-Speed (480Mbits/s) to flexible and configurable SPI or I^2C interfaces IC. The FT4222H includes an integrated +1.8V and +3.3V Low Drop-Out (LDO) regulator and 12MHz to 480MHz PLL. It also includes Power-On-Reset (POR), VBUS detection with 5V-tolerance and 128 bytes one-time-programmable(OTP) memory which simplify external circuit design and reduce external component count.

USB2.0 Hi-Speed Device Controller. The FT4222H integrates a USB protocol engine which controls the physical Universal Transceiver Macrocell Interface (UTMI) and handles all aspects of the USB 2.0 Hi-Speed interface. It contains one control endpoint, and 4-pairs of IN and OUT endpoints. These endpoints can implement up to 4 independent interfaces/applications mapped to combined I^2C, GPIO, SPI interfaces.

Highly Integrated USB2.0 to Configurable SPI Bridge. The FT4222H provides the bridge function between a USB2.0 device, upstream port and an SPI Master/Slave.

A support library, LibFT4222, based on FTDI's D2XX driver, enables easy configuration of the SPI as a master or slave. Operating clock frequency on the SPI bus, clock phase and polarity, transfer data bit width mode, and the number of slave selection controls are also configurable.

The maximum SPI interface operating clock can be set up to 40MHz in master mode and 20MHz in slave mode. With quad mode (4-bits) data bus width, the max data transfer throughput can be up to 53.8Mbps.

USB to Configurable I^2C Controller. The FT4222H also provides the bridge function between a USB2.0 device upstream port and an I^2C Master/Slave interface.

A support library, LibFT4222, based on FTDI's D2XX driver, enables easy configuration of the I^2C as either a master or slave, including target operating speed and bus protocol on the I^2C bus.

The device can run at common I^2C bus speeds, standard mode (SM), fast mode (FM), Fast mode plus (FM+), and High Speed mode (HS). A higher bit rate on the I^2C bus is also configurable up to 6.66Mbit/s. Clock stretching is supported to conform to v2.1 and v3.0 of the I^2C specification.

Configurable GPIOs. There are 4 GPIO pins in the FT4222H that can be configured for different purposes, such as a suspend indicator output, remote wake up input, an interrupt input or general purpose Input/Output. These GPIOs can be easily initialized and fully controlled at the USB host side by the application programming interface (API) defined in LibFT4222.

Signal drive strength and slew rate of these GPIOs can be configured via the FT_Prog utility for different design needs.

Embedded OTP memory. The internal OTP memory in the FT4222H is used to store USB Vendor ID (VID), Product ID (PID), device serial number, product description string and various other USB configuration descriptors. With this embedded OTP memory, the device can store vendor specific information and save the cost on BOM. The descriptors can be programmed using the FTDI utility software called FT_PROG, which can be downloaded from the FTDI Utilities page on the FTDI website (http://www.ftdichip.com/Support/Utilities.htm#FT_Prog).

Power management. USB 2.0 suspend/resume and remote wakeup are fully supported. The PHY will be put to a power saving mode and the clock to most of the digital circuits will be stopped when the device is suspended.

Source Power and Power Consumption. The FT4222H is capable of operating at a voltage supply of +3.3V or +5.0V with a nominal operational mode current of 68mA and a nominal USB suspend mode current of 375μA. This allows greater margin for peripheral designs to meet the USB suspend mode current limit of 2.5mA. An integrated level converter within the FT4222H allows the device to interface with logic running at +1.8V, +2.5V or +3.3V. (Note: External pull-ups are recommended for IO <3V3).

4.2 Functional Block Descriptions

The following paragraphs detail each function within the FT4222H. Please refer to the block diagram shown in **Figure 2.1**

USB2.0 UTMI PHY. The Universal Transceiver Macrocell Interface (UTMI) is a physical interface cell. This block handles the full speed and high speed SERDES (serialise - deserialise) function for the USB TX/RX data. It also provides the clocks for the rest of the chip. A 12 MHz crystal should be connected to the XSCI and XSCO pins. A 12k Ohm resistor should be connected between REF and GND on the PCB.

The UTMI PHY functions include:

- Supports 480 Mbit/s "Hi-Speed" (HS) and 12 Mbit/s "Full Speed" (FS).
- SYNC/EOP generation and checking.
- Data and clock recovery from a serial stream on the USB.
- Bit-stuffing/unstuffing; bit stuff error detection.
- Manages USB Resume, Wake Up and Suspend functions.

Single parallel data clock output with on-chip PLL to generate higher speed serial data clocks

USB Device Controller. The USB Device controller in the FT4222H controls and manages the interface between the UTMI PHY and the interfaces of the chip. It provides 9 endpoints to fit into the FT4222H applications.

The USB Device Controller function includes:

- Endpoint-0 for a control pipe with max packet size 64 Bytes
- 4 endpoints for bulk-in pipe with configurable max packet size up to 512 Bytes
- 4 endpoints for bulk-out pipe with configurable max packet size up to 512 Bytes
- Multiple interfaces configuration support
- Suspend detection and power management
- Remote wake-up support
- Fully compatible to USB2.0 specification requirement

Endpoint Buffer. For fulfilling the max packet size requirement and high performance data transfer throughput, the Endpoint Buffer is 4160 bytes SRAM with configurable size management to each endpoint. It can be configured as single or double buffers and adjustable size for each endpoint.

QuadSPI Master/Slave Controller. The QuadSPI is a fully configurable SPI master/slave device, which allows the user to configure polarity and phase of the serial clock signal SCK. When SPI is configured as a master, it can be configured automatically to drive slave select outputs (SS3O – SS0O), and address the SPI slave device to exchange serially shifted data. The data bus can be configured as single (1bit), dual (2-bits) and quad (4-bits) mode for different transfer requests and applications. The interface operating clock can be easily configured up to 30MHz. When SPI is configured as a slave, the SPI engine can support one slave port and operate a single data mode transfer. The max acceptable operating clock can be up to 20MHz. The QuadSPI controller can be configured via a support library, LibFT4222. For details refer to the User Guide For LibFT4222.

QuadSPI as master functions include:

- Single Mode (1-bit) data transfer with full duplex serial data transfer
- Dual Mode (2-bit) data transfer
- Quad Mode (4-bit) data transfer
- Up to 4 SPI slave channels can be addressed via pins SS3O~SS0O
- Shared data bus to minimize related pin counts
- 4 types of transfer format can be selected by Phase and Polarity
- Configurable interface clock on SCK as 1/2, 1/4, 1/8, 1/16, 1/32, 1/64, 1/128, 1/256 of 80MHz, 60MHz,48MHz and 24MHz

SCK Freq. (Hz)		SCK = Operating Clock * the following ratio							
Operating Clock	Max Throughput can be expected	1/2	1/4	1/8	1/16	1/32	1/64	1/128	1/256
80MHz	53.8Mbps*	40M*	20M*	10M	5M	2.5M	1.25M	625K	312.5K
60MHz	39.7Mbps*	30M*	15M	7.5M	3.75M	1.875M	937.5K	468.75K	234.375K
48MHz	31.5Mbps*	24M*	12M	6M	3M	1.5M	750K	375K	187.5K
24MHz	15.8Mbps*	12M*	6M	3M	1.5M	750K	375K	187.5K	93.75K

Table 4.1 SCK Operating Frequency in SPI Master Mode

*The max. throughput can be expected under the condition of quad mode transfers on FT4222H-C with a high operating frequency on SCK. It also depends on the USB bus transfer condition. For example, the max throughput that can be expected is up to 53.8Mbps when the operating clock is equal to 80MHz, SCK is set as 20MHz or 40MHz, the data bus is operating in quad mode and the USB bus is operating at hi-speed USB rates with sufficient bandwidth. The performance for FT4222H-B and FT4222H can be referred to TN_170_FT4222H_Rev.C_Technical_Note.PDF

QuadSPI as slave functions include:

- Single Mode (1-bit) data transfer with full duplex serial data transfer
- Can accept SCK operating frequency up to 20 MHz

Operating Clock Frequency	**Max Acceptable Frequency on SCK**
80MHz	<= 20MHz
60MHz	<= 15MHz
48MHz	<= 12MHz
24MHz	<= 6MHz

Table 4.2 Max. Acceptable Operating Frequency on SCK in SPI Slave Mode

I²C Master/Slave Controller. I²C (Inter Integrated Circuit) is a multi-master serial bus invented by Philips. I²C uses two bi-directional open-drain wires called serial data (SDA) and serial clock (SCL). Common I²C bus speeds are the standard mode (SM) with bit rate up to 100 kbit/s, fast mode (FM) with the bit rate up to 400 kbit/s, Fast mode plus (FM+) with the bit rate up to 1 Mbit/s, and High Speed mode (HS) with the bit rate up to 3.4 Mbit/s. Refer to the I²C specification for more information on the protocol.

The FT4222H device can operates as master or slave, and the major functions include:

- Master or slave mode configurable
- Fully compatible to v2.1 and v3 specification
- 7-bit address support
- Support 4 speed configurations defined in I²C-bus specification
- Support bit rate up to 6.66Mbit/s both in master and slave mode
- Clock stretching support in master and slave mode

GPIOs. FT4222H contains 4 GPIO pins for various functions. The drive strength, slew rate control and pull high/low resistors can be configured in the vendor configurable area of the OTP via FT_PROG. When the USB GPIO interface is enabled and supported, GPIOs can be directly controlled by APIs (Application Programming Interface) which are defined in the support library, LibFT4222, to match the requirement.

GPIOs in the FT4222H functions include:

- GPIO0 can be configured as GPIO0 or I²C SCL or SPIM slave selection SS1O

- GPIO1 can be configured as GPIO1 or I^2C SDA or SPIM slave selection SS2O
- GPIO2 can be configured as GPIO2 or USB suspend status output(SUSP) or SPIM slave selection SS3O
- GPIO3 can be configured as GPIO3 or USB remote wake-up input(WAKE) or external interrupt input(INTR)
- Adjustable Driving Strength : 4mA/8mA/12mA/16mA
- Slew Rate, Pull High/Low resistor, open drain configurable
- WAKE can be configured as rising or falling edge triggered
- SUSP trigger mode can be configured as rising edge, falling edge, high level and low level trigger

For configuration details refer to Section 9.1.

Built-in Clock Synthesizer. With an on-chip clock synthesizer, the FT4222H may operate with a low-cost 12 MHz crystal (or oscillator) by connecting to XSCI and XSCO, and generates a standard internal 480 MHz clock for the USB interface. The Clock Synthesizer takes the 480MHz clock from the embedded UTMI PHY and generates the 80MHz, 60MHz, 48MHz and 24MHz as reference clocks. The user can select one of these reference clocks via the API, FT4222_SetClock which is defined in LibFT4222, as the system operating clock. The system operating clock will be the base and used by the embedded functions to generate the required interface clock.

Protocol Control Engine. The FT4222H has an embedded and robust control engine. It deals with the USB enumeration commands and flow control between driver and function such as SPI or I^2C devices. It can perform the bridge function initialization and enable an exceptional data transfer performance through the USB bus. It collects and summarizes the SPI and I^2C bus protocol and simplifies the protocol as a command set via the USB Bulk transfer pipe. A support library, LibFT4222, is defined for the FT4222H and is responsible for communicating with this protocol engine. With related APIs (Application Programming Interface) defined in LibFT4222, this control engine provides a very flexible USB bridge for SPI and I^2C bus access suitable for a wide range of applications.

OTP Controller + Internal OTP Memory. The internal OTP memory provides storage for vendor configuration data. This vendor configuration area, named as user area, is used to store USB Vendor ID (VID), Product ID (PID), device serial number, product description string and various other USB configuration descriptors. It is also used to configure the function pins capability. For further details refer to Section 9. This user area in the internal OTP memory is available to system designers to allow storing additional data from the user application over USB. The internal OTP memory can be programmed in circuit, over USB with an external voltage requirement on the VPP pin (6.5V). The descriptors can be programmed using the FTDI utility software called FT_PROG, which can be downloaded from FTDI Utilities on the FTDI website (http://www.ftdichip.com/Support/Utilities.htm#FT_Prog).

5V-3.3V-1.8V LDO regulator. The LDO will regulate out 2 reference voltages for use within the FT4222H. The +3.3V LDO regulator generates the +3.3V reference voltage for driving the USB transceiver cell output buffers. It requires an external decoupling capacitor to be attached to the VOUT3V3 regulator output pin. Another +1.8V LDO regulator generates the +1.8V reference voltage for driving the internal core of the IC.

POR RESET Generator. POR is the integrated Power on Reset Generator Cell providing a reliable power-on reset to the device internal circuitry at power up. There is also a RESETN input pin allowing an external device to reset the FT4222H. RESETN can be tied to VCCIO (+3.3v) if not being used.

Embedded BCD Detection. Supports Battery Charger Detection. The BCD_DET pin will be active if the device is connected to a dedicated charger instead of a standard USB Host. Refer to section 7.5 for an example application circuit.

5 FT4222H Chip Mode Configuration and SPI/I²C Interface

5.1 Chip Mode Configuration

The FT4222H has 4 configuration modes selected by {DCNF1, DCNF0}. The chip configuration mode will determine the number of USB interfaces for data streams and for GPIO control. The data stream interface is for data transfer between the USB2.0 host and the SPI/ I²C device. The purpose of the GPIO interface is for fully controlling the GPIOs. The following table shows the pin functions corresponding to the chip configuration mode.

Pin Functions	CNFMODE0 {DCNF1, DCNF0} = 00	CNFMODE1 {DCNF1, DCNF0} = 01	CNFMOD2 {DCNF1, DCNF0} = 10	CNFMODE3 {DCNF1, DCNF0} = 11
USB interface number	1 for data stream 1 for GPIOs	3 for data stream 1 for GPIOs	4 for data stream	1 for data stream
SPI Master(SPIM) related pins (SCK, MISO, MOSI, IO2,IO3, SS0O)	SPIM*	Active USB interface-0	Active USB interface-0	SPIM*
SPI Slave(SPIS) related pins (SCK, MISO, MOSI, SS)	SPIS*	Disable	Disable	SPIS*
GPIO0	GPIO/SCL*	SS1O USB interface-1	SS1O USB interface-1	SCL*
GPIO1	GPIO/SDA*	SS2O USB interface-2	SS2O USB interface-2	SDA*
GPIO2	GPIO/SUSP	GPIO/SUSP	SS3O USB interface-3	SUSP
GPIO3	GPIO/WAKE/INTR	GPIO/WAKE/INTR	WAKE	WAKE

Table 5.1 FT4222H Pin Functions on Chip Configuration Mode

*One of the SPIM, SPIS, I²C function is selected, the other 2 functions will be disabled

Note that GPIOx pins cannot be controlled by the software driver when GPIOx pins play the role as SPIM SSxO, I²C SCL/SDA, SUSP or WAKE.

Chip Configuration only determines the number of interface/functions supported but do not decide which bus interface (SPI/ I²C /GPIO) or which role (master/slave) that the FT4222H will take. The user can use the initialisation APIs provided by the support library, LibFT4222, to configure which interface and role will be taken.

The support library for FT4222H, LibFT4222, which is based on D2XX, provides high-level and convenient APIs (Application Programming Interface) to speed up user application development. For further details refer to the User Guide For LibFT4222.

5.2 SPI Bus Interface

5.2.1 SPI Pin Definition

The QuadSPI function in the FT4222H is a fully configurable SPI master/slave device. Users can utilize the API in LibFT4222, FT4222_SPIMaster_Init or FT4222_SPISlave_Init, to select in which mode (master or slave) the FT4222H will function. When the FT4222H is set as a USB-to-SPI bridge function, and chip configuration mode is chosen, the pins of the FT4222H will be mapped accordingly.
The SPI related pins are

- Clock – SCK (pin-8), 4 types of transfer formats supported, details refer to Section5.2.2
- Data – MISO (pin-9), data transfer from slave to master for single mode, or
  data bus bit-1 for dual and quad mode
  – MOSI (pin-10), data transfer from master to slave for single mode, or
  data bus bit-0 for dual and quad mode
  – IO2 (pin-11), data bus bit-2 for quad mode
  – IO3 (pin-12), data bus bit-3 for quad mode
- Slave Selection when QuadSPI acts as SPI master
  – SS0O (pin-17), slave selection to slave device-0
  – SS1O (pin-13), slave selection to slave device-1
  – SS2O (pin-14), slave selection to slave device-2
  – SS3O (pin-15), slave selection to slave device-3
- Slave Selection when QuadSPI acts as SPI slave
  – SS (pin-32), slave selection for SPI master control. Must tie high when QuadSPI acts as SPI master

5.2.2 SPI Bus Protocol

The QuadSPI allows SPI data transfers in three types of bit width:

- Single SPI transfer – Standard data transfer format – data is read and written simultaneously
- DUAL SPI Transfer/Receive - Data is transferred out or received in on 2 SPI lines simultaneously
- QUAD SPI Transfer/Receive – Data is transferred out or received in on 4 SPI lines simultaneously

The operating bit width in single, dual or quad mode can also be determined by these 2 APIs, FT4222_SPIMaster_Init and FT4222_SPISlave_Init, which are defined in LibFT4222 when the SPI function is enabled and selected.

When the FT4222H is operating as an SPI master or slave device, QuadSPI can transfer data in single bit mode with full-duplex transmission. Figure5.1 shows the basic protocol in single transfer mode

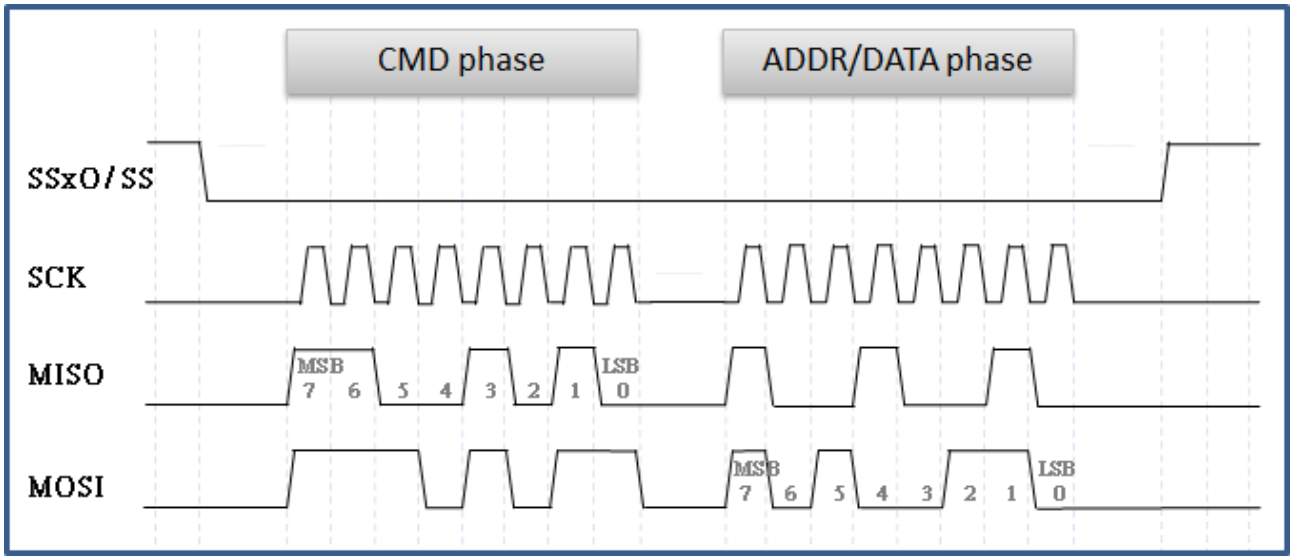

Figure 5.1 QuadSPI Bus Protocol when Transferring in Single Mode

QuadSPI can operate in dual or quad transfer mode when QuadSPI is programmed as an SPI master. These multi-bit transfer modes can speed up the data transfer rate between QuadSPI and the SPI slave device supporting the multi-bit transfer. Figure5.2 shows the bus protocol in dual or quad mode

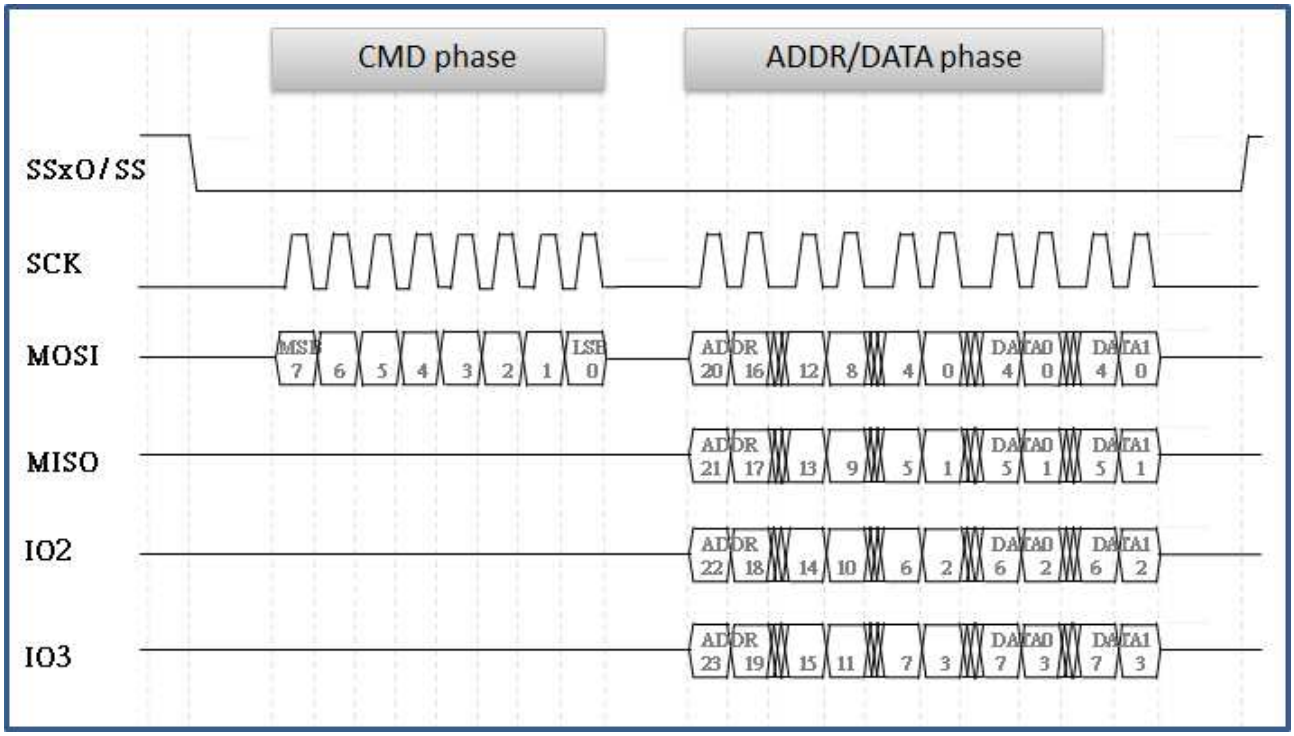

Figure 5.2 QuadSPI Bus Protocol when Transferring in Quad Mode

5.2.3 SCK Format

Software can select any of four combinations of serial clock (SCK) phase and polarity. The clock polarity is specified by the CPOL control bit, which selects an active high or active low clock and has no significant effect on the transfer format. The clock phase (CPHA) control bit selects one of two fundamentally different transfer formats. The clock phase and polarity should be identical for the master SPI device and the communicating slave device. In some cases, the phase and polarity are changed between transfers to allow a master device to communicate with peripheral slaves having different requirements. The flexibility of the SPI system on the QuadSPI allows direct interface to almost any existing synchronous serial peripheral. Users can also use the FT4222_SPIMaster_Init API which is defined in the support library LibFT4222 to select the operating phase and polarity of SCK.

5.2.3.1 CPHA=0 Transfer Format

Figure5.3 shows a timing diagram of an SPI transfer where CPHA is equal to 0. Two waveforms are shown for SCK: one for CPOL equal to 0 and another for CPOL equal to 1. The diagram may be interpreted as a master or slave timing diagram since the SCK, master in/slave out (MISO), and master out/slave in (MOSI) pins are directly connected between the master and the slave. The MISO signal is the output from the slave, and the MOSI signal is the output from the master.

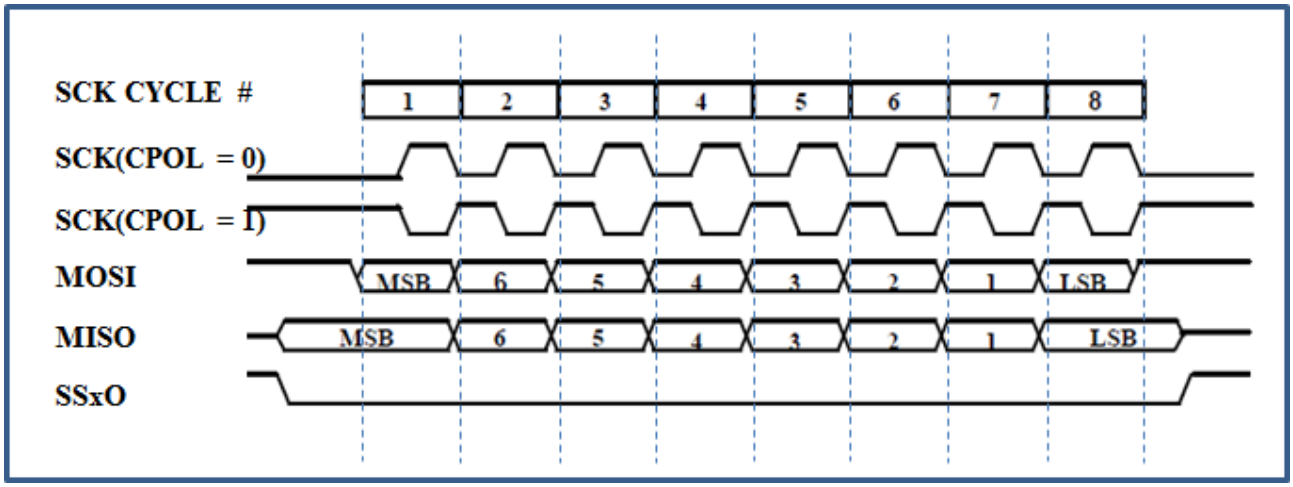

Figure 5.3 SCK Transfer Format when CPHA=0

5.2.3.2 CPHA=1 Transfer Format

Figure 5.4 is a timing diagram of an SPI transfer where CPHA equal to 1. Two waveforms are shown for SCK: one for CPOL equal to 0 and another for CPOL equal to 1. The diagram may be interpreted as a master or slave timing diagram since the SCK, MISO, and MOSI pins are directly connected between the master and the slave. The MISO signal is the output from the slave, and the MOSI signal is the output from the master. The SS line is the slave select input to the slave.

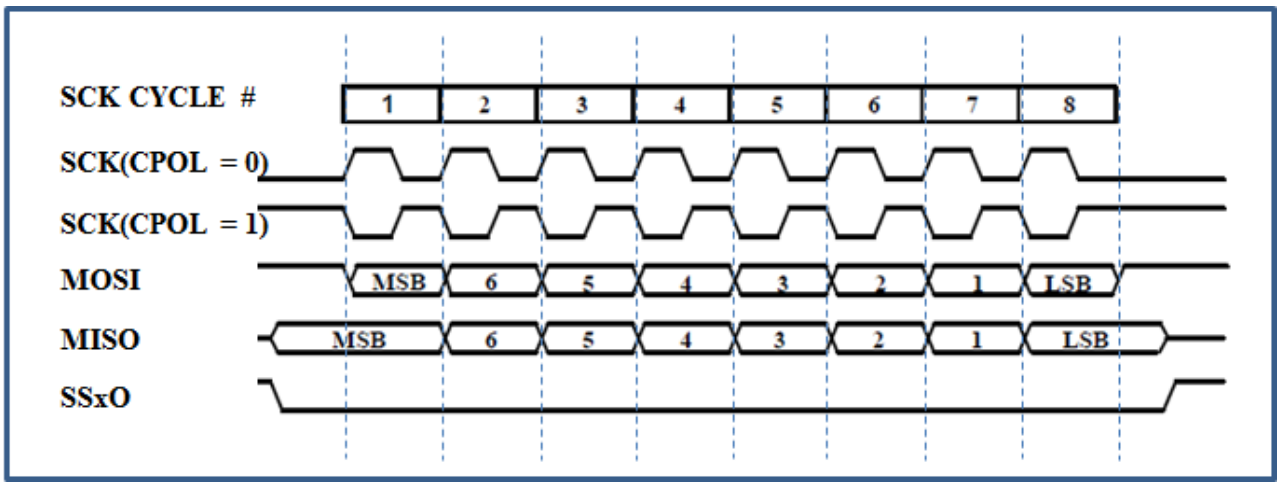

Figure 5.4 SCK Transfer Format when CPHA=1

5.2.4 SPI Timing

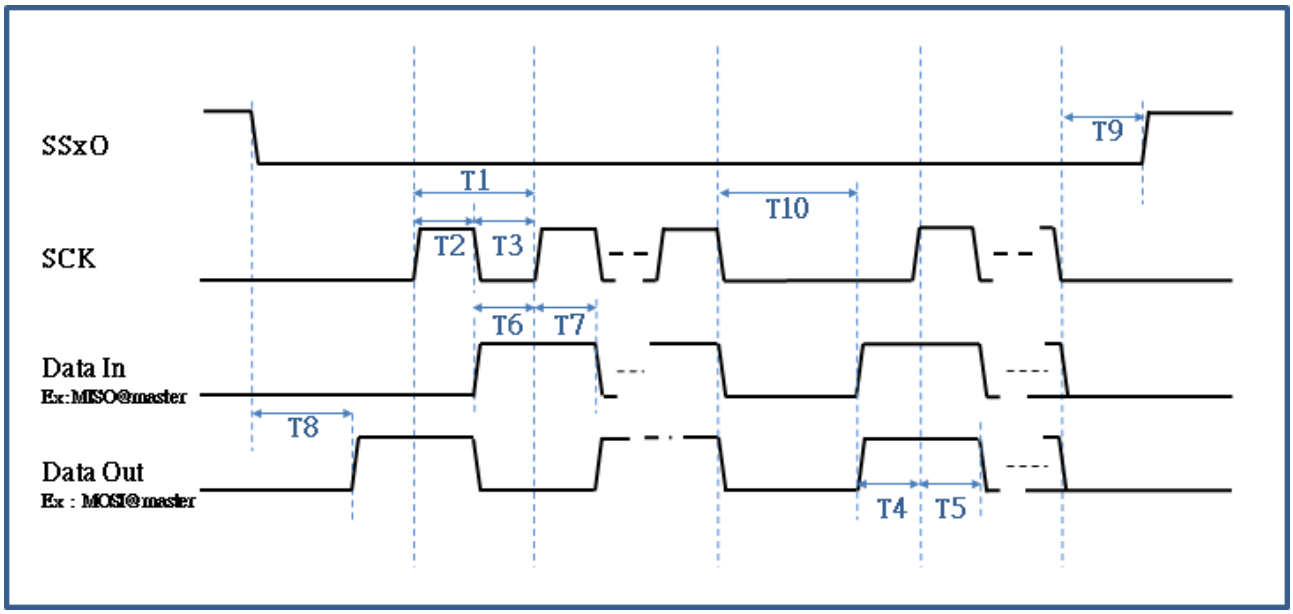

Figure 5.5 SPI Timing

The Table5.2 shows the timing information for QuadSPI. The result is under the condition of all the related pins with 5pF loading. T6 is the required setup time to the related SCK edge for the input data path of QuadSPI. The minimum value of T4 means that the guaranteed setup time to the related SCK edge for connected device to fetch data from QuadSPI. The maximum value of T6 means that data can be accepted correctly by QuadSPI with 5pF pin loading assumed. If the pin load is larger, the timing should be considered conservatively.

Parameter	Min (ns)	Typ(ns)	Max(ns)	Description
T1@master	T2+T3			SCK Period when QuadSPI as master
T1@slave	50			Acceptable SCK Period when QuadSPI as slave device
T2	12.5			SCK HIGH, related to the operating clock and ratio
T3	12.5			SCLK LOW, related to the operating clock and ratio
T4	T3-2.0		T3-1.1	Data output path: setup time to corresponding SCK edge
T5	T2+0.1		T2+0.6	Data output path: hold time to corresponding SCK edge
T6	9.8			Data input path: required setup time to corresponding SCK edge
T7			0.1	Data input path: required hold time to corresponding SCK edge
T8		6*T1		SSxO setup time to 1st SCK period boundary
T9		6*T1		SSxO hold time from last SCK period boundary
T10@master		6*T1		Idle time on SCK between byte boundary when master
T10@slave	0			Idle time on SCK between byte boundary when slave

Table 5.2 SPI Timing for VCCIO=3.3V with 5pF output pin load

Table5.3 shows the timing information for QuadSPI with VCCIO equal to 1.8V and with 5pF loading on all the related pins. The required setup time for input path is increasing since VCCIO=1.8V. The maximum operating frequency of SCK is recommended not exceeded 30MHz.

Parameter	Min (ns)	Typ(ns)	Max(ns)	Description
T1@master	T2+T3			SCK Period when QuadSPI as master
T1@slave	50			Acceptable SCK Period when QuadSPI as slave device
T2	16.67			SCK HIGH, related to the operating clock and ratio
T3	16.67			SCLK LOW, related to the operating clock and ratio
T4	T3-2.1		T3-1.2	Data output path: setup time to corresponding SCK edge
T5	T2+0.1		T2+0.6	Data output path: hold time to corresponding SCK edge
T6	8.6		16.5	Data input path: required setup time to corresponding SCK edge
T7			0.1	Data input path: required hold time to corresponding SCK edge
T8		6*T1		SSxO setup time to 1st SCK period boundary
T9		6*T1		SSxO hold time from last SCK period boundary
T10@master		6*T1		Idle time on SCK between byte boundary when master
T10@slave	0			Idle time on SCK between byte boundary when slave

Table 5.3 SPI Timing for VCCIO=1.8V with 5pF output pin load

5.3 I²C Bus Interface

I²C (Inter Integrated Circuit) is a multi-master serial bus invented by Philips. I²C uses two bi-directional open-drain wires called serial data (SDA) and serial clock (SCL). Common I²C bus speeds are standard mode (SM) with bit rate up to 100 Kbit/s, fast mode (FM) with bit rate up to 400 Kbit/s, Fast mode plus (FM+) with bit rate up to 1 Mbit/s, and High Speed mode (HS) with the bit rate up to 3.4 Mbit/s.

An I²C bus node can operate either as a master or a slave:

- Master node – issues the clock and addresses slaves
- Slave node – receives the clock line and address.

The FT4222H can operate as a master or slave, and is capable of being set to the speed modes defined in the I²C bus specification. Besides the speed mode defined in the I²C standard specification, the I²C controller of the FT4222H can support flexible SCL frequencies defined by the following function

$$SCL\ Freq = \frac{\text{Operating Clock Frequency}}{M*(N+1)} \quad M = 6\ or\ 8;\ \ N = 1, 2, 3, \ldots\ldots, 127$$

When the target frequency is below 100 KHz, M will be equal to 8; otherwise, M will be equal to 6. For example, to generate a 2.5MHz frequency on SCL, M will be selected as 6. Then with an operating clock frequency equal to 60MHz the user can set N as 3. The SCL frequency for I²C master mode can be set via the FT4222_I2CMaster_Init command defined in the support library, LibFT4222. Refer to the User Guide For LibFT4222 for further details.

5.3.1 I²C Pin Definition

The I²C function in the FT4222H is a fully configurable I²C master/slave device. When the chip configuration is set as CNFMODE0 or CNFMODE3 and the USB-to-I²C bridge function is enabled via the FT4222_I2CMaster_Init API which is defined in the support library LibFT4222. The pins of the FT4222H will be mapped accordingly. The I²C pins are

- Clock – SCL (pin-13), as clock output with open-drain design when I²C bus is set as master.
  as clock input when I²C bus is set as slave.
- Data – SDA (pin-14), command/address/data transfer between master and slave with open-drain design

5.3.2 I²C Bus Protocol

There are four potential modes of operation for a given bus device, although most devices only use a single role (Master or Slave) and its two modes (Transmit and Receive):

- Master transmit – sending data to a slave
- Master receive – receiving data from a slave
- Slave transmit – sending data to a master
- Slave receive – receiving data from the master

The following figure shows the basic I²C bus protocol

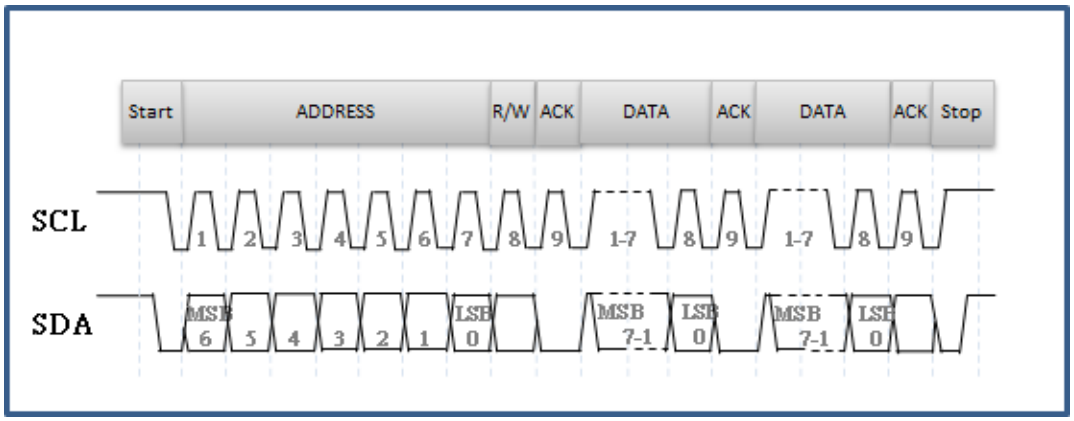

Figure 5.6 I²C Bus Protocol

The master is initially in master transmit mode by sending a start bit followed by the 7-bit address of the slave it wishes to communicate with, which is finally followed by a single bit representing whether it wishes to write(0) to or read(1) from the slave.

If the slave exists on the bus then it will respond with an ACK bit (active low for acknowledged) for that address. The master then continues in either transmit or receive mode (according to the read/write bit it sent), and the slave continues in its complementary mode (receive or transmit, respectively).

The address and the data bytes are sent most significant bit first. The start bit is indicated by a high-to-low transition of SDA with SCL high; the stop bit is indicated by a low-to-high transition of SDA with SCL high.

If the master wishes to write to the slave then it repeatedly sends a byte with the slave sending an ACK bit. (In this situation, the master is in master transmit mode and the slave is in slave receive mode.)

If the master wish to read from the slave then it repeatedly receives a byte from the slave, the master sends an ACK bit after every byte but the last one. (In this situation, the master is in master receive mode and the slave is in slave transmit mode.)

The master then ends transmission with a stop bit, or it may send another START bit if it wishes to retain control of the bus for another transfer (a "combined message").

I²C defines three basic types of message, each of which begins with a START and ends with a STOP:

- Single message where a master writes data to a slave;
- Single message where a master reads data from a slave;
- Combined messages, where a master issues at least two reads and/or writes to one or more slaves

In a combined message, each read or write begins with a START and the slave address. After the first START, these are also called repeated START bits; repeated START bits are not preceded by STOP bits, which is how slaves know the next transfer is part of the same message.

Users can refer to the I^2C specification for more information on the protocol.

5.3.3 I^2C Slave Address

When the FT4222H is configured as a USB to I²C master bridge, it must be able to issue any value of 7-bits slave address. Users can issue I^2C commands to read or write data to a slave via the commands FT4222_I2CMaster_Read and FT4222_I2CMaster_Write, defined in the support library LibFT4222, with a corresponding slave address.

When the FT4222H is configured as a USB to I²C slave bridge, the slave address may be defined by the user. This slave address parameter is defined by default as 40h and can be set once in the I²C Slave Address parameter which is defined in the user data area of the OTP memory. For further details refer to Section 9.

5.3.4 I^2C Timing

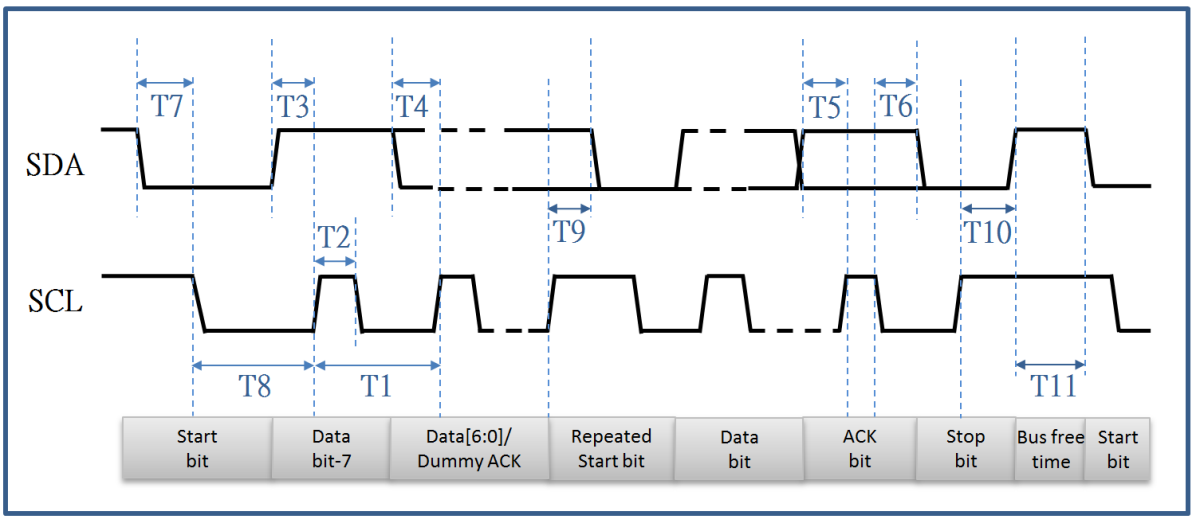

Figure 5.7 I^2C Bus Timing

Parameter	Min(ns)	Typ(ns)	Max(ns)	Description
T0@48MHz		20.833		T0 is the period when operating clock=48MHz
T0@60MHz		16.666		T0 is the period when operating clock=60MHz
T0@80MHz		12.500		T0 is the period when operating clock=80MHz
Timing for I^2C Master				
T1@SM	16*T0	8*(1+N)*T0		SCK Period when I^2C as master with standard speed mode(SM)
T1@FM/HM	12*T0	6*(1+N)*T0		SCK Period when I^2C as master with FM, FM+, HS speed mode
T2	8*T0	4*(1+N)*T0		SCK high pulse width when I^2C as master with standard speed mode(SM)
T2	4*T0	2*(1+N)*T0		SCK high pulse width when I^2C as master with FM, FM+, HS speed mode
T3		2*(1+N)*T0		SDA output setup time to SCL rising edge when I^2C as master
T4		2*(1+N)*T0		SDA output hold time to SCL falling edge when I^2C as master
T5			>=0	input setup time requirement from SDA to SCL rising edge when I^2C as master
T6			>=0	input hold time requirement from SDA to SCL falling edge when I^2C as master
T7		2*(1+N)*T0		Start bit setup time to SCL falling edge
T8		4*(1+N)*T0		Start bit hold time to SCL falling edge
T9		2*(1+N)*T0		Stop bit setup time to SCL rising edge
T10		2*(1+N)*T0		Stop bit hold time to SCL rising edge
T11	4*(1+N)*T0			Bus free time between Start and Stop bit
Timing for I^2C Slave				
T1	12*T0			Acceptable SCL Period when I^2C as slave device
T2	1*T0			SCL high pulse width requirement when I^2C as slave
T3			>=0	input setup time requirement from SDA to SCL rising edge when I^2C as slave device
T4	1*T0			input hold time requirement from SDA to SCL falling edge when I^2C as slave device
T5	T8 - T6			SDA output setup time to SCL rising edge
T6	3*T0	4*T0	5*T0	SDA output hold time to SCL falling edge

Table 5.4 I^2C Timing for VCCIO=3.3V

Note that N can be ranged from 1 to 255

5.4 GPIOs

When the configuration mode of the FT4222H is set as CNFMODE0 or CNFMODE1, a GPIO pipe will be enabled. These 4 pins, GPIO0, GPIO1, GPIO2 and GPIO3, can be set as general purpose Input/Output pins or other functions such as multi-channel SPI slave selections, I^2C interface, suspend out indicator, remote wake up input or interrupt. If no functions are set on these pins, the default function is GPIO. The user can set the direction for GPIOs via the API, FT4222_GPIO_Init, defined in LibFT4222. The logic level can be read and written via the APIs, FT4222_GPIO_Read and FT4222_GPIO_Write.

The FT4222H also provides an interrupt input source for the user to utilize. GPIO3(pin-16) can be set as an interrupt input source via the API**,** FT4222_SetWakeUpInterrupt, defined in LibFT4222. GPIO3 can be set as a rising edge or falling edge triggered interrupt via FT_Prog. The related parameter defined in the user area is named as the interrupt trigger edge. The default setting is raising edge triggered. Details can be referenced in Table9.1.

Figure5.8 shows the different behaviour when GPIO3 acts as GPIO or interrupt. The interrupt is set by default as rising edge triggered. Users can choose either one for their application.

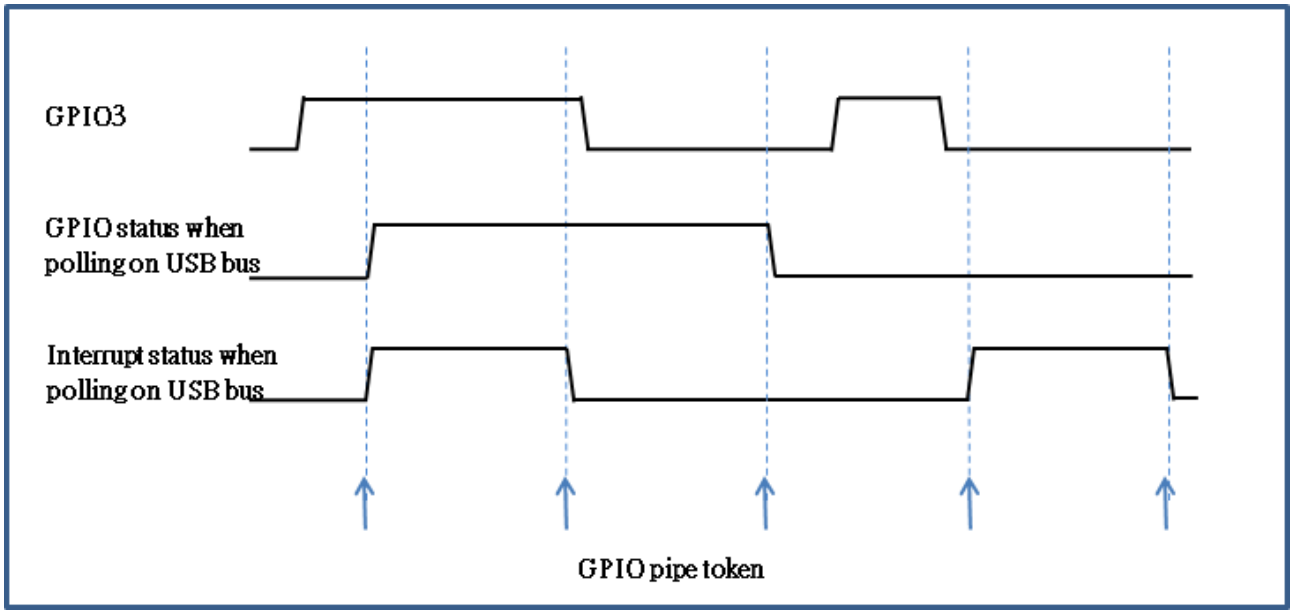

Figure 5.8 Different status when GPIO3 set as GPIO or interrupt input

6 Devices Characteristics and Ratings

6.1 Absolute Maximum Ratings

The absolute maximum ratings for the FT4222H devices are as follows. These are in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these may cause permanent damage to the device.

Parameter	Value	Unit	Conditions
Storage Temperature	-65°C to 150°C	Degrees C	
Floor Life (Out of Bag) At Factory Ambient (30°C / 60% Relative Humidity)	168 Hours (IPC/JEDEC J-STD-033A MSL Level 3 Compliant)*	Hours	
Ambient Operating Temperature (Power Applied)	-40°C to 85°C	Degrees C	
MTTF FT4222H	TBD	Hours	
VCCIN Supply Voltage	-0.3 to +5.5	V	
VCCIO IO Voltage	-0.3 to +4.0	V	
VPP Supply Voltage	6.5±0.25	V	
DC Input Voltage – USBDP and USBDM	-0.5 to +3.63	V	
DC Input Voltage – High Impedance Bi-directional (powered from VCCIO)	-0.3 to +(VCCIO+0.5V)	V	
DC Output Current – Outputs	100 **	mA	

Table 6.1 Absolute Maximum Ratings

* If devices are stored out of the packaging beyond this time limit the devices should be baked before use. The devices should be ramped up to a temperature of +125°C and baked for up to 17 hours.

** This DC output current is also the power supply source for FT4222H operation. If it must be the source for other component on the system, it only can supply 25mA or less.

6.2 ESD and Latch-up Specifications

Description	Specification
Human Body Mode (HBM)	**> ± 2kV**
Machine mode (MM)	**> ± 200V**
Charged Device Mode (CDM)	**> ± 500V**
Latch-up	**> ± 200mA**

Table 6.2 ESD and Latch-Up Specifications

6.3 DC Characteristics

DC Characteristics (Ambient Temperature = -40°C to +85°C)

Parameter	Description	Minimum	Typical	Maximum	Units	Conditions
VCC1	VCCIN Operating Supply Voltage	4.5	5	5.5	V	VCCIN is supplied with 5V
		2.97	3.3	3.63V	V	VCCIN is supplied with 3.3V
VCC2	VCCIO Operating Supply Voltage	2.97	3.3	3.63	V	VCCIO is supplied with 3.3V
		2.25	2.5	2.75	V	VCCIO is supplied with 2.5V
		1.62	1.8	1.98	V	VCCIO is supplied with 1.8V
Icc1	Operating Supply Current		50	52	mA	Normal Operation at 24MHz
			62	64	mA	Normal Operation at 48MHz
			68	70	mA	Normal Operation at 60MHz
			78	80	mA	Normal Operation at 80MHz
Icc2	Suspend Supply Current		375	460	µA	USB Suspend when SPI Master
			377	465	µA	USB Suspend when SPI Slave
			386	419	µA	USB Suspend when I^2C Master
			388	456	µA	USB Suspend when I^2C Slave
3V3	3.3v regulator output	2.97	3.3	3.63	V	VCCIN must be greater than 3V3 otherwise VOUT3V3 is an input which must be driven with 3.3V

Table 6.3 Operating Voltage and Current