Chipsmall Limited consists of a professional team with an average of over 10 year of expertise in the distribution of electronic components. Based in Hongkong, we have already established firm and mutual-benefit business relationships with customers from,Europe,America and south Asia,supplying obsolete and hard-to-find components to meet their specific needs.

With the principle of “Quality Parts,Customers Priority,Honest Operation,and Considerate Service”,our business mainly focus on the distribution of electronic components. Line cards we deal with include Microchip,ALPS,ROHM,Xilinx,Pulse,ON,Everlight and Freescale. Main products comprise IC,Modules,Potentiometer,IC Socket,Relay,Connector.Our parts cover such applications as commercial,industrial, and automotives areas.

We are looking forward to setting up business relationship with you and hope to provide you with the best service and solution. Let us make a better world for our industry!

Contact us

Tel: +86-755-8981 8866 Fax: +86-755-8427 6832
Email & Skype: info@chipsmall.com Web: www.chipsmall.com
Address: A1208, Overseas Decoration Building, #122 Zhenhua RD., Futian, Shenzhen, China

PRELIMINARY Product Specification

40GE SWDM4 QSFP+ Optical Transceiver Module

FTL4S1QE1C

PRODUCT FEATURES

- Hot-pluggable QSFP+ form factor
- 240m operation over duplex OM3 MMF (350m over OM4, 440m over OM5)
- Supports 41.2 Gb/s aggregate bit rates
- Uncooled 4x10Gb/s SWDM transmitter
- Built-in SWDM mux and demux
- Power dissipation < 2.5W
- Commercial case temperature range 0°C to 70°C
- XLPPI electrical interface
- Duplex LC receptacles
- Built-in digital diagnostic functions, including Tx/Rx power monitoring
- RoHS-6 compliant

APPLICATIONS

- 40G Ethernet over duplex MMF
- Allows upgrades from 10GBASE-SR without changing fiber plant

Finisar's FTL4S1QE1C QSFP+ transceiver modules are designed for use in 40 Gigabit Ethernet links over duplex multimode fiber. They are compliant with the QSFP+ MSA[1,2] and IEEE 802.3ba XLPPI electrical interface[3]. Digital diagnostics functions are available via an I2C interface, as specified by the QSFP+ MSA. The optical transceiver is compliant per the RoHS Directive 2011/65/EU. See Finisar Application Note AN-2038 for more details.

PRODUCT SELECTION

FTL4S1QE1C

FTL: Finisar transceiver
4: 4 optical WDM channels
S1: Shortwave WDM
Q: QSFP+ form factor
E: Ethernet
1: First generation product
C: Commercial temperature range

I. Pin Descriptions

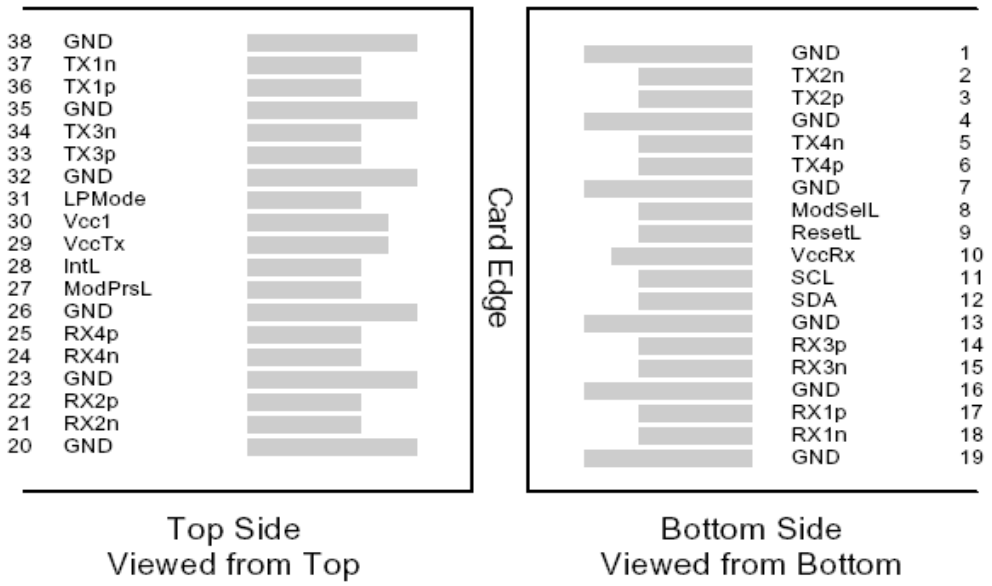

Figure 1 – QSFP+ MSA-compliant 38-pin connector

Pin	Symbol	Name/Description	Notes
1	GND	Ground	1
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	1
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	1
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	Vcc Rx	+3.3 V Power supply receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	1
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	1
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	1
20	GND	Ground	1
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	1
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	

26	GND	Ground	1
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	Vcc Tx	+3.3 V Power supply transmitter	
30	Vcc1	+3.3 V Power Supply	
31	LPMode	Low Power Mode	
32	GND	Ground	1
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	1
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	1

Notes
1. Circuit ground is internally isolated from chassis ground.

II. General Product Characteristics

Parameter	Value	Unit	Notes
Module Form Factor	QSFP+		
Maximum Aggregate Data Rate	41.2	Gb/s	
Maximum Data Rate per Lane	10.3	Gb/s	
Protocols Supported	40G Ethernet		
Electrical Interface and Pin-out	38-pin edge connector		Pin-out as defined by the QSFP+ MSA
Maximum Power Consumption	2.5	Watts	1
Management Interface	Serial, I2C-based, 400 kHz maximum frequency		As defined by the QSFP+ MSA

Notes:
1. Will be <2.5W in link established mode. If the input optical signal is without data, the CDR will keep searching and push the power consumption over the maximum spec.

Data Rate Specifications	Symbol	Min	Typ	Max	Units	Ref.
Bit Rate per Lane	BR			10.3125	Mb/sec	1
Bit Error Ratio	BER			10^{-12}		2
Link distance on OM3	d	0		240	meters	
Link distance on OM3, CDR off	d	0		200	meters	
Link distance on OM4	d	0		350	meters	

Notes:
1. Compliant with XLPPI per IEEE 802.3ba.
2. Tested with a PRBS 2^{31}-1 test pattern.

III. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Maximum Supply Voltage	Vcc1, VccTx, VccRx	-0.5		3.6	V	
Storage Temperature	T_S	-40		85	°C	
Case Operating Temperature	T_{OP}	0		70	°C	
Relative Humidity	RH	0		85	%	1
Damage Threshold, per Lane	DT	4			dBm	

Notes:
1. Non-condensing.

IV. Electrical Characteristics (T_{OP} = 0 to 70°C, V_{CC} = 3.1 to 3.47 Volts)

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Supply Voltage	Vcc1, VccTx, VccRx	3.1		3.47	V	
Supply Current	Icc			0.9	A	1
Link turn-on time						
Transmit turn-on time				2000	ms	2
Transmitter (per Lane)						
Single-ended input voltage tolerance	VinT	-0.3		4.0	V	
Differential data input swing	Vin,pp	120		1200	mVpp	3
Differential input threshold			50		mV	
AC common mode input voltage tolerance (RMS)		15			mV	
Differential input return loss		Per IEEE P802.3ba, Section 86A.4.1.1			dB	4
J2 Jitter Tolerance	Jt2	0.17			UI	
J9 Jitter Tolerance	Jt9	0.29			UI	
Data Dependent Pulse Width Shrinkage	DDPWS	0.07			UI	
Eye mask coordinates {X1, X2 Y1, Y2}		0.11, 0.31 95, 350			UI mV	5
Receiver (per Lane)						
Single-ended output voltage		-0.3		4.0	V	
Differential data output swing	Vout,pp	200		400	mVpp	6, 7
		300		600		
		400		800		
		600		1200		
AC common mode output voltage (RMS)				7.5	mV	
Termination mismatch at 1 MHx				5	%	
Differential output return loss		Per IEEE P802.3ba, Section 86A.4.2.1			dB	4
Common mode output return loss		Per IEEE P802.3ba, Section 86A.4.2.2			dB	4
Output transition time, 20% to 80%		28			ps	
J2 Jitter output	Jo2			0.42	UI	
J9 Jitter output	Jo9			0.65	UI	

Eye mask coordinates #1 {X1, X2 Y1, Y2}		0.29, 0.5 150, 425			UI mV	5
Power Supply Ripple Tolerance	PSR	50			mVpp	

Notes:

1. Will be <2.5W in link established mode. If the input optical signal is without data, the CDR will keep searching and push the supply current over the maximum spec.
2. From power-on and end of any fault conditions.
3. After internal AC coupling. Self-biasing 100Ω differential input.
4. 10 MHz to 11.1 GHz range.
5. Hit ratio = 5 x 10E-5.
6. AC coupled with 100Ω differential output impedance.
7. Output voltage is settable in 4 discrete steps via I2C.

V. Optical Characteristics (T_{OP} = 0 to 70°C, V_{CC} = 3.1 to 3.47 Volts)

Per-channel optical characteristics vary over the 4 wavelengths. Below are the worst-case

Parameter	Symbol	Min	Typ	Max	Unit	Ref.
Transmitter						
Signaling Speed per Lane			10.3125		GBd	1
Lane center wavelengths			850 880 910 940		nm	
Spectral width @ 850nm	SBW			0.53		
Spectral width @ 880nm, 910nm, 940nm	SBW			0.59	nm	
Total Average Launch Power	P_{OUT}	-1.6		9.0	dBm	3
Average Launch Power per Lane	TXP_x	-7.6		3.0	dBm	2,3
Transmit OMA per Lane	TxOMA	-5.3		3	dBm	2
Launch Power Tx OMA - TDP		-6.6			dBm	
Transmitter and Dispersion Penalty	TDP			4.9	dB	2
Optical Extinction Ratio	ER	3.0			dB	
Average launch power of OFF transmitter, per lane				-30	dBm	
Relative Intensity Noise	RIN			-128	dB/Hz	4
Optical Return Loss Tolerance		12			dB	
Transmitter eye mask definition {X1, X2, X3, Y1, Y2, Y3}		0.23, 0.34, 0.43, 0.27, 0.35, 0.4				
Receiver						
Signaling Speed per Lane			10.3125		GBd	5
Lane center wavelengths			850 880 910 940		nm	
Average Receive Power per Lane	RXP_x	-9.0		3.0	dBm	2,6
Receive Power (OMA) per Lane	RxOMA			3	dBm	2
Receiver Sensitivity (OMA) per Lane	Rxsens			-9.1	dBm	2,7
Stressed Receiver Sensitivity (OMA) per Lane @ 850nm	SRS			-5.7	dBm	2
Stressed Receiver Sensitivity (OMA) per Lane @ 880nm, 910nm, 940nm	SRS			-4.4	dBm	2

Return Loss	RL			12	dB	
LOS De-Assert	LOS_D			-13	dBm	
LOS Assert	LOS_A	-30			dBm	
LOS Hysteresis		0.5			dB	

Notes:
1. Transmitter consists of 4 lasers operating at 10.3Gb/s each.
2. This value varies among the 4 channels. The value shown is for the worst-case channel.
3. Minimum value is informative.
4. Maximum value is informative. TDP guarantees Tx performance
5. Receiver consists of 4 photodetectors operating at 10.3 Gb/s each.
6. Minimum value is informative, equals min TxOMA with infinite ER and max channel insertion loss.
7. Maximum value is informative based on a theoretical perfect unstressed optical source

VI. Memory Map and Control Registers

Compatible with SFF-8636 (QSFP+)[2]. See Finisar Application Note AN-2104[6] for details of the EEPROM memory map.

VII. Environmental Specifications

Finisar FTL4S1QE1C transceivers have an operating temperature range from 0°C to +70°C case temperature.

Environmental Specifications	Symbol	Min	Typ	Max	Units	Ref.
Case Operating Temperature	T_{op}	0		70	°C	
Storage Temperature	T_{sto}	-40		85	°C	

VIII. Regulatory Compliance

Finisar FTL4S1QE1C transceivers are RoHS-6 compliant.[4] Copies of certificates are available at Finisar Corporation upon request.

FTL4S1QE1C transceiver modules are Class 1M laser eye safety compliant per IEC 60825-1.

IX. Mechanical Specifications

The FTL4S1QE1C mechanical specifications are compliant to the QSFP+ MSA transceiver module specifications.

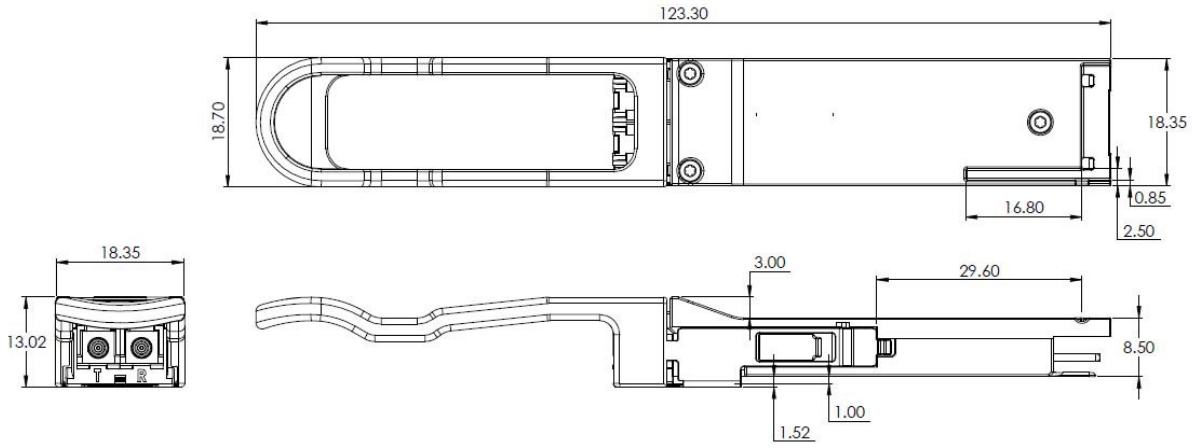

Figure 2 – FTL4S1QE1C mechanical drawing

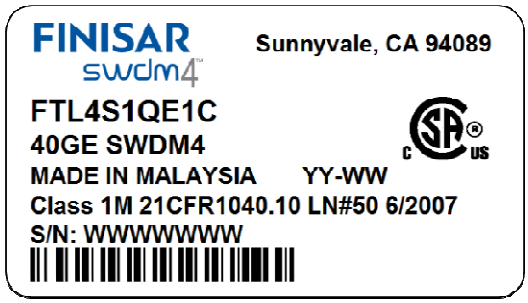

Figure 3 – FTL4S1QE1C production label

X. References

1. SFF-8436 – Specification for QSFP+ Copper and Optical Transceiver, Rev 4.8, October 2013.

2. SFF-8636 – Common Management Interface, Rev 2.7, January, 2016.

3. IEEE 802.3ba – Annex 86A "Parallel Physical Interface (nPPI) for 40GBASE-SR4 and 40GBASE-LR4 (XLPPI) and 100GBASE-SR10 (CPPI)"

4. Directive 2011/65/EU of the European Council Parliament and of the Council, "on the restriction of the use of certain hazardous substances in electrical and electronic equipment," June 8, 2011, which supercedes the previous RoHS Directive 2002/95/EC.

5. "Application Note AN-2038: Finisar Implementation of RoHS Compliant Transceivers", Finisar Corporation, January 21, 2005.

6. "Application Note AN-2104: QSFP+ 40G LR4 Transceiver EEPROM Mapping," Rev. A, Finisar Corporation, June, 2013.

XI. For More Information

Finisar Corporation
1389 Moffett Park Drive
Sunnyvale, CA 94089-1133
Tel. 1-408-548-1000
Fax 1-408-541-6138
sales@finisar.com
www.finisar.com